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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	100MHz
Non-Volatile Memory	ROM (9kB)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-TQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56301pw100

External Memory Expansion

- Data memory expansion to two 16 M × 24-bit word memory spaces in 24-Bit mode or two 64 K × 16-bit memory spaces in 16-Bit Compatibility mode
- Program memory expansion to one 16 M × 24-bit words memory space in 24-Bit mode or 64 K × 16-bit in 16-Bit Compatibility mode
- External memory expansion port
- Chip Select Logic for glueless interface to SRAMs
- Internal DRAM Controller for glueless interface to dynamic random access memory (DRAMs)

Reduced Power Dissipation

- Very low-power CMOS design
- Wait and Stop low-power standby modes
- Fully static design specified to operate down to 0 Hz (dc)
- Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)

Packaging

The DSP56301 is available in a 208-pin thin quad flat pack (TQFP) or a 252-pin molded array process-ball grid array (MAP-BGA) package. Both packages are available in lead-bearing and lead-free versions.

Target Applications

Examples of target applications include:

- Wireless and wireline infrastructure applications
- Multi-channel wireless local loop systems
- DSP resource boards
- High-speed modem banks
- Packet telephony

Product Documentation

The three documents listed in the following table are required for a complete description of the DSP56301 and are necessary to design properly with the part. Documentation is available from the following sources. (See the back cover for detailed information.)

- A local Freescale distributor
- A Freescale semiconductor sales office
- A Freescale Literature Distribution Center
- The World Wide Web (WWW)

Table 1. DSP56301 Documentation

Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD
DSP56301 User's Manual	Detailed functional description of the DSP56301 memory configuration, operation, and register programming	DSP56301UM/D
DSP56301 Technical Data	DSP56301 features list and physical, electrical, timing, and package specifications	DSP56301

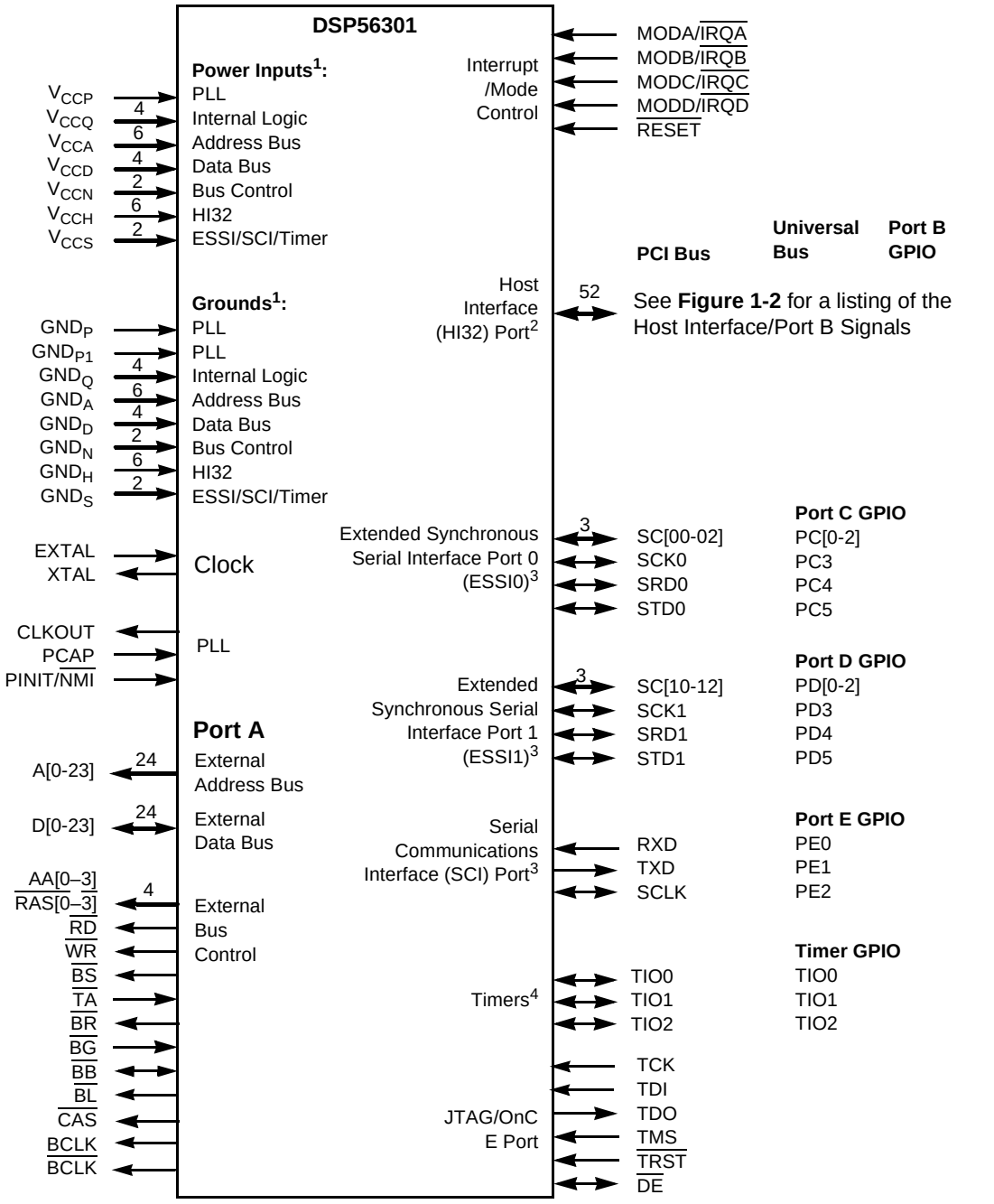
Signals/Connections 1

The DSP56301 input and output signals are organized into functional groups, as shown in **Table 1-1** and illustrated in **Figure 1-1**. The DSP56301 operates from a 3 V supply; however, some of the inputs can tolerate 5 V. A special notice for this feature is added to the signal descriptions of those inputs.

Table 1-1. DSP56301 Functional Signal Groupings

Functional Group		Number of Signals by Package Type		Detailed Description
		TQFP	MAP-BGA	
Power (V_{CC})[1]		25	45	**Table 1-2**
Ground (GND)[1]		26	38	**Table 1-3**
Clock		2	2	**Table 1-4**
PLL		3	3	**Table 1-5**
Address Bus	Port A[2]	24	24	**Table 1-6**
Data Bus		24	24	**Table 1-7**
Bus Control		15	15	**Table 1-8**
Interrupt and Mode Control		5	5	**Table 1-9**
Host Interface (HI32)	Port B[3]	52	52	**Table 1-11**
Enhanced Synchronous Serial Interface (ESSI)	Ports C and D[4]	12	12	**Table 1-12** and **Table 1-13**
Serial Communication Interface (SCI)	Port E[5]	3	3	**Table 1-14**
Timer		3	3	**Table 1-15**
JTAG/OnCE Port		6	6	**Table 1-16**

Notes:
1. The number of available power and ground signals is package-dependent. In the TQFP package specific pins are dedicated internally to device subsystems. In the MAP-BGA package, power and ground connections (except those providing PLL power) connect to internal power and ground planes, respectively.
2. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals.
3. Port B signals are the HI32 port signals multiplexed with the GPIO signals.
4. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals.
5. Port E signals are the SCI port signals multiplexed with the GPIO signals.
6. Each device also includes several no connect (NC) pins. The number of NC connections is package-dependent: the TQFP has 9 NCs and the MAP-BGA has 20 NCs. Do not connect any line, component, trace, or via to these pins. See **Chapter 3** for details.



Notes:
1. Power and ground connections are shown for the TQFP package. The MAP-BGA package uses one V_{CCP} for the PLL power input and 44 V_{CC} pins that connect to an internal power plane. The MAP-BGA package uses two ground connections for the PLL (GND_P and GND_{P1}) and 36 GND pins that connect to an internal ground plane.
2. The HI32 port supports PCI and non-PCI bus configurations. Twenty-four HI32 signals can also be configured as GPIO signals (PB[0–23]).
3. The ESSI0, ESSI1, and SCI signals are multiplexed with the Port C GPIO signals (PC[0–5]), Port D GPIO signals (PD[0–5]), and Port E GPIO signals (PE[0–2]), respectively.
4. TIO[0–2] can be configured as GPIO signals.

Figure 1-1. Signals Identified by Functional Group

Table 1-8. External Bus Control Signals (Continued)

Signal Name	Type	State During Reset	Signal Description
$\overline{BB}$	Input/ Output	Input	**Bus Busy** Indicates that the bus is active and must be asserted and deasserted synchronous to CLKOUT. Only after $\overline{BB}$ is deasserted can the pending bus master become the bus master (and then assert the signal again). The bus master can keep $\overline{BB}$ asserted after ceasing bus activity, regardless of whether $\overline{BR}$ is asserted or deasserted. This is called “bus parking” and allows the current bus master to reuse the bus without re-arbitration until another device requires the bus. $\overline{BB}$ is deasserted by an “active pull-up” method (that is, $\overline{BB}$ is driven high and then released and held high by an external pull-up resistor). $\overline{BB}$ requires an external pull-up resistor.
$\overline{BL}$	Output	Driven high (deasserted)	**Bus Lock**—$\overline{BL}$ is asserted at the start of an external divisible Read-Modify-Write (RMW) bus cycle, remains asserted between the read and write cycles, and is deasserted at the end of the write bus cycle. This provides an “early bus start” signal for the bus controller. BL may be used to “resource lock” an external multi-port memory for secure semaphore updates. Early deassertion provides an “early bus end” signal useful for external bus control. If the external bus is not used during an instruction cycle, BL remains deasserted until the next external indivisible RMW cycle. The only instructions that assert $\overline{BL}$ automatically are the BSET, CLR, and BCHG instructions when they are used to modify external memory. An operation can also assert $\overline{BL}$ by setting the BLH bit in the Bus Control Register.
$\overline{CAS}$	Output	Tri-stated	**Column Address Strobe** When the DSP is the bus master, DRAM uses $\overline{CAS}$ to strobe the column address. Otherwise, if the Bus Mastership Enable (BME) bit in the DRAM Control Register is cleared, the signal is tri-stated.
BCLK	Output	Tri-stated	**Bus Clock** When the DSP is the bus master, BCLK is active when the OMR[ATE] is set. When BCLK is active and synchronized to CLKOUT by the internal PLL, BCLK precedes CLKOUT by one-fourth of a clock cycle.
$\overline{BCLK}$	Output	Tri-stated	**Bus Clock Not** When the DSP is the bus master, $\overline{BCLK}$ is the inverse of the BCLK signal. Otherwise, the signal is tri-stated.

Table 1-11. Host Interface (Continued)

Signal Name	Type	State During Reset	Signal Description
HCLK	Input	Input	**Host Clock** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Bus Clock input. **Non-PCI bus** When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal must be connected to a pull-up resistor or directly to V_{CC}. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
HAD[16–31] HD[8–23]	Input/Output Input/Output	Tri-stated	**Host Address/Data 16–31** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, these signals are lines 16–31 of the Address/Data bus. **Host Data 8–23** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, these signals are lines 8–23 of the Data bus. **Port B** When the HI32 is configured as GPIO through the DCTR, these signals are internally disconnected. These inputs are 5 V tolerant.
$\overline{\text{HRST}}$ HRST	Input Input	Tri-stated	**Hardware Reset** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Hardware Reset input. **Hardware Reset** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Hardware Reset Schmitt-trigger signal. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
$\overline{\text{HINTA}}$	Output, open drain	Tri-stated	**Host Interrupt A** When the HI function is selected, this signal is the Interrupt A open-drain output. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
PVCL	Input	Input	**PCI Voltage Clamp** When the HI32 is programmed to interface with a PCI bus and the HI function is selected and the PCI bus uses a 3 V signal environment, connect this pin to V_{CC} (3.3 V) to enable the high voltage clamping required by the PCI specifications. In all other cases, including a 5 V PCI signal environment, leave the input unconnected.

2.5.4 Reset, Stop, Mode Select, and Interrupt Timing

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6]

No.	Characteristics	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
8	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3]	—	—	26.0	—	26.0	ns
9	Required $\overline{\text{RESET}}$ duration[4] • Power on, external clock generator, PLL disabled • Power on, external clock generator, PLL enabled • Power on, internal oscillator • During STOP, XTAL disabled (PCTL Bit 16 = 0) • During STOP, XTAL enabled (PCTL Bit 16 = 1) • During normal operation	 $50 \times ET_C$ $1000 \times ET_C$ $75000 \times ET_C$ $75000 \times ET_C$ $2.5 \times T_C$ $2.5 \times T_C$	 625.0 12.5 1.0 1.0 31.3 31.3	 — — — — — —	 500.0 10.0 0.75 0.75 25.0 25.0	 — — — — — —	 ns µs ms ms ns ns
10	Delay from asynchronous $\overline{\text{RESET}}$ deassertion to first external address output (internal reset deassertion)[5] • Minimum • Maximum	 $3.25 \times T_C + 2.0$ $20.25\ T_C + 10.0$	 42.6 —	 — 263.1	 34.5 —	 — 212.5	 ns ns
11	Synchronous reset setup time from $\overline{\text{RESET}}$ deassertion to CLKOUT Transition 1 • Minimum • Maximum	T_C	 7.4 —	 — 12.5	 5.9 —	 — 10.0	 ns ns
12	Synchronous reset deasserted, delay time from the CLKOUT Transition 1 to the first external address output • Minimum • Maximum	 $3.25 \times T_C + 1.0$ $20.25 \times T_C + 1.0$	 41.6 —	 — 258.1	 33.5 —	 — 207.5	 ns ns
13	Mode select setup time		30.0	—	30.0	—	ns
14	Mode select hold time		0.0	—	0.0	—	ns
15	Minimum edge-triggered interrupt request assertion width		8.25	—	6.6	—	ns
16	Minimum edge-triggered interrupt request deassertion width		8.25	—	7.1	—	ns
17	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory access address out valid • Caused by first interrupt instruction fetch • Caused by first interrupt instruction execution	 $4.25 \times T_C + 2.0$ $7.25 \times T_C + 2.0$	 55.1 92.6	 — —	 44.5 74.5	 — —	 ns ns
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution	$10 \times T_C + 5.0$	130.0	—	105.0	—	ns
19	Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts[1]	**80 MHz**: $3.75 \times T_C + WS \times T_C - 12.4$ **100 MHz**: $3.75 \times T_C + WS \times T_C - 10.94$	—	Note 8	—	Note 8	ns ns
20	Delay from $\overline{\text{RD}}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1]	**80 MHz**: $3.25 \times T_C + WS \times T_C - 12.4$ **100 MHz**: $3.25 \times T_C + WS \times T_C - 10.94$	—	Note 8	—	Note 8	ns ns

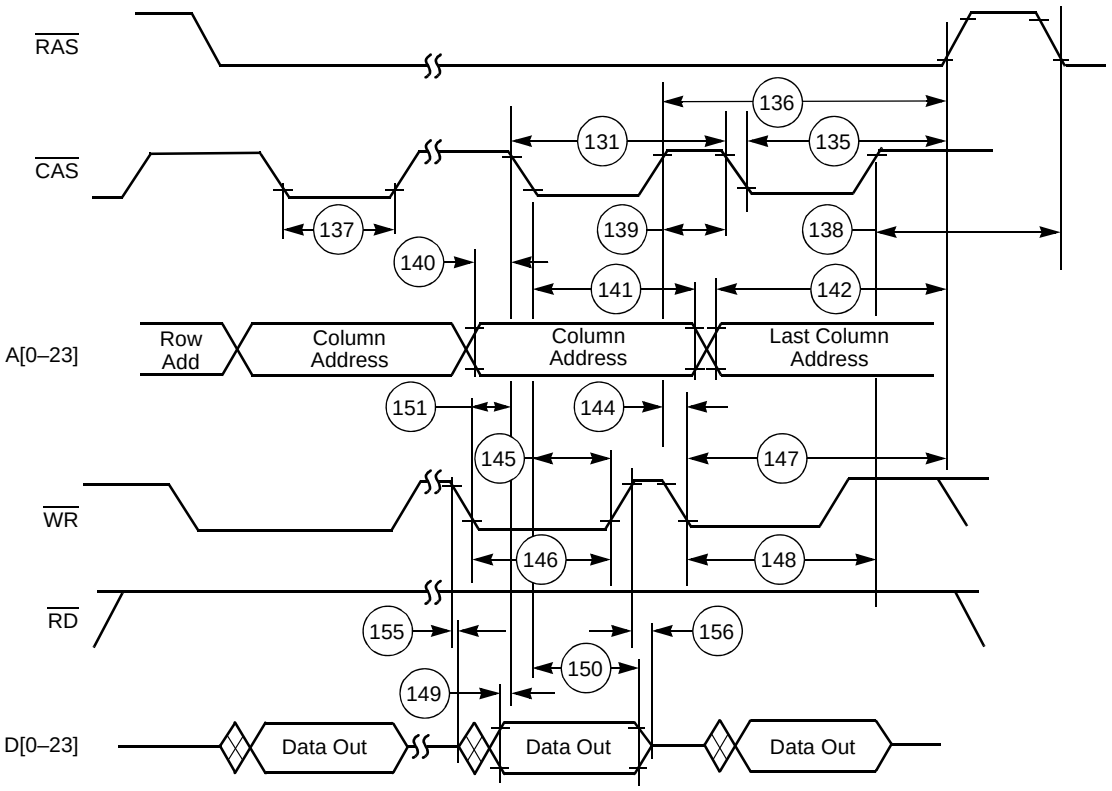


Figure 2-15. DRAM Page Mode Write Accesses

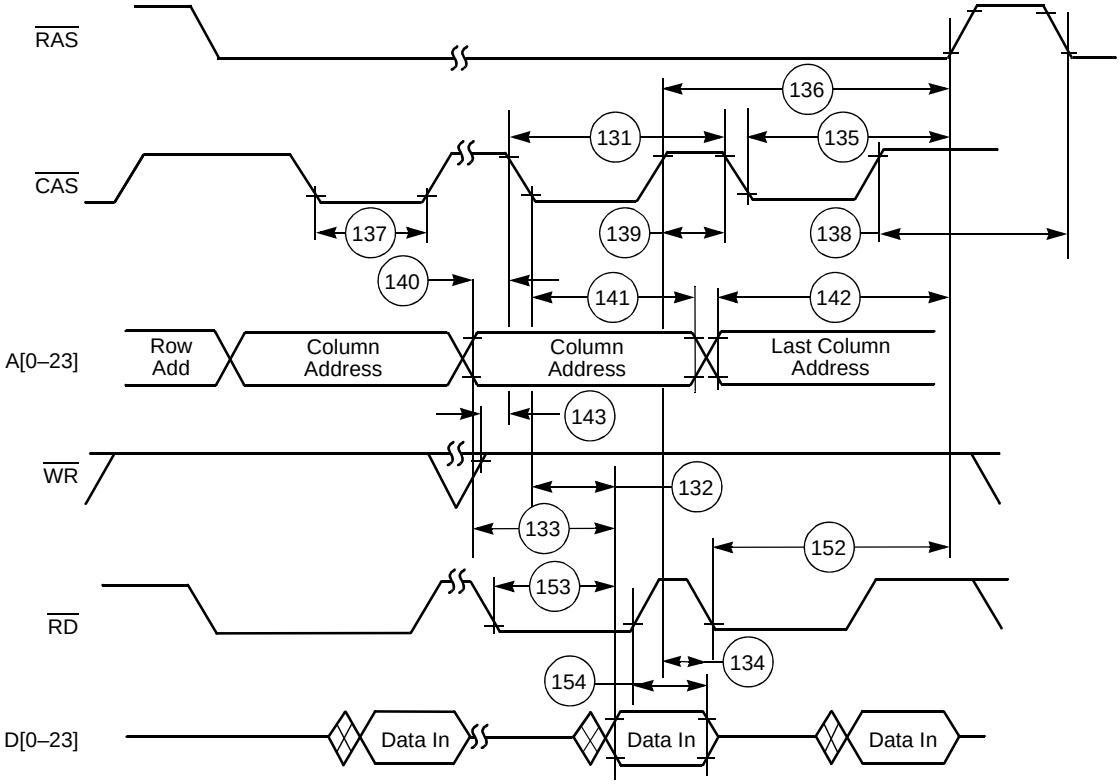


Figure 2-16. DRAM Page Mode Read Accesses

Table 2-14. DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$6.25 \times T_C - 6.0$	74.1	—	56.5	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$2.75 \times T_C - 4.0$	30.4	—	23.5	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	5.4	—	3.5	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$9.75 \times T_C - 4.0$	117.9	—	93.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$7 \times T_C - 4.0$	83.5	—	66.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$5 \times T_C - 3.8$	58.7	—	46.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RCH}	$1.75 \times T_C - 3.7$	18.2	—	13.8	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RRH}	**80 MHz**: $0.25 \times T_C - 2.6$ **100 MHz**: $0.25 \times T_C - 2.0$	0.5 —	— —	— 0.5	— —	ns ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$6 \times T_C - 4.2$	70.8	—	55.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$9.5 \times T_C - 4.2$	114.6	—	90.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$15.5 \times T_C - 4.5$	189.3	—	150.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$15.75 \times T_C - 4.3$	192.6	—	153.2	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$14.25 \times T_C - 4.3$	173.8	—	138.2	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$8.75 \times T_C - 4.0$	105.4	—	83.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$9.75 \times T_C - 4.0$	117.9	—	93.5	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$9.5 \times T_C - 4.3$	114.5	—	90.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	14.8	—	11.0	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$4.75 \times T_C - 4.0$	55.4	—	43.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$15.5 \times T_C - 4.0$	189.8	—	151.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	**80 MHz**: $14 \times T_C - 6.5$ **100 MHz**: $14 \times T_C - 5.7$	— —	168.5 —	— —	— 134.3	ns ns
193	$\overline{RD}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 1.5$	9.1	—	6.0	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for an out-of-page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. $\overline{RD}$ deassertion always occurs after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

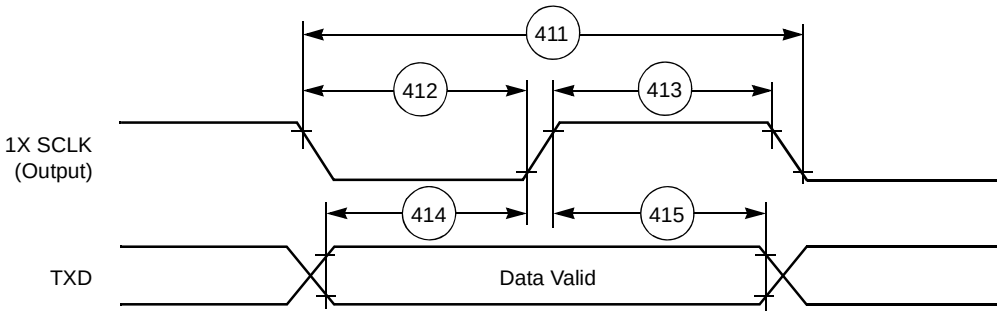


Figure 2-39. SCI Asynchronous Mode Timing

2.5.8 ESSI0/ESSI1 Timing

Table 2-22. ESSI Timings

No.	Characteristics[4, 5, 7]	Symbol	Expression	80 MHz		100 MHz		Cond-ition[6]	Unit
				Min	Max	Min	Max		
430	Clock cycle[1]	t_{SSICC}	$3 \times T_C$ $4 \times T_C$	50.0 37.5	— —	30.0 40.0	— —	x ck i ck	ns
431	Clock high period For internal clock For external clock		 $2 \times T_C - 10.0$ $1.5 \times T_C$	 15.0 18.8	 — —	 10.0 15.0	 — —		 ns ns
432	Clock low period For internal clock For external clock		 $2 \times T_C - 10.0$ $1.5 \times T_C$	 15.0 18.8	 — —	 10.0 15.0	 — —		 ns ns
433	RXC rising edge to FSR out (bl) high			— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
434	RXC rising edge to FSR out (bl) low			— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
435	RXC rising edge to FSR out (wr) high[2]			— —	39.0 24.0	— —	39.0 24.0	x ck i ck a	ns
436	RXC rising edge to FSR out (wr) low[2]			— —	39.0 24.0	— —	39.0 24.0	x ck i ck a	ns
437	RXC rising edge to FSR out (wl) high			— —	36.0 21.0	— —	36.0 21.0	x ck i ck a	ns
438	RXC rising edge to FSR out (wl) low			— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
439	Data in setup time before RXC (SCK in Synchronous mode) falling edge			10.0 19.0	— —	10.0 19.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge			5.0 3.0	— —	5.0 3.0	— —	x ck i ck	ns
441	FSR input (bl, wr) high before RXC falling edge[2]			1.0 23.0	— —	1.0 23.0	— —	x ck i ck a	ns
442	FSR input (wl) high before RXC falling edge			3.5 23.0	— —	3.5 23.0	— —	x ck i ck a	ns
443	FSR input hold time after RXC falling edge			3.0 0.0	— —	3.0 0.0	— —	x ck i ck a	ns
444	Flags input setup before RXC falling edge			5.5 19.0	— —	5.5 19.0	— —	x ck i ck s	ns

Table 3-2. DSP56301 TQFP Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	29	AA3	21	D3	72
A1	30	$\overline{BB}$	15	D4	73
A10	45	BCLK	6	D5	74
A11	46	$\overline{BCLK}$	28	D6	75
A12	47	$\overline{BG}$	16	D7	76
A13	48	$\overline{BL}$	206	D8	77
A14	51	$\overline{BR}$	17	D9	82
A15	52	$\overline{BS}$	205	$\overline{DE}$	199
A16	55	$\overline{CAS}$	7	EXTAL	26
A17	56	CLKOUT	5	GND_{P1}	14
A18	59	D0	67	GND_A	31
A19	60	D1	68	GND_A	37
A2	33	D10	83	GND_A	43
A20	61	D11	84	GND_A	49
A21	62	D12	85	GND_A	57
A22	65	D13	86	GND_A	63
A23	66	D14	87	GND_D	70
A3	34	D15	90	GND_D	80
A4	35	D16	91	GND_D	88
A5	36	D17	92	GND_D	96
A6	39	D18	93	GND_H	112
A7	40	D19	94	GND_H	123
A8	41	D2	69	GND_H	136
A9	42	D20	95	GND_H	143
AA0	1	D21	98	GND_H	155
AA1	2	D22	99	GND_H	168
AA2	20	D23	100	GND_N	4

Table 3-2. DSP56301 TQFP Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
PC2	198	SC02	198	V_{CCA}	58
PC3	192	SC10	187	V_{CCA}	64
PC4	191	SC11	186	V_{CCD}	71
PC5	195	SC12	185	V_{CCD}	81
PCAP	12	SCK0	192	V_{CCD}	89
PD0	187	SCK1	189	V_{CCD}	97
PD1	186	SCLK	178	V_{CCH}	111
PD2	185	SRD0	191	V_{CCH}	122
PD3	189	SRD1	190	V_{CCH}	135
PD4	190	STD0	195	V_{CCH}	144
PD5	188	STD1	188	V_{CCH}	156
PE0	177	$\overline{TA}$	8	V_{CCH}	169
PE1	184	TCK	201	V_{CCN}	3
PE2	178	TDI	202	V_{CCN}	18
PINIT	9	TDO	203	V_{CCP}	11
PVCL	137	TIO0	176	V_{CCQ}	25
$\overline{RAS0}$	1	TIO1	175	V_{CCQ}	79
$\overline{RAS1}$	2	TIO2	174	V_{CCQ}	131
$\overline{RAS2}$	20	TMS	200	V_{CCQ}	182
$\overline{RAS3}$	21	$\overline{TRST}$	204	V_{CCS}	179
$\overline{RD}$	23	TXD	184	V_{CCS}	193
$\overline{RESET}$	10	V_{CCA}	32	$\overline{WR}$	22
RXD	177	V_{CCA}	38	XTAL	24
SC00	196	V_{CCA}	44		
SC01	197	V_{CCA}	50		

Note: NC stands for Not Connected. These pins are reserved for future development. Do not connect any line, component, or trace to these pins.

- If the temperature of the package case (T_T) is determined by a thermocouple, thermal resistance is computed from the value obtained by the equation $(T_J - T_T)/P_D$.

As noted earlier, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable to determine the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, the use of the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will yield an estimate of a junction temperature slightly higher than actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when the surface temperature of the package is used. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

4.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

Use the following list of recommendations to ensure correct DSP operation.

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP and from the board ground to each GND pin.
- Use at least six 0.01–0.1 µF bypass capacitors positioned as close as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer PCB with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{TA}}$, and $\overline{\text{BG}}$ pins. Maximum PCB trace lengths on the order of 6 inches are recommended.
- Consider all device loads as well as parasitic capacitance due to PCB traces when you calculate capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (that is, not allowed to float) by CMOS levels except for the three pins with internal pull-up resistors ($\overline{\text{TRST}}$, TMS, $\overline{\text{DE}}$).
- Take special care to minimize noise levels on the V_{CCP}, GND_P, and GND_{P1} pins.
- The following pins must be asserted after power-up: $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$.

- If multiple DSP devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.
- $\overline{\text{RESET}}$ must be asserted when the chip is powered up. A stable EXTAL signal should be supplied before deassertion of $\overline{\text{RESET}}$.
- At power-up, ensure that the voltage difference between the 5 V tolerant pins and the chip V_{CC} never exceeds 3.5 V.

4.3 Power Consumption Considerations

Power dissipation is a key issue in portable DSP applications. Some of the factors affecting current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by this formula:

Equation 3: $$I = C \times V \times f$$

Where:

C	=	node/pin capacitance
V	=	voltage swing
f	=	frequency of node/pin toggle

Example 1. Current Consumption

For a Port A address pin loaded with 50 pF capacitance, operating at 3.3 V, with a 66 MHz clock, toggling at its maximum possible rate (33 MHz), the current consumption is expressed in **Equation 4**.

Equation 4: $$I = 50 \times 10^{-12} \times 3.3 \times 33 \times 10^{6} = 5.48\ mA$$

The maximum internal current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions—not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions. Perform the following steps for applications that require very low current consumption:

1. Set the EBD bit when you are not accessing external memory.
2. Minimize external memory accesses, and use internal memory accesses.
3. Minimize the number of pins that are switching.
4. Minimize the capacitive load on the pins.
5. Connect the unused inputs to pull-up or pull-down resistors.
6. Disable unused peripherals.
7. Disable unused pin activity (for example, CLKOUT, XTAL).

One way to evaluate power consumption is to use a current-per-MIPS measurement methodology to minimize specific board effects (that is, to compensate for measured board current not caused by the DSP). A benchmark power consumption test algorithm is listed in **Appendix A**. Use the test algorithm, specific test current measurements, and the following equation to derive the current-per-MIPS value.

Equation 5: $I/\text{MIPS} = I/\text{MHz} = (I_{typF2} - I_{typF1})/(F2 - F1)$

Where:

I_{typF2}	=	current at F2
I_{typF1}	=	current at F1
F2	=	high frequency (any specified operating frequency)
F1	=	low frequency (any specified operating frequency lower than F2)

Note: F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

4.4 PLL Performance Issues

The following explanations should be considered as general observations on expected PLL behavior. There is no test that replicates these exact numbers. These observations were measured on a limited number of parts and were not verified over the entire temperature and voltage ranges.

4.4.1 Phase Skew Performance

The phase skew of the PLL is defined as the time difference between the falling edges of EXTAL and CLKOUT for a given capacitive load on CLKOUT, over the entire process, temperature and voltage ranges. As defined in **Figure 2-2**, *External Clock Timing*, on page -5 for input frequencies greater than 15 MHz and the MF ≤ 4, this skew is greater than or equal to 0.0 ns and less than 1.8 ns; otherwise, this skew is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this skew is between −1.4 ns and +3.2 ns.

4.4.2 Phase Jitter Performance

The phase jitter of the PLL is defined as the variations in the skew between the falling edges of EXTAL and CLKOUT for a given device in specific temperature, voltage, input frequency, MF, and capacitive load on CLKOUT. These variations are a result of the PLL locking mechanism. For input frequencies greater than 15 MHz and MF ≤ 4, this jitter is less than ±0.6 ns; otherwise, this jitter is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this jitter is less than ±2 ns.

4.4.3 Frequency Jitter Performance

The frequency jitter of the PLL is defined as the variation of the frequency of CLKOUT. For small MF (MF < 10) this jitter is smaller than 0.5 per cent. For mid-range MF (10 < MF < 500) this jitter is between 0.5 per cent and approximately 2 per cent. For large MF (MF > 500), the frequency jitter is 2–3 per cent.

4.5 Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5 percent. If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time), then the allowed jitter can be 2 percent. The phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed values.

```
        do      #(XDAT_END-XDAT_START),XLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,x:(r0)+
XLOAD_LOOP
;
;Load the Y-data
;
        move    #INT_YDAT,r0
        move    #YDAT_START,r1
        do      #(YDAT_END-YDAT_START),YLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,y:(r0)+
YLOAD_LOOP
;

        jmp     INT_PROG

PROG_START
        move    #$0,r0
        move    #$0,r4
        move    #$3f,m0
        move    #$3f,m4
;
        clr     a
        clr     b
        move    #$0,x0
        move    #$0,x1
        move    #$0,y0
        move    #$0,y1
        bset    #4,omr          ; ebd
;
sbr     dor     #60,_end
        mac     x0,y0,ax:(r0)+,x1     y:(r4)+,y1
        mac     x1,y1,ax:(r0)+,x0     y:(r4)+,y0
        add     a,b
        mac     x0,y0,ax:(r0)+,x1
        mac     x1,y1,a               y:(r4)+,y0
        move    b1,x:$ff
_end
        bra     sbr
        nop
        nop
        nop
        nop
PROG_END
        nop
        nop


XDAT_START
;       org     x:0
        dc      $262EB9
        dc      $86F2FE
        dc      $E56A5F
        dc      $616CAC
        dc      $8FFD75
        dc      $9210A
        dc      $A06D7B
        dc      $CEA798
        dc      $8DFBF1
        dc      $A063D6
```

```
M_DSR EQU $FFFFC9; DSP STATUS REGISTER (DSR)
M_DPAR EQU $FFFFC8; DSP PCI ADDRESS REGISTER (DPAR)
M_DPMC EQU $FFFFC7; DSP PCI MASTER CONTROL REGISTER (DPMC)
M_DPCR EQU $FFFFC6; DSP PCI CONTROL REGISTER (DPCR)
M_DCTR EQU $FFFFC5 ; DSP CONTROL REGISTER (DCTR)

;       Host Control Register Bit Flags

M_HCIE EQU 0   ; Host Command Interrupt Enable
M_STIE EQU 1   ; Slave Transmit Interrupt Enable
M_SRIE EQU 2   ; Slave Receive Interrupt Enable
M_HF35 EQU $38 ; Host Flags 5-3 Mask
M_HF3 EQU 3    ; Host Flag 3
M_HF4 EQU 4    ; Host Flag 4
M_HF5 EQU 5    ; Host Flag 5
M_HINT EQU 6   ; Host Interrupt A
M_HDSM EQU 13  ; Host Data Strobe Mode
M_HRWP EQU 14  ; Host RD/WR Polarity
M_HTAP EQU 15  ; Host Transfer Acknowledge Polarity
M_HDRP EQU 16  ; Host Dma Request Polarity
M_HRSP EQU 17  ; Host Reset Polarity
M_HIRP EQU 18  ; Host Interrupt  Request Polarity
M_HIRC EQU 19  ; Host Interupt Request Control
M_HM0 EQU 20   ; Host Interface Mode
M_HM1 EQU 21   ; Host Interface Mode
M_HM2 EQU 22   ; Host Interface Mode
M_HM EQU $700000 ; Host Interface Mode Mask

;       Host PCI Control Register Bit Flags

M_PMTIE EQU 1  ; PCI Master Transmit Interrupt Enable
M_PMRIE EQU 2  ; PCI Master Receive Interrupt Enable
M_PMAIE EQU 4  ; PCI Master Address Interrupt Enable
M_PPEIE EQU 5  ; PCI Parity Error Interrupt Enable
M_PTAIE EQU 7  ; PCI Transaction Abort Interrupt Enable
M_PTTIE EQU 9  ; PCI Transaction Termination Interrupt Enable
M_PTCIE EQU 12    ; PCI Transfer Complete Interrupt Enable
M_CLRT EQU 14  ; Clear Transmitter
M_MTT EQU 15   ; Master Transfer Terminate
M_SERF EQU 16  ; HSERR~ Force
M_MACE EQU 18  ; Master Access Counter Enable
M_MWSD EQU 19  ; Master Wait States Disable
M_RBLE EQU 20  ; Receive Buffer Lock Enable
M_IAE EQU 21   ; Insert Address Enable

;       Host PCI Master Control Register Bit Flags

M_ARH EQU $00ffff; DSP PCI Transaction Address (High)
M_BL EQU $3f0000; PCI Data Burst Length
M_FC EQU $c00000; Data Transfer Format Control

;       Host PCI Address Register Bit Flags

M_ARL EQU $00ffff; DSP PCI Transaction Address (Low)
M_C EQU $0f0000; PCI Bus Command
M_BE EQU $f00000; PCI Byte Enables

;       DSP Status Register Bit Flags

M_HCP EQU 0    ; Host Command pending
```

```
M_SCRE EQU 8      ; SCI Receiver Enable
M_SCTE EQU 9      ; SCI Transmitter Enable
M_ILIE EQU 10     ; Idle Line Interrupt Enable
M_SCRIE EQU 11     ; SCI Receive Interrupt Enable
M_SCTIE EQU 12     ; SCI Transmit Interrupt Enable
M_TMIE EQU 13     ; Timer Interrupt Enable
M_TIR EQU 14     ; Timer Interrupt Rate
M_SCKP EQU 15     ; SCI Clock Polarity
M_REIE EQU 16     ; SCI Error Interrupt Enable (REIE)

;       SCI Status Register Bit Flags

M_TRNE EQU 0      ; Transmitter Empty
M_TDRE EQU 1      ; Transmit Data Register Empty
M_RDRF EQU 2      ; Receive Data Register Full
M_IDLE EQU 3      ; Idle Line Flag
M_OR EQU 4      ; Overrun Error Flag
M_PE EQU 5      ; Parity Error
M_FE EQU 6      ; Framing Error Flag
M_R8 EQU 7      ; Received Bit 8 (R8) Address

;       SCI Clock Control Register

M_CD EQU $FFF   ; Clock Divider Mask (CD0-CD11)
M_COD EQU 12     ; Clock Out Divider
M_SCP EQU 13     ; Clock Prescaler
M_RCM EQU 14     ; Receive Clock Mode Source Bit
M_TCM EQU 15     ; Transmit Clock Source Bit

;------------------------------------------------------------------------
;
;      EQUATES for Synchronous Serial Interface (SSI)
;
;------------------------------------------------------------------------

;
;       Register Addresses Of SSI0
M_TX00 EQU $FFFFBC; SSI0 Transmit Data Register 0
M_TX01 EQU $FFFFBB; SSIO Transmit Data Register 1
M_TX02 EQU $FFFFBA; SSIO Transmit Data Register 2
M_TSR0 EQU $FFFFB9; SSI0 Time Slot Register
M_RX0 EQU $FFFFB8; SSI0 Receive Data Register
M_SSISR0 EQU $FFFFB7; SSI0 Status Register
M_CRB0 EQU $FFFFB6; SSI0 Control Register B
M_CRA0 EQU $FFFFB5; SSI0 Control Register A
M_TSMA0 EQU $FFFFB4; SSI0 Transmit Slot Mask Register A
M_TSMB0 EQU $FFFFB3; SSI0 Transmit Slot Mask Register B
M_RSMA0 EQU $FFFFB2; SSI0 Receive Slot Mask Register A
M_RSMB0 EQU $FFFFB1; SSI0 Receive Slot Mask Register B

;       Register Addresses Of SSI1
M_TX10 EQU $FFFFAC; SSI1 Transmit Data Register 0
M_TX11 EQU $FFFFAB; SSI1 Transmit Data Register 1
M_TX12 EQU $FFFFAA; SSI1 Transmit Data Register 2
M_TSR1 EQU $FFFFA9; SSI1 Time Slot Register
M_RX1 EQU $FFFFA8; SSI1 Receive Data Register
M_SSISR1 EQU $FFFFA7; SSI1 Status Register
M_CRB1 EQU $FFFFA6; SSI1 Control Register B
M_CRA1 EQU $FFFFA5; SSI1 Control Register A
M_TSMA1 EQU $FFFFA4; SSI1 Transmit Slot Mask Register A
```

```
M_TC EQU $F0    ; Timer Control Mask (TC0-TC3)
M_INV EQU 8      ; Inverter Bit
M_TRM EQU 9      ; Timer Restart Mode
M_DIR EQU 11     ; Direction Bit
M_DI EQU 12     ; Data Input
M_DO EQU 13     ; Data Output
M_PCE EQU 15   ; Prescaled Clock Enable
M_TOF EQU 20     ; Timer Overflow Flag
M_TCF EQU 21     ; Timer Compare Flag

;       Timer Prescaler Register Bit Flags

M_PS EQU $600000  ; Prescaler Source Mask
M_PS0 EQU 21
M_PS1 EQU 22

;      Timer Control Bits
M_TC0 EQU 4      ; Timer Control 0
M_TC1 EQU 5      ; Timer Control 1
M_TC2 EQU 6      ; Timer Control 2
M_TC3 EQU 7      ; Timer Control 3


;---------------------------------------------------------------------------
;
;       EQUATES for Direct Memory Access (DMA)
;
;---------------------------------------------------------------------------

;       Register Addresses Of DMA
M_DSTR EQU $FFFFF4; DMA Status Register
M_DOR0 EQU $FFFFF3; DMA Offset Register 0
M_DOR1 EQU $FFFFF2; DMA Offset Register 1
M_DOR2 EQU $FFFFF1; DMA Offset Register 2
M_DOR3 EQU $FFFFF0; DMA Offset Register 3


;       Register Addresses Of DMA0

M_DSR0 EQU $FFFFEF; DMA0 Source Address Register
M_DDR0 EQU $FFFFEE; DMA0 Destination Address Register
M_DCO0 EQU $FFFFED; DMA0 Counter
M_DCR0 EQU $FFFFEC; DMA0 Control Register

;       Register Addresses Of DMA1

M_DSR1 EQU $FFFFEB; DMA1 Source Address Register
M_DDR1 EQU $FFFFEA; DMA1 Destination Address Register
M_DCO1 EQU $FFFFE9; DMA1 Counter
M_DCR1 EQU $FFFFE8; DMA1 Control Register

;       Register Addresses Of DMA2

M_DSR2 EQU $FFFFE7; DMA2 Source Address Register
M_DDR2 EQU $FFFFE6; DMA2 Destination Address Register
M_DCO2 EQU $FFFFE5; DMA2 Counter
M_DCR2 EQU $FFFFE4; DMA2 Control Register

;       Register Addresses Of DMA4
```

```
M_WRP EQU 19      ; Extended WRaP flag in OMR.
M_SEN EQU 20      ; Stack Extension Enable bit in OMR.
;*************************************************************************
;
;     EQUATES for DSP56301 interrupts
;     Reference: DSP56301 Specifications Revision 3.00
;
;     Last update: November 15 1993 (Debug request & HI32 interrupts)
;                  December 19 1993 (cosmetic - page and opt directives)
;              August 16 1994 (change interrupt addresses to be
;                      relative to I_VEC)
;
;*************************************************************************

       page   132,55,0,0,0
       opt    mex

intequ  ident   1,0

       if     @DEF(I_VEC)
       ;leave user definition as is.
       else
I_VEC  equ    $0
       endif

;------------------------------------------------------------------------
; Non-Maskable interrupts
;------------------------------------------------------------------------
I_RESET  EQU  I_VEC+$00   ; Hardware RESET
I_STACK  EQU  I_VEC+$02   ; Stack Error
I_ILL    EQU  I_VEC+$04   ; Illegal Instruction
I_DBG    EQU  I_VEC+$06   ; Debug Request
I_TRAP   EQU  I_VEC+$08   ; Trap
I_NMI    EQU  I_VEC+$0A   ; Non Maskable Interrupt

;------------------------------------------------------------------------
; Interrupt Request Pins
;------------------------------------------------------------------------
I_IRQA   EQU  I_VEC+$10   ; IRQA
I_IRQB   EQU  I_VEC+$12   ; IRQB
I_IRQC   EQU  I_VEC+$14   ; IRQC
I_IRQD   EQU  I_VEC+$16   ; IRQD

;------------------------------------------------------------------------
; DMA Interrupts
;------------------------------------------------------------------------
I_DMA0   EQU  I_VEC+$18   ; DMA Channel 0
I_DMA1   EQU  I_VEC+$1A   ; DMA Channel 1
I_DMA2   EQU  I_VEC+$1C   ; DMA Channel 2
I_DMA3   EQU  I_VEC+$1E   ; DMA Channel 3
I_DMA4   EQU  I_VEC+$20   ; DMA Channel 4
I_DMA5   EQU  I_VEC+$22   ; DMA Channel 5



;------------------------------------------------------------------------
; Timer Interrupts
;------------------------------------------------------------------------
I_TIM0C  EQU  I_VEC+$24   ; TIMER 0 compare
I_TIM0OF EQU  I_VEC+$26   ; TIMER 0 overflow
```

Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Supply Voltage	Package Type	Pin Count	Core Frequency (MHz)	Solder Spheres	Order Number
DSP56301	3.3 V	Thin Quad Flat Pack (TQFP)	208	80	Lead-free	DSP56301AG80
					Lead-bearing	DSP56301PW80
				100	Lead-free	DSP56301AG100
					Lead-bearing	DSP56301PW100
		Molded Array Process-Ball Grid Array (MAP-BGA)	252	80	Lead-free	DSP56301VL80
					Lead-bearing	DSP56301VF80
				100	Lead-free	DSP56301VL100
					Lead-bearing	DSP56301VF100

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Document Order No.: DSP56301
Rev. 10
7/2006