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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	80MHz
Non-Volatile Memory	ROM (9kB)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-TQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56301pw80

Table 2-10. DRAM Page Mode Timings, Three Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction		$4 \times T_C$	50.0	—	40.0	—	ns
	Page mode cycle time for mixed (read and write) accesses	t_{PC}	$3.5 \times T_C$	43.7	—	35.0	—	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$2 \times T_C - 5.7$	—	19.3	—	14.3	ns
133	Column address valid to data valid (read)	t_{AA}	$3 \times T_C - 5.7$	—	31.8	—	24.3	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$2.5 \times T_C - 4.0$	27.3	—	21.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$4.5 \times T_C - 4.0$	52.3	—	41.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2 \times T_C - 4.0$	21.0	—	16.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion[5] • BRW[1–0] = 00 • BRW[1–0] = 01 • BRW[1–0] = 10 • BRW[1–0] = 11	t_{CRP}	 Not supported $3.75 \times T_C - 6.0$ $4.75 \times T_C - 6.0$ $6.75 \times T_C - 6.0$	 — 40.9 53.4 78.4	 — — — —	 — 31.5 41.5 61.5	 — — — —	 ns ns ns ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.5 \times T_C - 4.0$	14.8	—	11.0	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	8.5	—	6.0	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$2.5 \times T_C - 4.0$	27.3	—	21.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	46.0	—	36.0	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 4.0$	11.6	—	8.5	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.75 \times TC - 4.0$	5.4	—	3.5	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$2.25 \times T_C - 4.2$	23.9	—	18.3	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$3.5 \times T_C - 4.5$	39.3	—	30.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$3.75 \times T_C - 4.3$	42.6	—	33.2	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.25 \times T_C - 4.3$	36.3	—	28.2	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.8$	2.0	—	0.2	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$2.5 \times T_C - 4.0$	27.3	—	21.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	11.3	—	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$3.5 \times T_C - 4.0$	39.8	—	31.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$2.5 \times T_C - 5.7$	—	25.6	—	19.3	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 1.5$	7.9	—	6.0	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for Page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56301.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (for example, t_{PC} equals $4 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1–0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of page-access.
6. $\overline{RD}$ deassertion always occurs after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

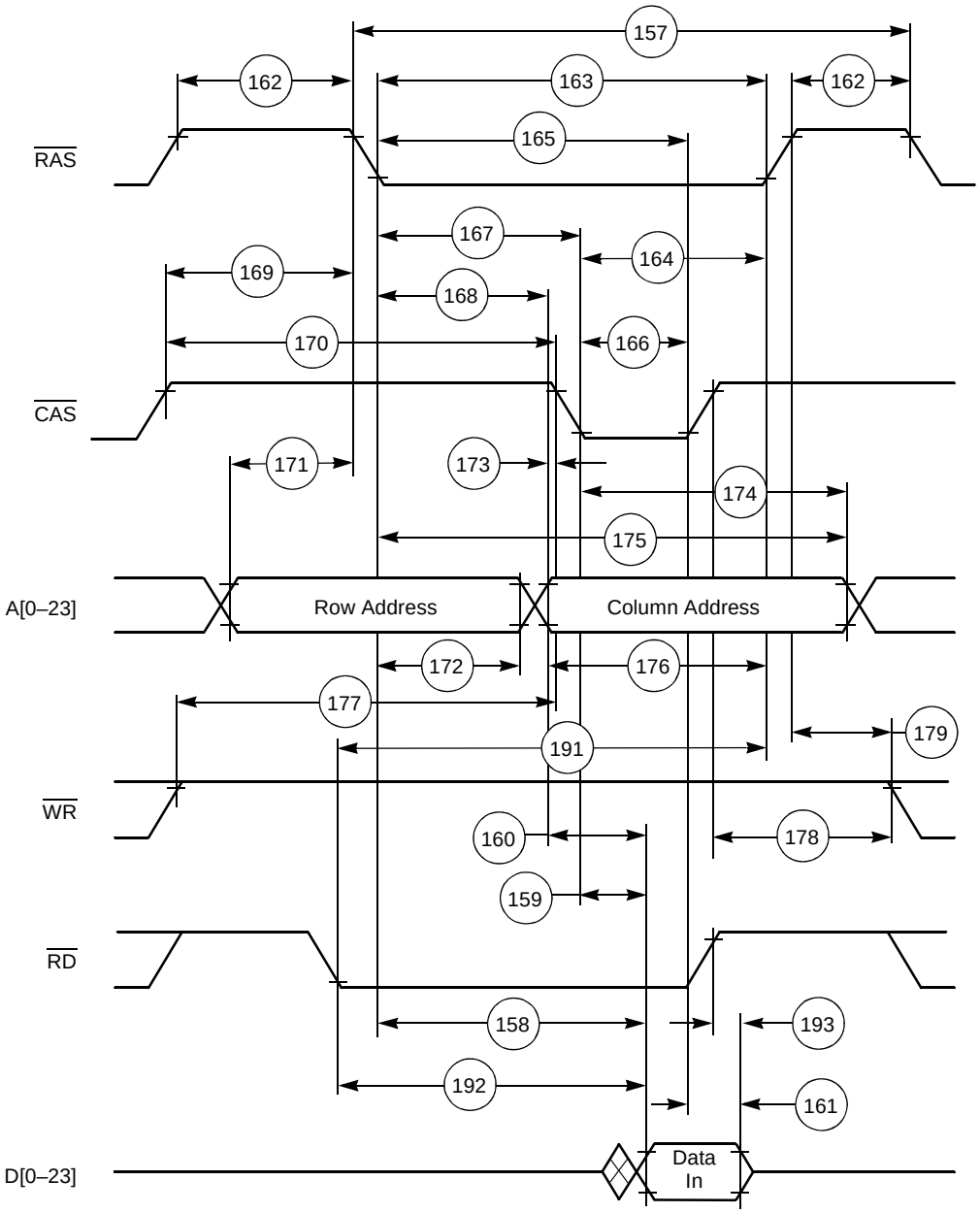
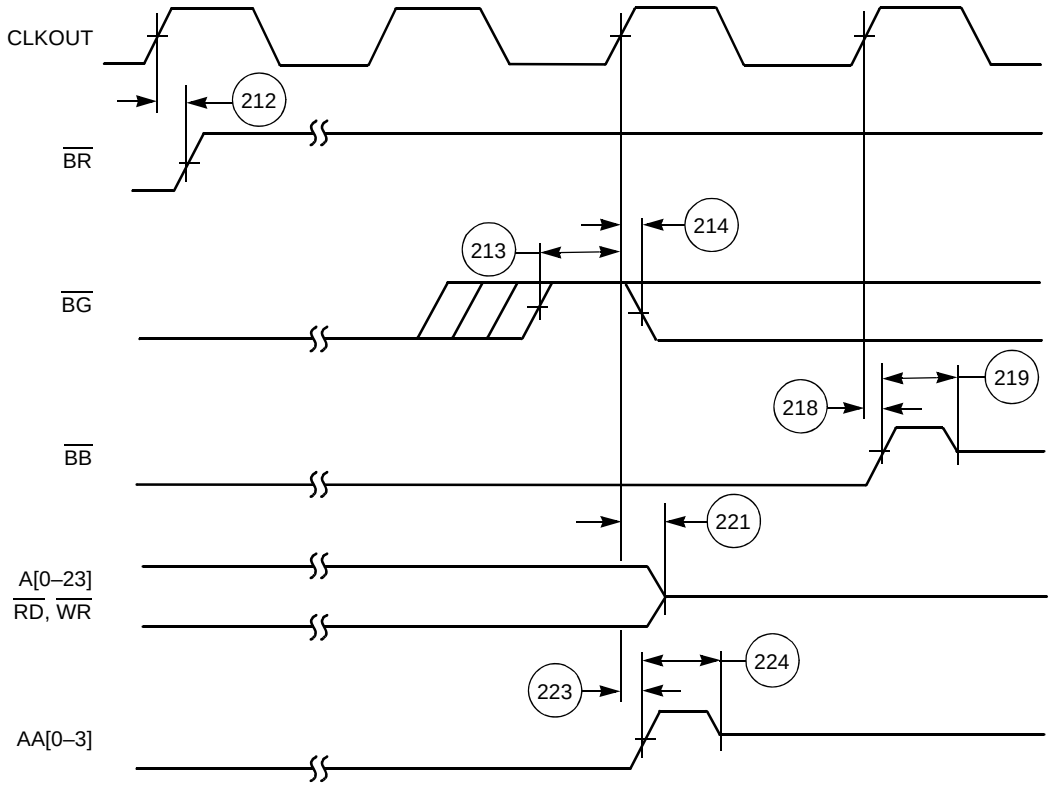


Figure 2-18. DRAM Out-of-Page Read Access



Note: Address lines A[0–23] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-25. Bus Release Timings Case 2 (BRT Bit in Operating Mode Register Set)

2.5.5.5 Asynchronous Bus Arbitrations Timings

Table 2-17. Asynchronous Bus Arbitration Timing[1,3]

No.	Characteristics	Expression	80 MHz		100 MHz[2]		Unit
			Min	Max	Min	Max	
250	$\overline{BB}$ assertion window from $\overline{BG}$ input deassertion[4]	2.5 × Tc + 5	—	25	—	30	ns
251	Delay from $\overline{BB}$ assertion to $\overline{BG}$ assertion[4]	2 × Tc + 5	25	—	25	—	ns

Notes:
1. Bit 13 in the Operating Mode Register must be set to enter Asynchronous Arbitration mode.
2. Asynchronous Arbitration mode is recommended for operation at 100 MHz.
3. If Asynchronous Arbitration mode is active, none of the timings in **Table 2-16** is required.
4. In order to guarantee timings 250, and 251, $\overline{BG}$ inputs must be asserted to different DSP56300 devices on the same bus in the non-overlap manner shown in **Figure 2-26**.

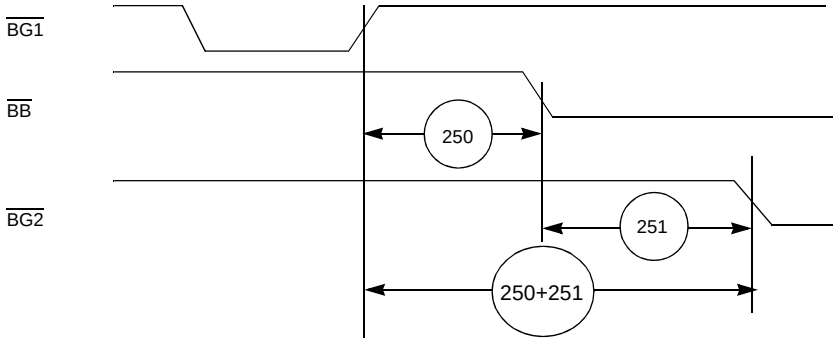


Figure 2-26. Asynchronous Bus Arbitration Timing

The asynchronous bus arbitration is enabled by internal $\overline{BB}$ inputs and synchronization circuits on $\overline{BG}$. These synchronization circuits add delay from the external signal until it is exposed to internal logic. As a result of this delay, a DSP56300 part can assume mastership and assert $\overline{BB}$, for some time after $\overline{BG}$ is deasserted. Timing 250 defines when $\overline{BB}$ can be asserted.

Once $\overline{BB}$ is asserted, there is a synchronization delay from $\overline{BB}$ assertion to the time this assertion is exposed to other DSP56300 components which are potential masters on the same bus. If $\overline{BG}$ input is asserted before that time, a situation of $\overline{BG}$ asserted, and $\overline{BB}$ deasserted, can cause another DSP56300 component to assume mastership at the same time. Therefore, a non-overlap period between one $\overline{BG}$ input active to another $\overline{BG}$ input active is required. Timing 251 ensures that such a situation is avoided.

2.5.6 Host Interface Timing

Table 2-18. Universal Bus Mode Timing Parameters

No.	Characteristic	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
300	Access Cycle Time	$3 \times T_C$	37.5	—	30.0	—	ns
301	HA[10–0], HAEN Setup to Data Strobe Assertion[1]		5.8	—	4.6	—	ns
302	HA[10–0], HAEN Valid Hold from Data Strobe Deassertion[1]		0.0	—	0.0	—	ns
303	HRW Setup to $\overline{HDS}$ Assertion[2]		5.8	—	4.6	—	ns
304	HRW Valid Hold from $\overline{HDS}$ Deassertion[2]		0.0	—	0.0	—	ns
305	Data Strobe Deasserted Width[1]		4.1	—	3.3	—	ns
306	Data Strobe Asserted Pulse Width[1]	**80 MHz:** $2.5 \times T_C + 1.7$ **100 MHz:** $2.5 \times T_C + 1.3$	32.9	—	 26.3	 —	ns ns
307	$\overline{HBS}$ Asserted Pulse Width		2.5	—	2.0	—	ns
308	$\overline{HBS}$ Assertion to Data Strobe Assertion[1]	**80 MHz:** $T_C - 4.9$ **100 MHz:** $T_C - 4.0$	— 	7.6 	 —	 6.0	ns ns
309	$\overline{HBS}$ Assertion to Data Strobe Deassertion[1]	**80 MHz:** $2.5 \times T_C + 2.9$ **100 MHz:** $2.5 \times T_C + 2.3$	34.1	—	 27.3	 —	ns ns
310	$\overline{HBS}$ Deassertion to Data Strobe Deassertion[1]	**80 MHz:** $1.5 \times T_C + 3.3$ **100 MHz:** $1.5 \times T_C + 2.6$	22.1	—	 17.6	 —	ns ns
311	Data Out Valid to TA Assertion ($\overline{HBS}$ Not Used—Tied to V_{CC})[2]	**80 MHz:** $2 \times T_C - 11.6$ **100 MHz:** $2 \times T_C - 9.2$	13.4	—	 10.8	 —	ns ns
312	Data Out Active from Read Data Strobe Assertion[3]		1.7	—	1.3	—	ns

Table 2-18. Universal Bus Mode Timing Parameters (Continued)

No.	Characteristic	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
313	Data Out Valid from Read Data Strobe Assertion (No Wait States Inserted—$\overline{\text{HTA}}$ Asserted)[3]		—	18.9	—	16.9	ns
314	Data Out Valid Hold from Read Data Strobe Deassertion$_3$		1.7	—	1.3	—	ns
315	Data Out High Impedance from Read Data Strobe Deassertion[3]		—	12.0	—	9.6	ns
316	Data In Valid Setup to Write Data Strobe Deassertion[4]		8.3	—	6.6	—	ns
317	Data In Valid Hold from Write Data Strobe Deassertion[4]		0.0	—	0.0	—	ns
318	$\overline{\text{HSAK}}$ Assertion from Data Strobe Assertion[1]		—	30.0	—	30.0	ns
319	$\overline{\text{HSAK}}$ Asserted Hold from Data Strobe Deassertion[1]		2.0	—	2.0	—	ns
320	$\overline{\text{HTA}}$ Active from Data Strobe Assertion[1,2,5]		3.1	—	2.5	—	ns
321	$\overline{\text{HTA}}$ Assertion from Data Strobe Assertion ($\overline{\text{HBS}}$ Not Used—Tied to V_{CC})[1,2,5]	**80 MHz:** $2.0 \times T_C + 13.0$ **100 MHz:** $2.0 \times T_C + 12.2$	38.0	—	 32.2	 —	ns ns
322	$\overline{\text{HTA}}$ Assertion from $\overline{\text{HBS}}$ Assertion[2,5]	**80 MHz:** $2.0 \times T_C + 13.0$ **100 MHz:** $2.0 \times T_C + 12.2$	38.0	—	 32.2	 —	ns ns
323	$\overline{\text{HTA}}$ Deasserted from Data Strobe Assertion[1,2,5]		—	17.1	—	15.0	ns
324	$\overline{\text{HTA}}$ Assertion to Data Strobe Deassertion[1,2]		0.0	—	0.0	—	ns
325	$\overline{\text{HTA}}$ High Impedance from Data Strobe Deassertion[1,2]		—	15.3	—	12.2	ns
326	$\overline{\text{HIRQ}}$ Asserted Pulse Width (HIRH = 0, HIRD = 1)	$(LT + 1) \times T_C - 6.0$[7]	19.0	—	14.0	—	ns
327	Data Strobe Deasserted Hold from $\overline{\text{HIRQ}}$ Deassertion (HIRH = 0)[1]		0.0	—	0.0	—	ns
328	$\overline{\text{HIRQ}}$ Asserted Hold from Data Strobe Assertion (HIRH = 1)[1]	$1.5 \times T_C$	18.8	—	15.0	—	ns
329	$\overline{\text{HIRQ}}$ Deassertion from Data Strobe Assertion (HIRH = 1, HIRD = 1)[1]	**80 MHz:** $2.5 \times T_C + 24.7$ 100 MHz: $2.5 \times T_C + 21.5$	—	55.9	 —	 46.5	ns ns
330	$\overline{\text{HIRQ}}$ High Impedance from Data Strobe Assertion (HIRH = 1, HIRD = 0)[1,6]	**80 MHz:** $2.5 \times T_C + 24.7$ **100 MHz:** $2.5 \times T_C + 21.5$	—	55.9	 —	 46.5	ns ns
331	$\overline{\text{HIRQ}}$ Active from Data Strobe Deassertion (HIRH = 1, HIRD = 0)[1]	$2.5 \times T_C$	31.3	—	25.0	—	ns
332	$\overline{\text{HIRQ}}$ Deasserted Hold from Data Strobe Deassertion[1]	$2.5 \times T_C$	31.3	—	25.0	—	ns
333	HDRQ[2] Asserted Hold from Data Strobe Assertion[1]	$1.5 \times T_C$	18.8	—	15.0	—	ns
334	HDRQ[2] Deassertion from Data Strobe Assertion[1]	**80 MHz:** $2.5 \times T_C + 24.7$ **100 MHz:** $2.5 \times T_C + 21.5$	—	55.9	 —	 46.5	ns ns
335	HDRQ[2] Deasserted Hold from Data Strobe Deassertion[1]	**80 MHz:** $2.5 \times T_C + 3.7$ **100 MHz:** $2.5 \times T_C + 3.0$	35.0	—	 28.0	 —	ns ns
336	$\overline{\text{HDAK}}$ Assertion to Data Strobe Assertion[1]		5.8	—	4.6	—	ns
337	$\overline{\text{HDAK}}$ Asserted Hold from Data Strobe Deassertion[1]		0.0	—	0.0	—	ns
338	$\overline{\text{HDBEN}}$ Deasserted Hold from Data Strobe Assertion[1]		2.5	—	2.0	—	ns
339	$\overline{\text{HDBEN}}$ Assertion from Data Strobe Assertion[1]		—	22.2	—	19.6	ns
340	$\overline{\text{HDBEN}}$ Asserted Hold from Data Strobe Deassertion[1]		2.5	—	2.0	—	ns
341	$\overline{\text{HDBEN}}$ Deassertion from Data Strobe Deassertion[1]		—	22.2	—	19.6	ns
342	HDBDR High Hold from Read Data Strobe Assertion[3]		2.5	—	2.0	—	ns
343	HDBDR Low from Read Data Strobe Assertion[3]		—	22.2	—	19.6	ns
344	HDBDR Low Hold from Read Data Strobe Deassertion[3]		2.5	—	2.0	—	ns

Table 2-19. Universal Bus Mode, Synchronous Port A Type Host Timing (Continued)

No.	Characteristic	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
330	$\overline{\text{HIRQ}}$ High Impedance from Data Strobe Assertion (HIRH = 1, HIRD = 0)[1,6]	**80 MHz:** $2.5 \times T_C + 24.7$ **100 MHz:** $2.5 \times T_C + 21.5$	—	55.9	— —	46.5	ns ns
331	$\overline{\text{HIRQ}}$ Active from Data Strobe Deassertion (HIRH = 1, HIRD = 0)[1]	$2.5 \times T_C$	31.3	—	25.0	—	ns
332	$\overline{\text{HIRQ}}$ Deasserted Hold from Data Strobe Deassertion[1]	$2.5 \times T_C$	31.3	—	25.0	—	ns
346	HRST Assertion to Host Port Pins High Impedance[2]		—	22.2	—	19.6	ns
347	$\overline{\text{HBS}}$ Assertion to CLKOUT Rising Edge		4.3	—	3.4	—	ns
348	Data Strobe Deassertion to CLKOUT Rising Edge[1]		7.4	—	5.9	—	ns

Notes:
1. The Data Strobe is $\overline{\text{HRD}}$ or $\overline{\text{HWR}}$ in the Dual Data Strobe mode and $\overline{\text{HDS}}$ in the Single Data Strobe mode.
2. $\overline{\text{HTA}}$, HDRQ, and HRST may be programmed as active-high or active-low. In the example timing diagrams, HDRQ and HRST are shown as active-high and $\overline{\text{HTA}}$ is shown as active low.
3. The Read Data Strobe is $\overline{\text{HRD}}$ in the Dual Data Strobe mode and $\overline{\text{HDS}}$ in the Single Data Strobe mode.
4. The Write Data Strobe is $\overline{\text{HWR}}$ in the Dual Data Strobe mode and $\overline{\text{HDS}}$ in the Single Data Strobe mode.
5. $\overline{\text{HTA}}$ requires an external pull-down resistor if programmed as active high (HTAP = 0); or an external pull-up resistor if programmed as active low (HTAP = 1). The resistor value should be consistent with the DC specifications.
6. $\overline{\text{HIRQ}}$ requires an external pull-up resistor if programmed as open drain (HIRD = 0). The resistor value should be consistent with the DC specifications.
7. "LT" is the value of the latency timer register (CLAT) as programmed by the user during self configuration.
8. Values are valid for $V_{CC} = 3.3 \pm 0.3V$

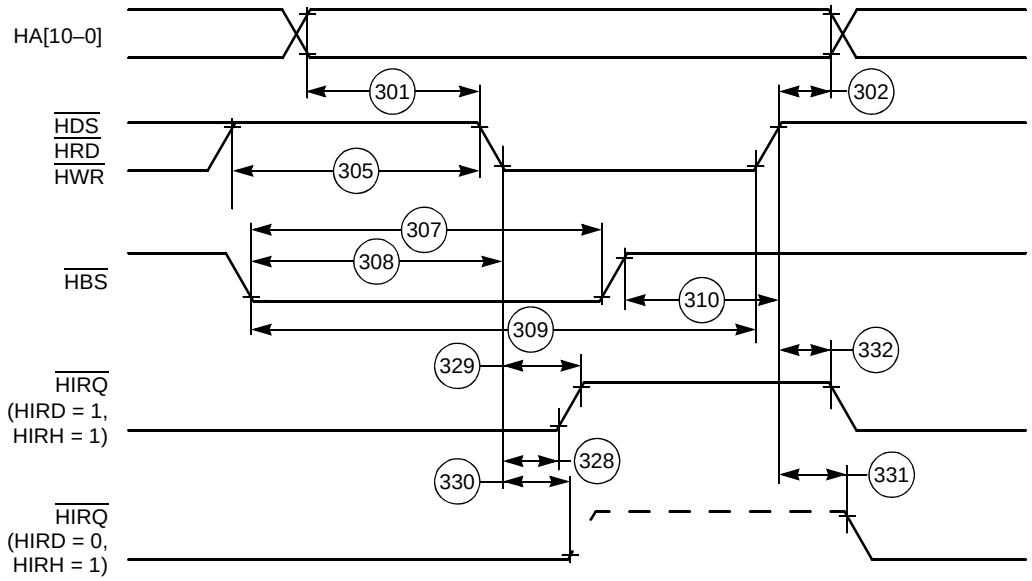


Figure 2-27. Universal Bus Mode I/O Access Timing

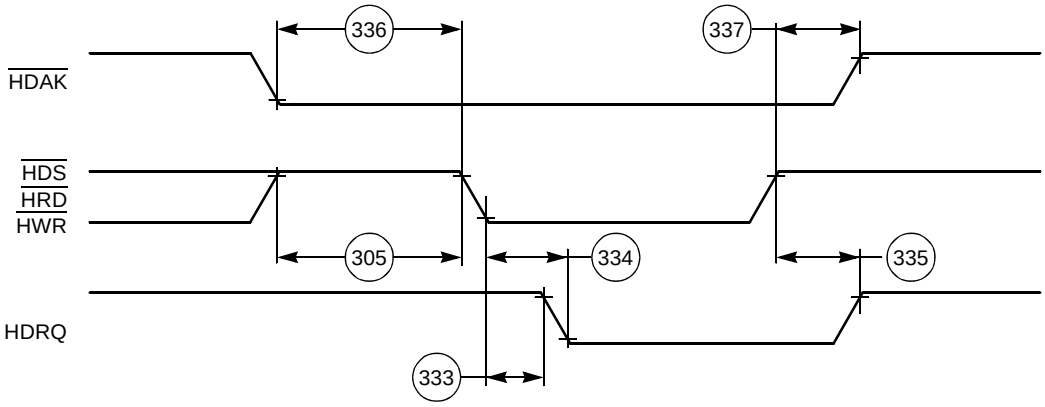


Figure 2-28. Universal Bus Mode DMA Access Timing

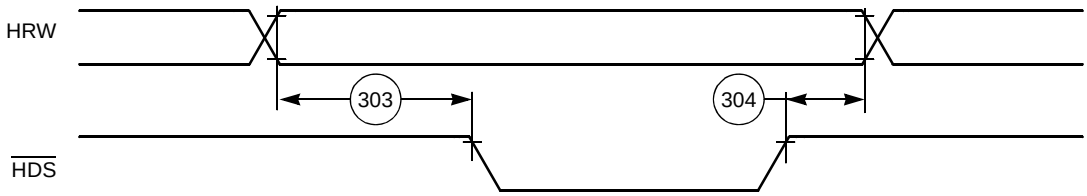


Figure 2-29. HRW to HDS Timing

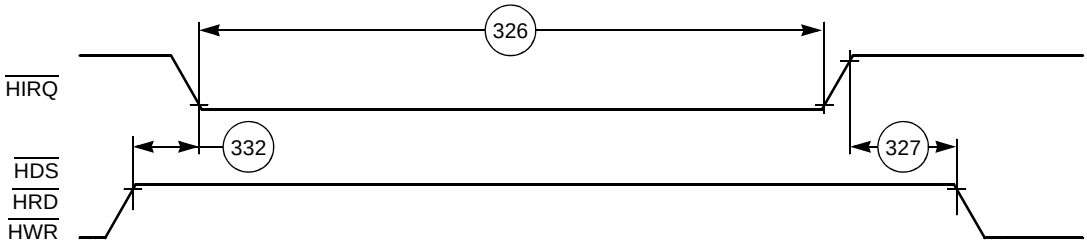


Figure 2-30. HIRQ Pulse Width (HIRH = 0)

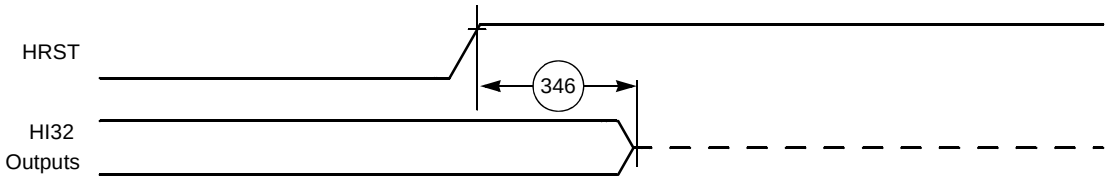
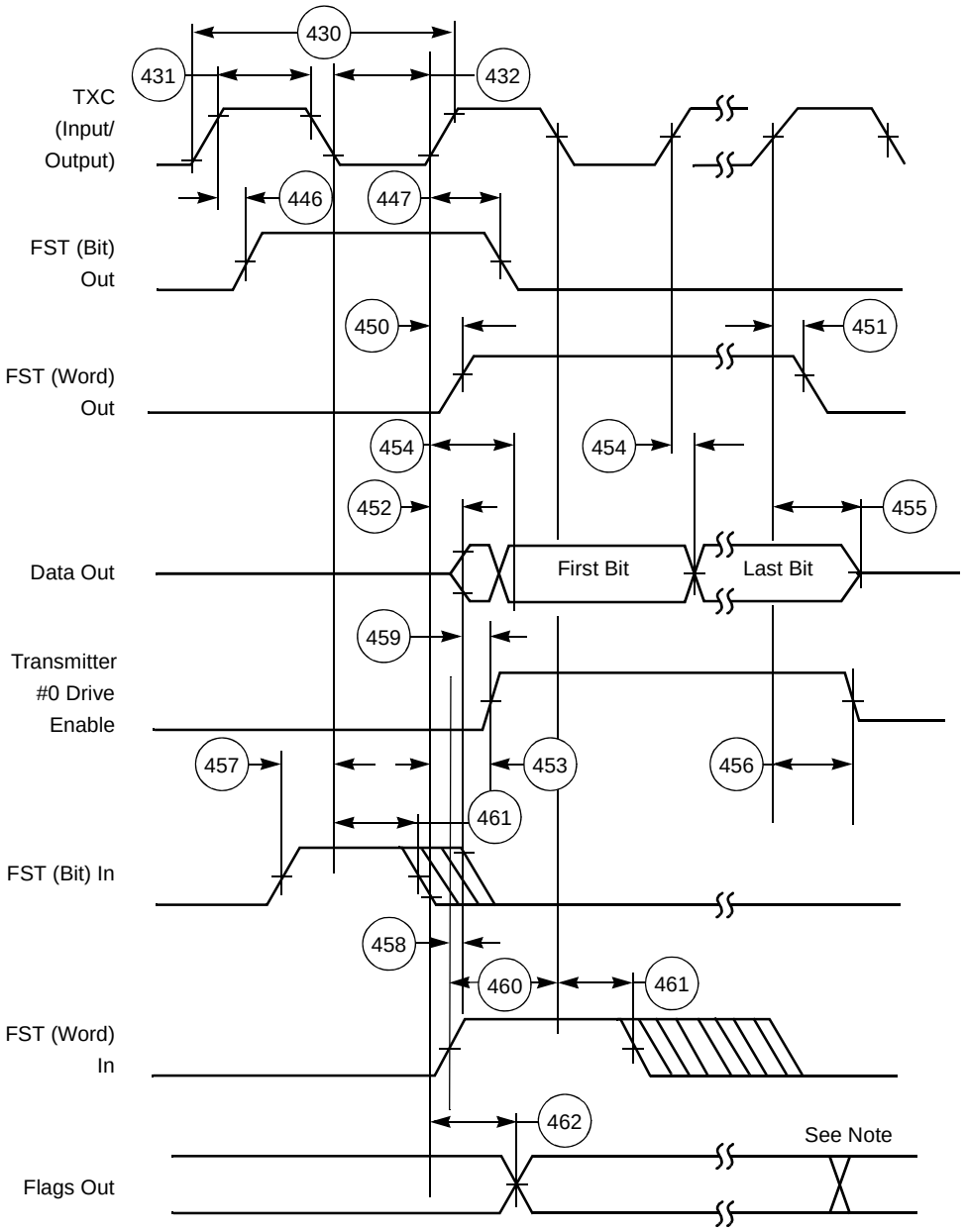


Figure 2-31. HRST Timing



Note: In Network mode, output flag transitions can occur at the start of each time slot within the frame. In Normal mode, the output flag state is asserted for the entire frame period.

Figure 2-40. ESSI Transmitter Timing

Table 2-23. Timer Timing (Continued)

No.	Characteristics	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
485	CLKOUT rising edge to TIO (Output) deassertion • Minimum • Maximum	 $0.5 \times T_C + 0.5$ $0.5 \times T_C + 19.8$	 9.8 —	 — 26.1	 5.5 —	 — 24.8	 ns ns
Note: $V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF$							

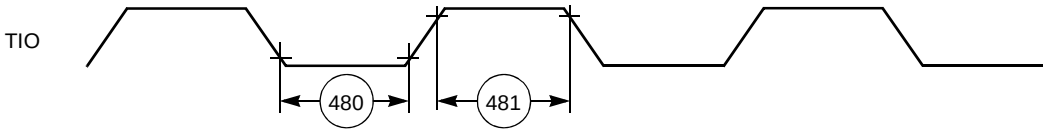


Figure 2-42. TIO Timer Event Input Restrictions

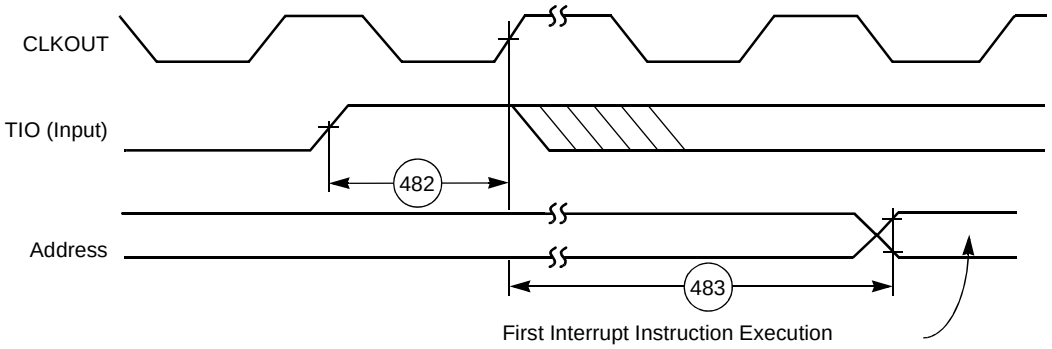


Figure 2-43. Timer Interrupt Generation

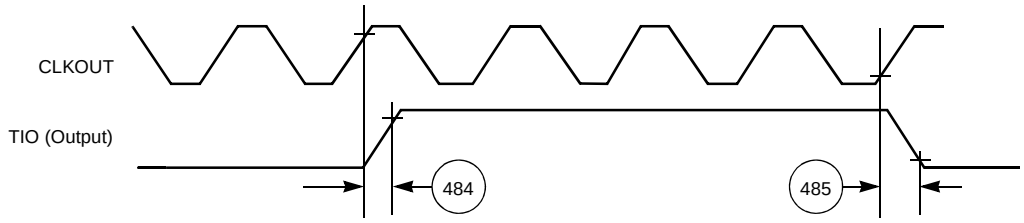


Figure 2-44. External Pulse Generation

2.5.10 GPIO Timing

Table 2-24. GPIO Timing

No.	Characteristics	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
490	CLKOUT edge to GPIO out valid (GPIO out delay time)		—	31.0	—	8.5	ns
491	CLKOUT edge to GPIO out not valid (GPIO out hold time)		0.0	—	0.0	—	ns
492	GPIO In valid to CLKOUT edge (GPIO in set-up time)		8.5	—	8.5	—	ns
493	CLKOUT edge to GPIO in not valid (GPIO in hold time)		0.0	—	0.0	—	ns
494	Fetch to CLKOUT edge before GPIO change	$6.75 \times T_C$	84.4	—	67.5	—	ns
Note: $V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF$							

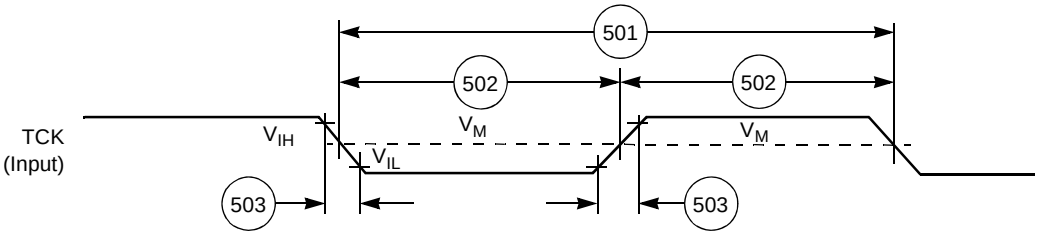


Figure 2-46. Test Clock Input Timing Diagram

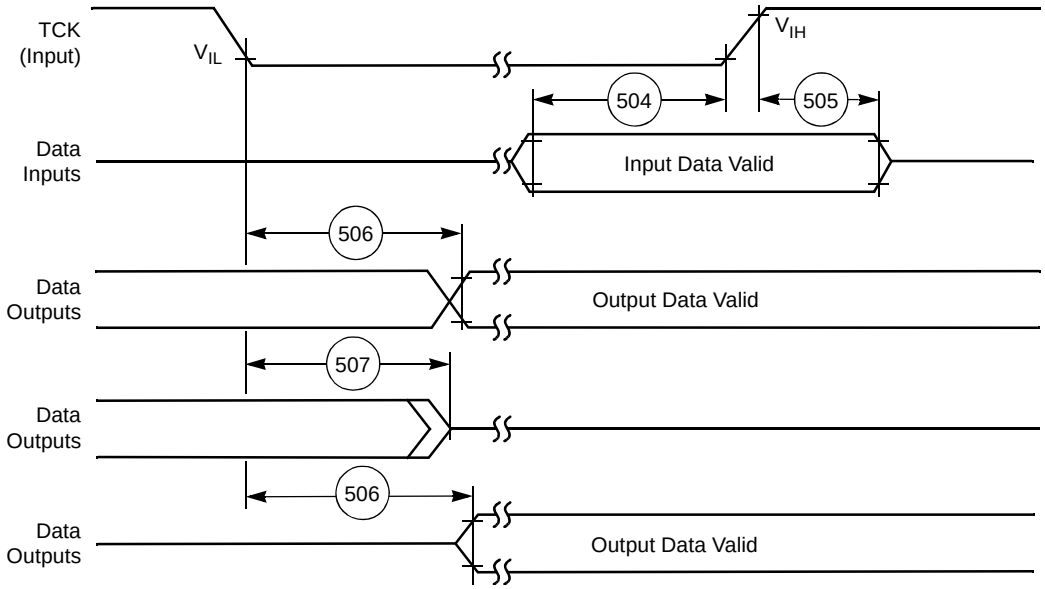


Figure 2-47. Boundary Scan (JTAG) Timing Diagram

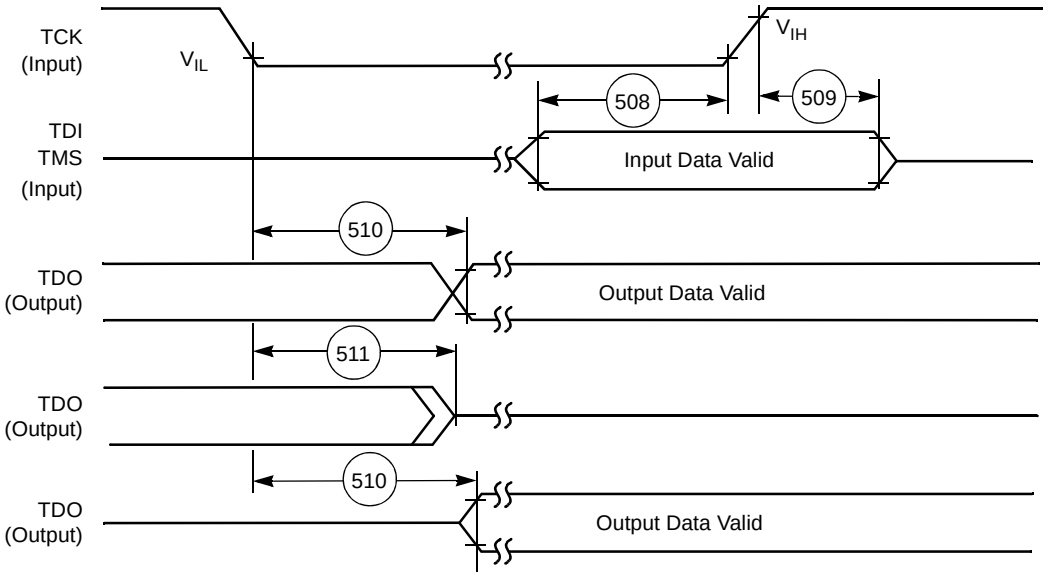


Figure 2-48. Test Access Port Timing Diagram

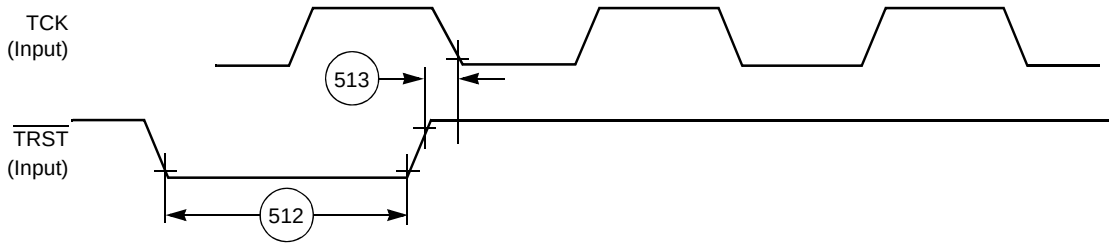


Figure 2-49. $\overline{\text{TRST}}$ Timing Diagram

2.5.12 OnCE Module TimIng

Table 2-26. OnCE Module Timing

No.	Characteristics	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
500	TCK frequency of operation	$1/(T_C \times 3)$, max: 22.0 MHz	0.0	22.0	0.0	22.0	MHz
514	$\overline{\text{DE}}$ assertion time in order to enter Debug mode	$1.5 \times T_C + 10.0$	28.8	—	25.0	—	ns
515	Response time when DSP56301 is executing NOP instructions from internal memory	$5.5 \times T_C + 30.0$	—	98.8	—	85.0	ns
516	Debug acknowledge assertion time	$3 \times T_C - 5.0$	47.5	—	25.0	—	ns
Note:	$V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF$						

Figure 2-50. OnCE—Debug Request

3.1 TQFP Package Description

Top and bottom views of the TQFP package are shown in **Figure 3-1** and **Figure 3-2** with their pin-outs.

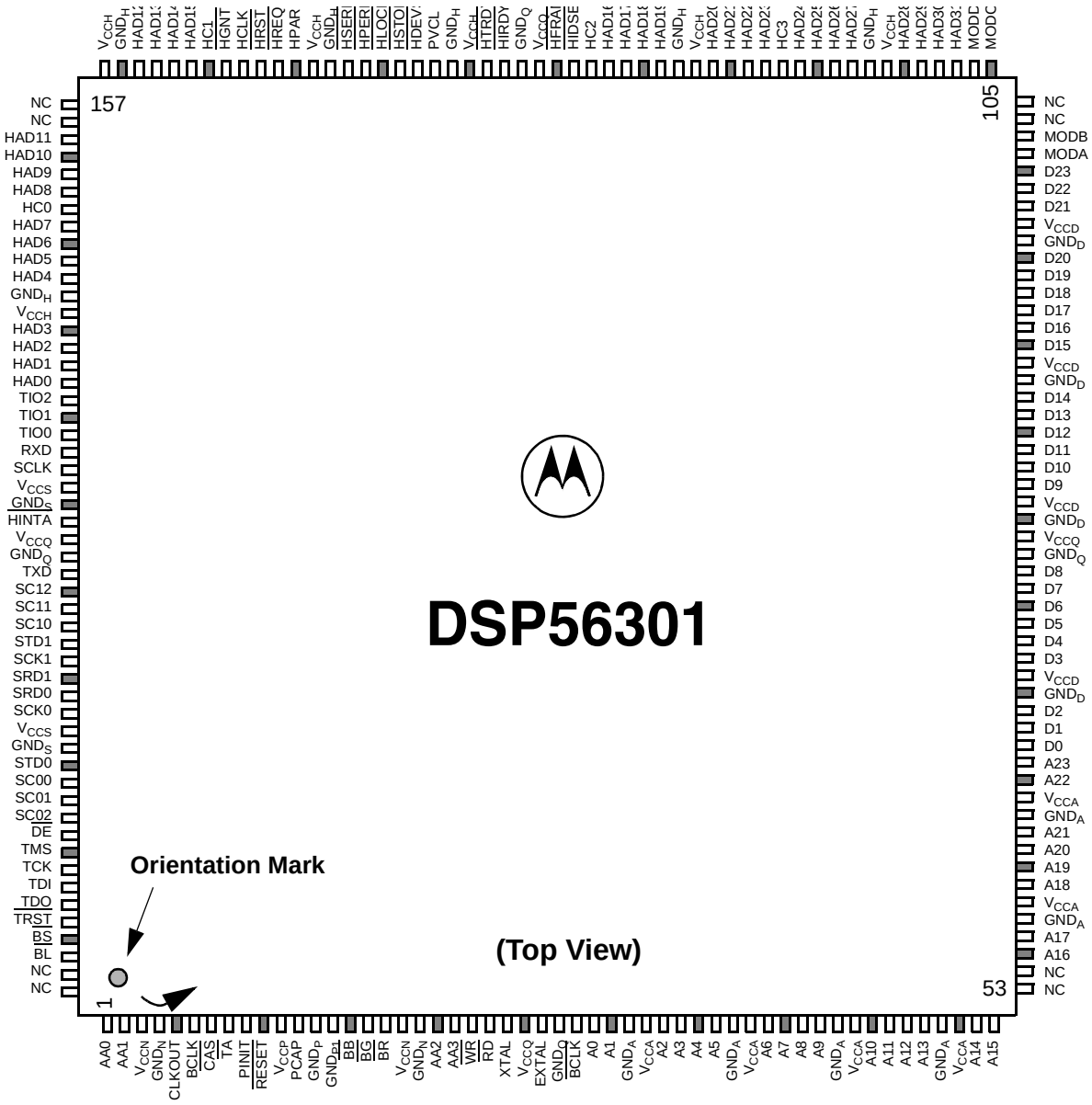


Figure 3-1. DSP56301 Thin Quad Flat Pack (TQFP), Top View

Table 3-2. DSP56301 TQFP Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
HD22	108	$\overline{\text{HRST}}$/HRST	147	PB0	173
HD23	107	HRW	139	PB1	172
HD3	159	$\overline{\text{HSAK}}$	138	PB10	160
HD4	154	$\overline{\text{HSERR}}$	142	PB11	159
HD5	153	$\overline{\text{HSTOP}}$	139	PB12	154
HD6	152	$\overline{\text{HTA}}$	146	PB13	153
HD7	151	$\overline{\text{HTRDY}}$	134	PB14	152
HD8	127	$\overline{\text{HWR}}$	139	PB15	151
HD9	126	$\overline{\text{IRQA}}$	101	PB16	163
$\overline{\text{HDAK}}$	145	$\overline{\text{IRQB}}$	102	PB17	150
$\overline{\text{HDBDR}}$	133	$\overline{\text{IRQC}}$	105	PB18	128
$\overline{\text{HDBEN}}$	134	$\overline{\text{IRQD}}$	106	PB19	117
$\overline{\text{HDEVSEL}}$	138	MODA	101	PB2	171
HDRQ	141	MODB	102	PB20	134
$\overline{\text{HDS}}$	129	MODC	105	PB21	133
$\overline{\text{HFRAME}}$	130	MODD	106	PB22	138
$\overline{\text{HGNT}}$	149	NC	28	PB23	140
HIDSEL	129	NC	53	PB3	170
$\overline{\text{HINTA}}$	181	NC	54	PB4	167
$\overline{\text{HIRDY}}$	133	NC	103	PB5	166
$\overline{\text{HIRQ}}$	142	NC	104	PB6	165
$\overline{\text{HLOCK}}$	140	NC	157	PB7	164
HPAR	145	NC	158	PB8	162
$\overline{\text{HPERR}}$	141	NC	207	PB9	161
$\overline{\text{HRD}}$	129	NC	208	PC0	196
$\overline{\text{HREQ}}$	146	$\overline{\text{NMI}}$	9	PC1	197

Table 3-4. DSP56301 MAP-BGA Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	T10	AA2	R7	D22	E15
A1	N9	AA3	P8	D23	D16
A10	T13	$\overline{BB}$	R6	D3	K14
A11	R13	BCLK	T3	D4	K16
A12	P12	$\overline{BCLK}$	R9	D5	J14
A13	T14	$\overline{BG}$	P7	D6	K15
A14	R14	$\overline{BL}$	N4	D7	J16
A15	P14	$\overline{BR}$	T7	D8	H16
A16	N13	$\overline{BS}$	P2	D9	H14
A17	N14	$\overline{CAS}$	R4	$\overline{DE}$	M2
A18	P16	CLKOUT	P4	EXTAL	P9
A19	M13	D0	L14	GND	F10
A2	N10	D1	L16	GND	F11
A20	N15	D10	J15	GND	F6
A21	M14	D11	H13	GND	F7
A22	M15	D12	G13	GND	F8
A23	M16	D13	H15	GND	F9
A3	R10	D14	G16	GND	G10
A4	T11	D15	G14	GND	G11
A5	P10	D16	G15	GND	G6
A6	R11	D17	F16	GND	G7
A7	T12	D18	F13	GND	G8
A8	P11	D19	F14	GND	G9
A9	R12	D2	L15	GND	H10
AA0	P3	D20	F15	GND	H11
AA1	R3	D21	E16	GND	H6

- If the temperature of the package case (T_T) is determined by a thermocouple, thermal resistance is computed from the value obtained by the equation $(T_J - T_T)/P_D$.

As noted earlier, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable to determine the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, the use of the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will yield an estimate of a junction temperature slightly higher than actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when the surface temperature of the package is used. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

4.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

Use the following list of recommendations to ensure correct DSP operation.

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP and from the board ground to each GND pin.
- Use at least six 0.01–0.1 µF bypass capacitors positioned as close as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer PCB with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{TA}}$, and $\overline{\text{BG}}$ pins. Maximum PCB trace lengths on the order of 6 inches are recommended.
- Consider all device loads as well as parasitic capacitance due to PCB traces when you calculate capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (that is, not allowed to float) by CMOS levels except for the three pins with internal pull-up resistors ($\overline{\text{TRST}}$, TMS, $\overline{\text{DE}}$).
- Take special care to minimize noise levels on the V_{CCP}, GND_P, and GND_{P1} pins.
- The following pins must be asserted after power-up: $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$.

```
        do      #(XDAT_END-XDAT_START),XLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,x:(r0)+
XLOAD_LOOP
;
;Load the Y-data
;
        move    #INT_YDAT,r0
        move    #YDAT_START,r1
        do      #(YDAT_END-YDAT_START),YLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,y:(r0)+
YLOAD_LOOP
;

        jmp     INT_PROG

PROG_START
        move    #$0,r0
        move    #$0,r4
        move    #$3f,m0
        move    #$3f,m4
;
        clr     a
        clr     b
        move    #$0,x0
        move    #$0,x1
        move    #$0,y0
        move    #$0,y1
        bset    #4,omr          ; ebd
;
sbr     dor     #60,_end
        mac     x0,y0,ax:(r0)+,x1     y:(r4)+,y1
        mac     x1,y1,ax:(r0)+,x0     y:(r4)+,y0
        add     a,b
        mac     x0,y0,ax:(r0)+,x1
        mac     x1,y1,a               y:(r4)+,y0
        move    b1,x:$ff
_end
        bra     sbr
        nop
        nop
        nop
        nop
PROG_END
        nop
        nop


XDAT_START
;       org     x:0
        dc      $262EB9
        dc      $86F2FE
        dc      $E56A5F
        dc      $616CAC
        dc      $8FFD75
        dc      $9210A
        dc      $A06D7B
        dc      $CEA798
        dc      $8DFBF1
        dc      $A063D6
```

```
        dc      $6A39E8
        dc      $81E801
        dc      $C666A6
        dc      $46F8E7
        dc      $AAEC94
        dc      $24233D
        dc      $802732
        dc      $2E3C83
        dc      $A43E00
        dc      $C2B639
        dc      $85A47E
        dc      $ABFDDF
        dc      $F3A2C
        dc      $2D7CF5
        dc      $E16A8A
        dc      $ECB8FB
        dc      $4BED18
        dc      $43F371
        dc      $83A556
        dc      $E1E9D7
        dc      $ACA2C4
        dc      $8135AD
        dc      $2CE0E2
        dc      $8F2C73
        dc      $432730
        dc      $A87FA9
        dc      $4A292E
        dc      $A63CCF
        dc      $6BA65C
        dc      $E06D65
        dc      $1AA3A
        dc      $A1B6EB
        dc      $48AC48
        dc      $EF7AE1
        dc      $6E3006
        dc      $62F6C7
        dc      $6064F4
        dc      $87E41D
        dc      $CB2692
        dc      $2C3863
        dc      $C6BC60
        dc      $43A519
        dc      $6139DE
        dc      $ADF7BF
        dc      $4B3E8C
        dc      $6079D5
        dc      $E0F5EA
        dc      $8230DB
        dc      $A3B778
        dc      $2BFE51
        dc      $E0A6B6
        dc      $68FFB7
        dc      $28F324
        dc      $8F2E8D
        dc      $667842
        dc      $83E053
        dc      $A1FD90
        dc      $6B2689
        dc      $85B68E
        dc      $622EAF
```

```
M_DSR3 EQU $FFFFE3; DMA3 Source Address Register
M_DDR3 EQU $FFFFE2; DMA3 Destination Address Register
M_DCO3 EQU $FFFFE1; DMA3 Counter
M_DCR3 EQU $FFFFE0; DMA3 Control Register

;       Register Addresses Of DMA4


M_DSR4 EQU $FFFFDF; DMA4 Source Address Register
M_DDR4 EQU $FFFFDE; DMA4 Destination Address Register
M_DCO4 EQU $FFFFDD; DMA4 Counter
M_DCR4 EQU $FFFFDC; DMA4 Control Register

;       Register Addresses Of DMA5

M_DSR5 EQU $FFFFDB; DMA5 Source Address Register
M_DDR5 EQU $FFFFDA; DMA5 Destination Address Register
M_DCO5 EQU $FFFFD9; DMA5 Counter
M_DCR5 EQU $FFFFD8; DMA5 Control Register

;       DMA Control Register

M_DSS EQU $3   ; DMA Source Space Mask (DSS0-Dss1)
M_DSS0 EQU 0   ; DMA Source Memory space 0
M_DSS1 EQU 1   ; DMA Source Memory space 1
M_DDS EQU $C   ; DMA Destination Space Mask (DDS-DDS1)
M_DDS0 EQU 2   ; DMA Destination Memory Space 0
M_DDS1 EQU 3   ; DMA Destination Memory Space 1
M_DAM EQU $3F0 ; DMA Address Mode Mask (DAM5-DAM0)
M_DAM0 EQU 4   ; DMA Address Mode 0
M_DAM1 EQU 5   ; DMA Address Mode 1
M_DAM2 EQU 6   ; DMA Address Mode 2
M_DAM3 EQU 7   ; DMA Address Mode 3
M_DAM4 EQU 8   ; DMA Address Mode 4
M_DAM5 EQU 9   ; DMA Address Mode 5
M_D3D EQU 10   ; DMA Three Dimensional Mode
M_DRS EQU $F800; DMA Request Source Mask (DRS0-DRS4)
M_DCON EQU 16  ; DMA Continuous Mode
M_DPR EQU $60000; DMA Channel Priority
M_DPR0 EQU 17  ; DMA Channel Priority Level (low)
M_DPR1 EQU 18  ; DMA Channel Priority Level (high)
M_DTM EQU $380000; DMA Transfer Mode Mask (DTM2-DTM0)
M_DTM0 EQU 19  ; DMA Transfer Mode 0
M_DTM1 EQU 20  ; DMA Transfer Mode 1
M_DTM2 EQU 21  ; DMA Transfer Mode 2
M_DIE EQU 22   ; DMA Interrupt Enable bit
M_DE EQU 23    ; DMA Channel Enable bit

;       DMA Status Register

M_DTD EQU $3F  ; Channel Transfer Done Status MASK (DTD0-DTD5)
M_DTD0 EQU 0       ; DMA Channel Transfer Done Status 0
M_DTD1 EQU 1       ; DMA Channel Transfer Done Status 1
M_DTD2 EQU 2       ; DMA Channel Transfer Done Status 2
M_DTD3 EQU 3       ; DMA Channel Transfer Done Status 3
M_DTD4 EQU 4       ; DMA Channel Transfer Done Status 4
M_DTD5 EQU 5       ; DMA Channel Transfer Done Status 5
M_DACT EQU 8   ; DMA Active State
M_DCH EQU $E00 ; DMA Active Channel Mask (DCH0-DCH2)
M_DCH0 EQU 9   ; DMA Active Channel 0
```

```
M_DCH1 EQU 10  ; DMA Active Channel 1
M_DCH2 EQU 11  ; DMA Active Channel 2


;------------------------------------------------------------------------
;
;       EQUATES for Phase Lock Loop (PLL)
;
;------------------------------------------------------------------------

;       Register Addresses Of PLL

M_PCTL EQU $FFFFFD; PLL Control Register

;       PLL Control Register

M_MF EQU $FFF   ; Multiplication Factor Bits Mask (MF0-MF11)
M_DF EQU $7000  ; Division Factor Bits Mask (DF0-DF2)
M_XTLR EQU 15     ; XTAL Range select bit
M_XTLD EQU 16     ; XTAL Disable Bit
M_PSTP EQU 17     ; STOP Processing State Bit
M_PEN EQU 18     ; PLL Enable Bit
M_PCOD EQU 19     ; PLL Clock Output Disable Bit
M_PD EQU $F00000; PreDivider Factor Bits Mask (PD0-PD3)


;------------------------------------------------------------------------
;
;       EQUATES for BIU
;
;------------------------------------------------------------------------

;       Register Addresses Of BIU


M_BCR EQU $FFFFFB; Bus Control Register
M_DCR EQU $FFFFFA; DRAM Control Register
M_AAR0 EQU $FFFFF9; Address Attribute Register 0
M_AAR1 EQU $FFFFF8; Address Attribute Register 1
M_AAR2 EQU $FFFFF7; Address Attribute Register 2
M_AAR3 EQU $FFFFF6; Address Attribute Register 3
M_IDR EQU $FFFFF5; ID Register

;       Bus Control Register

M_BA0W EQU $1F    ; Area 0 Wait Control Mask (BA0W0-BA0W4)
M_BA1W EQU $3E0   ; Area 1 Wait Control Mask (BA1W0-BA14)
M_BA2W EQU $1C00  ; Area 2 Wait Control Mask (BA2W0-BA2W2)
M_BA3W EQU $E000  ; Area 3 Wait Control Mask (BA3W0-BA3W3)
M_BDFW EQU $1F0000; Default Area Wait Control Mask (BDFW0-BDFW4)
M_BBS EQU 21     ; Bus State
M_BLH EQU 22     ; Bus Lock Hold
M_BRH EQU 23     ; Bus Request Hold

;       DRAM Control Register

M_BCW EQU $3     ; In Page Wait States Bits Mask (BCW0-BCW1)
M_BRW EQU $C     ; Out Of Page Wait States Bits Mask (BRW0-BRW1)
M_BPS EQU $300   ; DRAM Page Size Bits Mask (BPS0-BPS1)
M_BPLE EQU 11     ; Page Logic Enable
```

```
M_BME EQU 12     ; Mastership Enable
M_BRE EQU 13     ; Refresh Enable
M_BSTR EQU 14     ; Software Triggered Refresh
M_BRF EQU $7F8000; Refresh Rate Bits Mask (BRF0-BRF7)
M_BRP EQU 23     ; Refresh prescaler

;       Address Attribute Registers

M_BAT EQU $3     ; External Access Type and Pin Definition Bits Mask (BAT0-BAT1)
M_BAAP EQU 2      ; Address Attribute Pin Polarity
M_BPEN EQU 3      ; Program Space Enable
M_BXEN EQU 4      ; X Data Space Enable
M_BYEN EQU 5      ; Y Data Space Enable
M_BAM EQU 6      ; Address Muxing
M_BPAC EQU 7   ; Packing Enable
M_BNC EQU $F00   ; Number of Address Bits to Compare Mask (BNC0-BNC3)
M_BAC EQU $FFF000; Address to Compare Bits Mask (BAC0-BAC11)

;       control and status bits in SR

M_CP EQU $c00000 ; mask for CORE-DMA priority bits in SR
M_CA EQU 0       ; Carry
M_V EQU 1       ; Overflow
M_Z EQU 2       ; Zero
M_N EQU 3       ; Negative
M_U EQU 4       ; Unnormalized
M_E EQU 5       ; Extension
M_L EQU 6       ; Limit
M_S EQU 7       ; Scaling Bit
M_I0 EQU 8       ; Interupt Mask Bit 0
M_I1 EQU 9       ; Interupt Mask Bit 1
M_S0 EQU 10      ; Scaling Mode Bit 0
M_S1 EQU 11      ; Scaling Mode Bit 1
M_SC EQU 13      ; Sixteen_Bit Compatibility
M_DM EQU 14      ; Double Precision Multiply
M_LF EQU 15      ; DO-Loop Flag
M_FV EQU 16      ; DO-Forever Flag
M_SA EQU 17      ; Sixteen-Bit Arithmetic
M_CE EQU 19      ; Instruction Cache Enable
M_SM EQU 20      ; Arithmetic Saturation
M_RM EQU 21      ; Rounding Mode
M_CP0 EQU22      ; bit 0 of priority bits in SR
M_CP1 EQU 23      ; bit 1 of priority bits in SR

;       control and status bits in OMR
M_CDP EQU$300  ; mask for CORE-DMA priority bits in OMR
M_MA EQU 0       ; Operating Mode A
M_MB EQU 1       ; Operating Mode B
M_MC EQU 2       ; Operating Mode C
M_MD EQU 3       ; Operating Mode D
M_EBD EQU 4       ; External Bus Disable bit in OMR
M_SD EQU 6       ; Stop Delay
M_CDP0 EQU 8       ; bit 0 of priority bits in OMR
M_CDP1 EQU 9       ; bit 1 of priority bits in OMR
M_BEN EQU 10      ; Burst Enable
M_TAS EQU 11      ; TA Synchronize Select
M_BRT EQU 12      ; Bus Release Timing
M_XYS EQU 16      ; Stack Extension space select bit in OMR.
M_EUN EQU 17      ; Extensed stack UNderflow flag in OMR.
M_EOV EQU 18      ; Extended stack OVerflow flag in OMR.
```