Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	100MHz
Non-Volatile Memory	ROM (9kB)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	252-BGA
Supplier Device Package	252-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56301vf100

DSP56301 Features

High-Performance DSP56300 Core

- 80/100 million instructions per second (MIPS) with a 80/100 MHz clock at 3.0–3.6 V
- Object code compatible with the DSP56000 core with highly parallel instruction set
- Data Arithmetic Logic Unit (Data ALU) with fully pipelined 24 × 24-bit parallel Multiplier-Accumulator (MAC), 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control
- Program Control Unit (PCU) with Position Independent Code (PIC) support, addressing modes optimized for DSP applications (including immediate offsets), internal instruction cache controller, internal memory-expandable hardware stack, nested hardware DO loops, and fast auto-return interrupts
- Direct Memory Access (DMA) with six DMA channels supporting internal and external accesses; one-, two-, and three-dimensional transfers (including circular buffering); end-of-block-transfer interrupts; and triggering from interrupt lines and all peripherals
- Phase Lock Loop (PLL) allows change of low-power Divide Factor (DF) without loss of lock and output clock with skew elimination
- Hardware debugging support including On-Chip Emulation (OnCE™) module, Joint Test Action Group (JTAG) Test Access Port (TAP)

Internal Peripherals

- 32-bit parallel PCI/Universal Host Interface (HI32), PCI Rev. 2.1 compliant with glueless interface to other DSP563xx buses or ISA interface requiring only 74LS45-style buffers
- Two enhanced synchronous serial interfaces (ESSI), each with one receiver and three transmitters (allows six-channel home theater)
- Serial communications interface (SCI) with baud rate generator
- Triple timer module
- Up to forty-two programmable general-purpose input/output (GPIO) pins, depending on which peripherals are enabled

Internal Memories

- 3 K × 24-bit bootstrap ROM
- 8 K × 24-bit internal RAM total
- Program RAM, Instruction Cache, X data RAM, and Y data RAM sizes are programmable:

Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data RAM Size	Instruction Cache	Switch Mode
4096 × 24 bits	0	2048 × 24 bits	2048 × 24 bits	disabled	disabled
3072 × 24 bits	1024 × 24-bit	2048 × 24 bits	2048 × 24 bits	enabled	disabled
2048 × 24 bits	0	3072 × 24 bits	3072 × 24 bits	disabled	enabled
1024 × 24 bits	1024 × 24-bit	3072 × 24 bits	3072 × 24 bits	enabled	enabled

Signals/Connections 1

The DSP56301 input and output signals are organized into functional groups, as shown in **Table 1-1** and illustrated in **Figure 1-1**. The DSP56301 operates from a 3 V supply; however, some of the inputs can tolerate 5 V. A special notice for this feature is added to the signal descriptions of those inputs.

Table 1-1. DSP56301 Functional Signal Groupings

Functional Group		Number of Signals by Package Type		Detailed Description
		TQFP	MAP-BGA	
Power (V_{CC})[1]		25	45	**Table 1-2**
Ground (GND)[1]		26	38	**Table 1-3**
Clock		2	2	**Table 1-4**
PLL		3	3	**Table 1-5**
Address Bus	Port A[2]	24	24	**Table 1-6**
Data Bus		24	24	**Table 1-7**
Bus Control		15	15	**Table 1-8**
Interrupt and Mode Control		5	5	**Table 1-9**
Host Interface (HI32)	Port B[3]	52	52	**Table 1-11**
Enhanced Synchronous Serial Interface (ESSI)	Ports C and D[4]	12	12	**Table 1-12** and **Table 1-13**
Serial Communication Interface (SCI)	Port E[5]	3	3	**Table 1-14**
Timer		3	3	**Table 1-15**
JTAG/OnCE Port		6	6	**Table 1-16**

Notes:
1. The number of available power and ground signals is package-dependent. In the TQFP package specific pins are dedicated internally to device subsystems. In the MAP-BGA package, power and ground connections (except those providing PLL power) connect to internal power and ground planes, respectively.
2. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals.
3. Port B signals are the HI32 port signals multiplexed with the GPIO signals.
4. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals.
5. Port E signals are the SCI port signals multiplexed with the GPIO signals.
6. Each device also includes several no connect (NC) pins. The number of NC connections is package-dependent: the TQFP has 9 NCs and the MAP-BGA has 20 NCs. Do not connect any line, component, trace, or via to these pins. See **Chapter 3** for details.

Table 1-11. Host Interface (Continued)

Signal Name	Type	State During Reset	Signal Description
HPAR HDAK	Input/ Output Input	Tri-stated	**Host Parity** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Parity signal. **Host DMA Acknowledge** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host DMA Acknowledge Schmitt-trigger signal. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
HPERR HDRQ	Input/ Output Output	Tri-stated	**Host Parity Error** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Parity Error signal. **Host DMA Request** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host DMA Request output. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
HGNT HAEN	Input Input	Input	**Host Bus Grant** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Bus Grant signal. **Host Address Enable** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Address Enable output signal. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
HREQ HTA	Output Output	Tri-stated	**Host Bus Request** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Bus Request signal. **Host Transfer Acknowledge**—When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Data Bus Enable signal. HTA can be programmed as active high or active low. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.

Table 1-13. Enhanced Synchronous Serial Interface 1 (ESSI1) (Continued)

Signal Name	Type	State During Reset	Signal Description
SRD1 PD4	Input/Output Input or Output	Input	**Serial Receive Data** Receives serial data and transfers it to the ESSI receive shift register. SRD1 is an input when data is being received. **Port D 4** The default configuration following reset is GPIO. For PD4, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SRD1 through PCR1. This input is 5 V tolerant.
STD1 PD5	Input/Output Input or Output	Input	**Serial Transmit Data** Transmits data from the serial transmit shift register. STD1 is an output when data is being transmitted. **Port D 5** The default configuration following reset is GPIO. For PD5, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal STD1 through PCR1. This input is 5 V tolerant.

1.10 Serial Communication Interface (SCI)

The Serial Communication interface (SCI) provides a full duplex port for serial communication with other DSPs, microprocessors, or peripherals such as modems.

Table 1-14. Serial Communication Interface (SCI)

Signal Name	Type	State During Reset	Signal Description
RXD PE0	Input Input or Output	Input	**Serial Receive Data** Receives byte-oriented serial data and transfers it to the SCI receive shift register. **Port E 0** The default configuration following reset is GPIO. When configured as PE0, signal direction is controlled through the SCI Port Directions Register (PRR). The signal can be configured as an SCI signal RXD through the SCI Port Control Register (PCR). This input is 5 V tolerant.
TXD PE1	Output Input or Output	Input	**Serial Transmit Data** Transmits data from SCI transmit data register. **Port E 1** The default configuration following reset is GPIO. When configured as PE1, signal direction is controlled through the SCI PRR. The signal can be configured as an SCI signal TXD through the SCI PCR. This input is 5 V tolerant.

2.5.4 Reset, Stop, Mode Select, and Interrupt Timing

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6]

No.	Characteristics	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
8	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3]	—	—	26.0	—	26.0	ns
9	Required $\overline{\text{RESET}}$ duration[4] • Power on, external clock generator, PLL disabled • Power on, external clock generator, PLL enabled • Power on, internal oscillator • During STOP, XTAL disabled (PCTL Bit 16 = 0) • During STOP, XTAL enabled (PCTL Bit 16 = 1) • During normal operation	 $50 \times ET_C$ $1000 \times ET_C$ $75000 \times ET_C$ $75000 \times ET_C$ $2.5 \times T_C$ $2.5 \times T_C$	 625.0 12.5 1.0 1.0 31.3 31.3	 — — — — — —	 500.0 10.0 0.75 0.75 25.0 25.0	 — — — — — —	 ns µs ms ms ns ns
10	Delay from asynchronous $\overline{\text{RESET}}$ deassertion to first external address output (internal reset deassertion)[5] • Minimum • Maximum	 $3.25 \times T_C + 2.0$ $20.25\ T_C + 10.0$	 42.6 —	 — 263.1	 34.5 —	 — 212.5	 ns ns
11	Synchronous reset setup time from $\overline{\text{RESET}}$ deassertion to CLKOUT Transition 1 • Minimum • Maximum	T_C	 7.4 —	 — 12.5	 5.9 —	 — 10.0	 ns ns
12	Synchronous reset deasserted, delay time from the CLKOUT Transition 1 to the first external address output • Minimum • Maximum	 $3.25 \times T_C + 1.0$ $20.25 \times T_C + 1.0$	 41.6 —	 — 258.1	 33.5 —	 — 207.5	 ns ns
13	Mode select setup time		30.0	—	30.0	—	ns
14	Mode select hold time		0.0	—	0.0	—	ns
15	Minimum edge-triggered interrupt request assertion width		8.25	—	6.6	—	ns
16	Minimum edge-triggered interrupt request deassertion width		8.25	—	7.1	—	ns
17	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory access address out valid • Caused by first interrupt instruction fetch • Caused by first interrupt instruction execution	 $4.25 \times T_C + 2.0$ $7.25 \times T_C + 2.0$	 55.1 92.6	 — —	 44.5 74.5	 — —	 ns ns
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution	$10 \times T_C + 5.0$	130.0	—	105.0	—	ns
19	Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts[1]	**80 MHz**: $3.75 \times T_C + WS \times T_C - 12.4$ **100 MHz**: $3.75 \times T_C + WS \times T_C - 10.94$	—	Note 8	—	Note 8	ns ns
20	Delay from $\overline{\text{RD}}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1]	**80 MHz**: $3.25 \times T_C + WS \times T_C - 12.4$ **100 MHz**: $3.25 \times T_C + WS \times T_C - 10.94$	—	Note 8	—	Note 8	ns ns

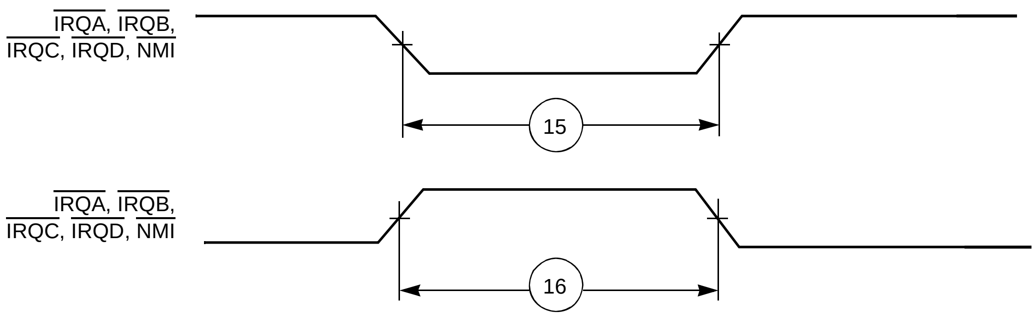


Figure 2-6. External Interrupt Timing (Negative Edge-Triggered)

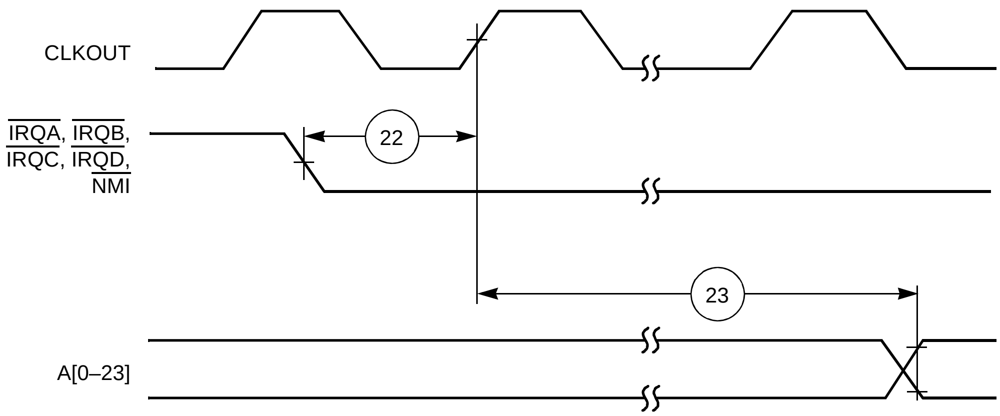


Figure 2-7. Synchronous Interrupt from Wait State Timing

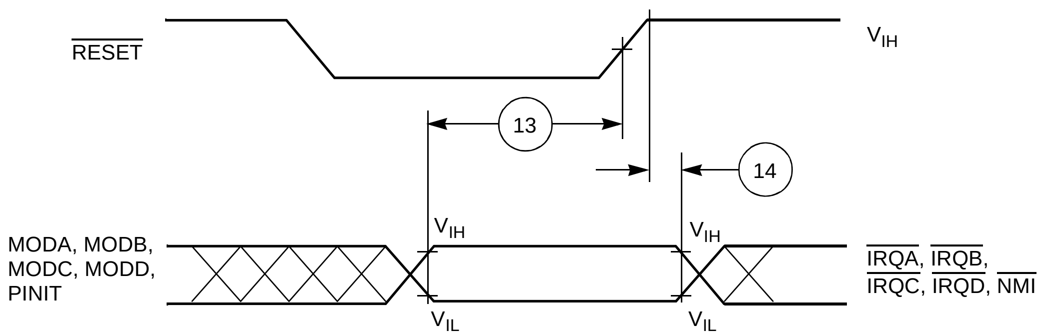
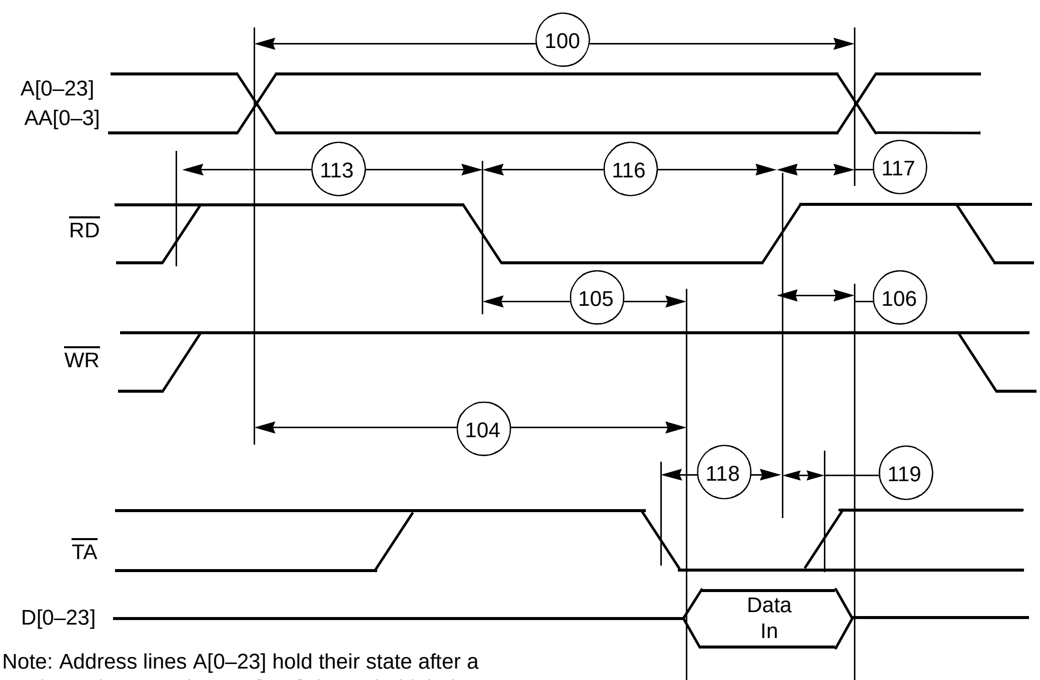


Figure 2-8. Operating Mode Select Timing

Table 2-8. SRAM Read and Write Accesses[3,6] (Continued)

No.	Characteristics	Symbol	Expression[1]	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
115	Address valid to $\overline{RD}$ assertion		$0.5 \times T_C - 4.0$	2.3	—	1.0	—	ns
116	$\overline{RD}$ assertion pulse width		$(WS + 0.25) \times T_C - 4.0$	11.6	—	8.5	—	ns
117	$\overline{RD}$ deassertion to address not valid		$0.25 \times T_C - 2.0$ [$1 \le WS \le 3$] $1.25 \times T_C - 2.0$ [$4 \le WS \le 7$] $2.25 \times T_C - 2.0$ [$WS \ge 8$]	1.1 13.6 26.1	— — —	0.5 10.5 20.5	— — —	ns ns ns
118	$\overline{TA}$ setup before $\overline{RD}$ or $\overline{WR}$ deassertion[4]		$0.25 \times T_C + 2.0$	5.1	—	4.5	—	ns
119	$\overline{TA}$ hold after $\overline{RD}$ or $\overline{WR}$ deassertion			0	—	0	—	ns

Notes:
1. WS is the number of wait states specified in the BCR.
2. Timings 100, 107 are guaranteed by design, not tested.
3. All timings for 100 MHz are measured from 0.5 · Vcc to 0.5 · Vcc
4. Timing 118 is relative to the deassertion edge of $\overline{RD}$ or $\overline{WR}$ even if $\overline{TA}$ remains active.
5. Timings 110, 111, and 112, are not helpful and are not specified for 100 MHz.
6. $V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100°C$, $C_L = 50\ pF$



Note: Address lines A[0–23] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-12. SRAM Read Access

Table 2-19. Universal Bus Mode, Synchronous Port A Type Host Timing (Continued)

No.	Characteristic	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
330	HIRQ High Impedance from Data Strobe Assertion (HIRH = 1, HIRD = 0)[1,6]	**80 MHz:** $2.5 \times T_C + 24.7$ **100 MHz:** $2.5 \times T_C + 21.5$	—	55.9	— 	46.5 	ns ns
331	HIRQ Active from Data Strobe Deassertion (HIRH = 1, HIRD = 0)[1]	$2.5 \times T_C$	31.3	—	25.0	—	ns
332	HIRQ Deasserted Hold from Data Strobe Deassertion[1]	$2.5 \times T_C$	31.3	—	25.0	—	ns
346	HRST Assertion to Host Port Pins High Impedance[2]		—	22.2	—	19.6	ns
347	HBS Assertion to CLKOUT Rising Edge		4.3	—	3.4	—	ns
348	Data Strobe Deassertion to CLKOUT Rising Edge[1]		7.4	—	5.9	—	ns

Notes:
1. The Data Strobe is HRD or HWR in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
2. HTA, HDRQ, and HRST may be programmed as active-high or active-low. In the example timing diagrams, HDRQ and HRST are shown as active-high and HTA is shown as active low.
3. The Read Data Strobe is HRD in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
4. The Write Data Strobe is HWR in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
5. HTA requires an external pull-down resistor if programmed as active high (HTAP = 0); or an external pull-up resistor if programmed as active low (HTAP = 1). The resistor value should be consistent with the DC specifications.
6. HIRQ requires an external pull-up resistor if programmed as open drain (HIRD = 0). The resistor value should be consistent with the DC specifications.
7. “LT” is the value of the latency timer register (CLAT) as programmed by the user during self configuration.
8. Values are valid for $V_{CC} = 3.3 \pm 0.3V$

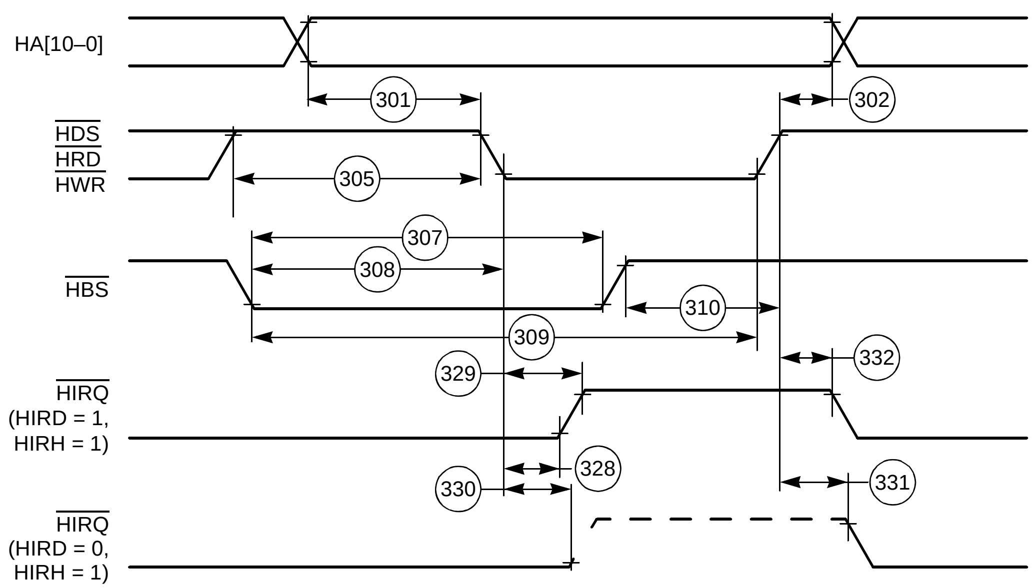


Figure 2-27. Universal Bus Mode I/O Access Timing

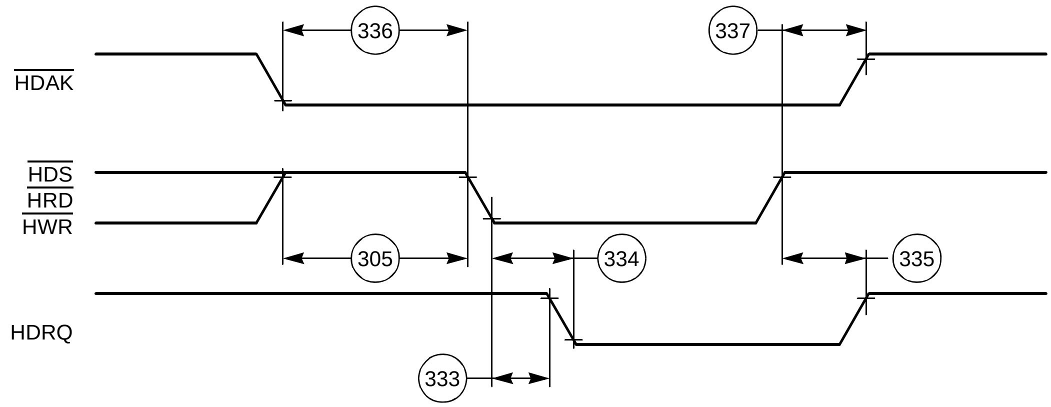


Figure 2-28. Universal Bus Mode DMA Access Timing

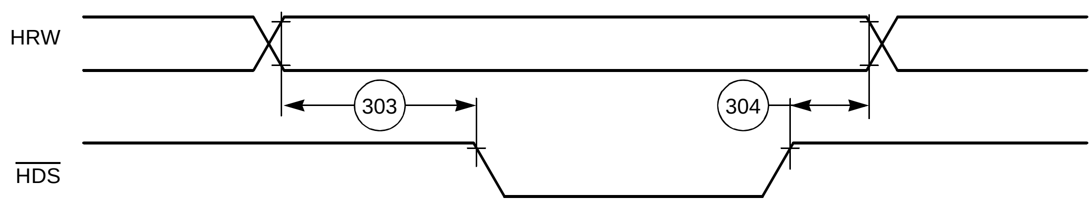


Figure 2-29. HRW to HDS Timing

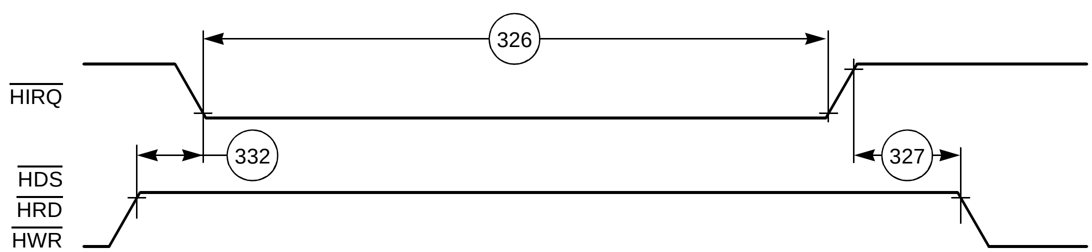


Figure 2-30. HIRQ Pulse Width (HIRH = 0)

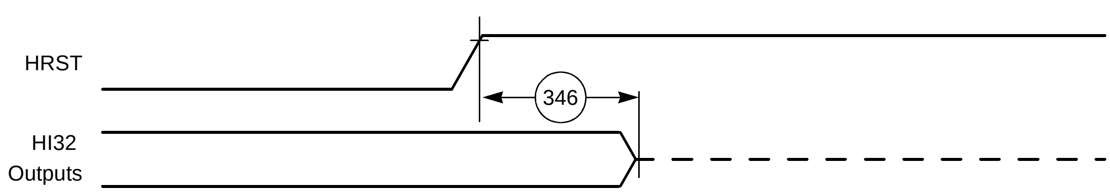


Figure 2-31. HRST Timing

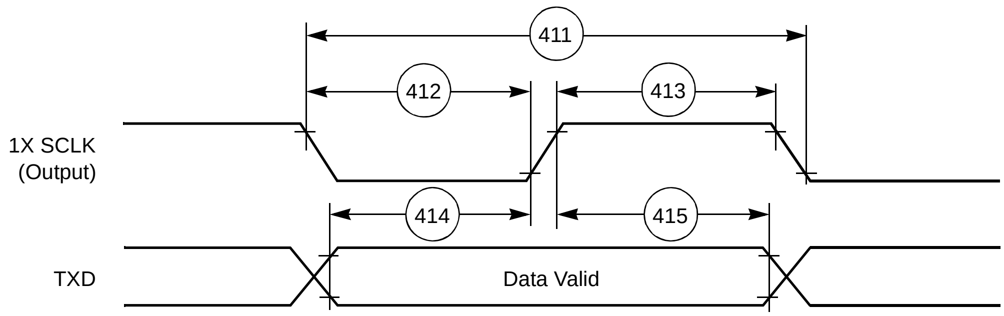


Figure 2-39. SCI Asynchronous Mode Timing

2.5.8 ESSI0/ESSI1 Timing

Table 2-22. ESSI Timings

No.	Characteristics[4, 5, 7]	Symbol	Expression	80 MHz		100 MHz		Cond-ition[6]	Unit
				Min	Max	Min	Max		
430	Clock cycle[1]	t_{SSICC}	$3 \times T_C$ $4 \times T_C$	50.0 37.5	— —	30.0 40.0	— —	x ck i ck	ns
431	Clock high period For internal clock For external clock		 $2 \times T_C - 10.0$ $1.5 \times T_C$	 15.0 18.8	 — —	 10.0 15.0	 — —		 ns ns
432	Clock low period For internal clock For external clock		 $2 \times T_C - 10.0$ $1.5 \times T_C$	 15.0 18.8	 — —	 10.0 15.0	 — —		 ns ns
433	RXC rising edge to FSR out (bl) high			— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
434	RXC rising edge to FSR out (bl) low			— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
435	RXC rising edge to FSR out (wr) high[2]			— —	39.0 24.0	— —	39.0 24.0	x ck i ck a	ns
436	RXC rising edge to FSR out (wr) low[2]			— —	39.0 24.0	— —	39.0 24.0	x ck i ck a	ns
437	RXC rising edge to FSR out (wl) high			— —	36.0 21.0	— —	36.0 21.0	x ck i ck a	ns
438	RXC rising edge to FSR out (wl) low			— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
439	Data in setup time before RXC (SCK in Synchronous mode) falling edge			10.0 19.0	— —	10.0 19.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge			5.0 3.0	— —	5.0 3.0	— —	x ck i ck	ns
441	FSR input (bl, wr) high before RXC falling edge[2]			1.0 23.0	— —	1.0 23.0	— —	x ck i ck a	ns
442	FSR input (wl) high before RXC falling edge			3.5 23.0	— —	3.5 23.0	— —	x ck i ck a	ns
443	FSR input hold time after RXC falling edge			3.0 0.0	— —	3.0 0.0	— —	x ck i ck a	ns
444	Flags input setup before RXC falling edge			5.5 19.0	— —	5.5 19.0	— —	x ck i ck s	ns

Table 2-22. ESSI Timings (Continued)

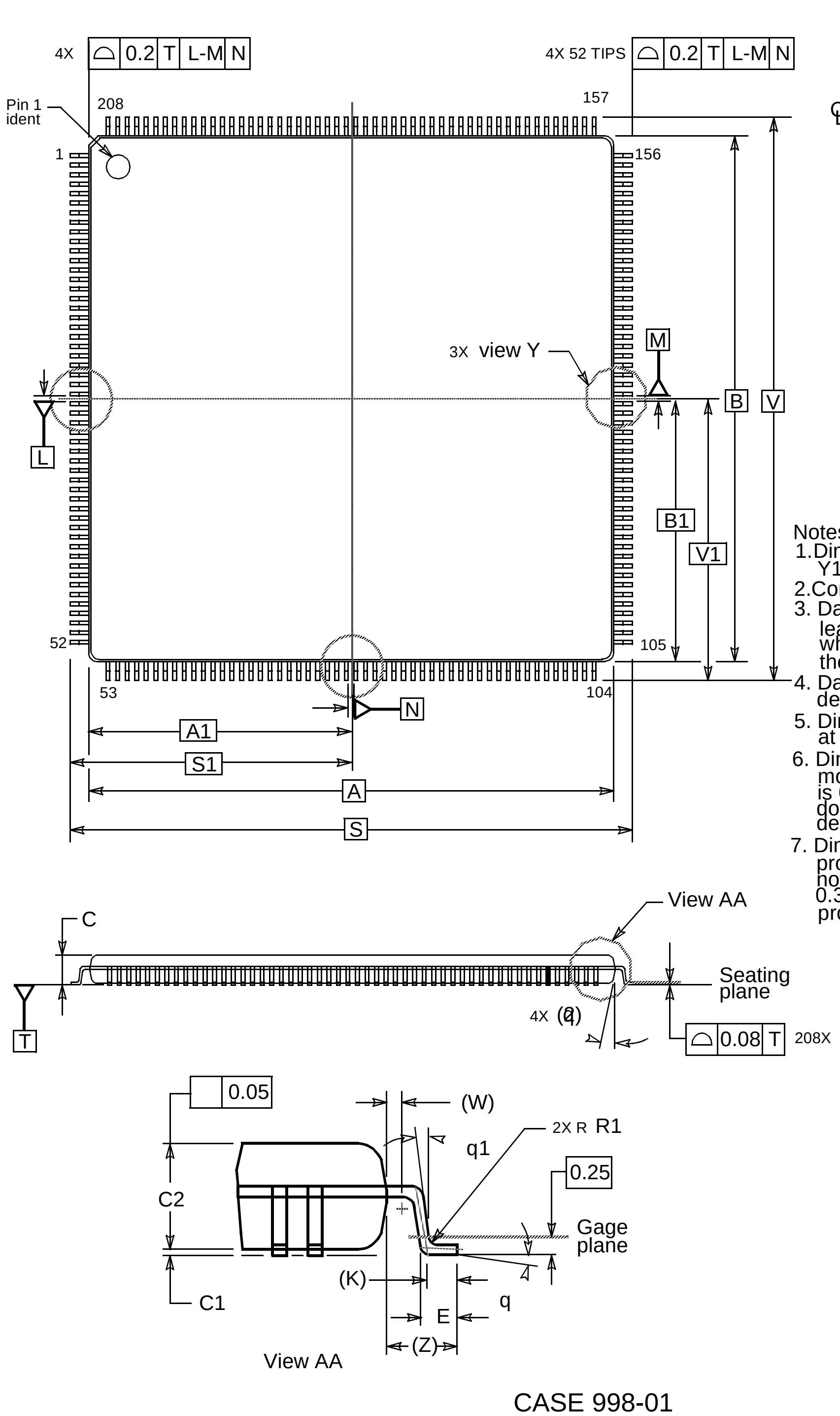
No.	Characteristics[4, 5, 7]	Symbol	Expression	80 MHz		100 MHz		Cond-ition[6]	Unit
				Min	Max	Min	Max		

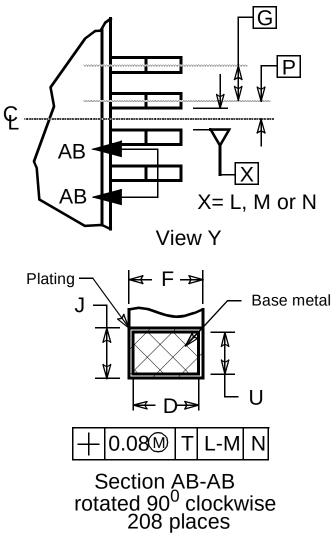
Notes:
1. For the internal clock, the external clock cycle is defined by the instruction cycle time (timing 7 in **Table 2-5** on page 2-6) and the ESSI control register.
2. The word-relative frame sync signal waveform relative to the clock operates the same way as the bit-length frame sync signal waveform, but spreads from one serial clock before the first bit clock (same as Bit Length Frame Sync signal), until the one before the last bit clock of the first word in frame.
3. Periodically sampled and not 100 percent tested
4. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF
5. TXC (SCK Pin) = Transmit Clock
   RXC (SC0 or SCK Pin) = Receive Clock
   FST (SC2 Pin) = Transmit Frame Sync
   FSR (SC1 or SC2 Pin) Receive Frame Sync
6. i ck = Internal Clock
   x ck = External Clock
   i ck a = Internal Clock, Asynchronous Mode
   (Asynchronous implies that TXC and RXC are two different clocks)
   i ck s = Internal Clock, Synchronous Mode
   (Synchronous implies that TXC and RXC are the same clock)
7. bl = bit length
   wl = word length
   wr = word length relative
8. If the DSP core writes to the transmit register during the last cycle before causing an underrun error, the delay is 20 ns + (0.5 × T_C).

Table 3-2. DSP56301 TQFP Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND_N	19	HAD14	152	HAEN	149
GND_P	13	HAD15	151	$\overline{HBE0}$	163
GND_Q	27	HAD16	127	$\overline{HBE1}$	150
GND_Q	78	HAD17	126	$\overline{HBE2}$	128
GND_Q	132	HAD18	125	$\overline{HBE3}$	117
GND_Q	183	HAD19	124	$\overline{HBS}$	140
GND_Q	183	HAD2	171	HC0	163
GND_S	180	HAD20	121	HC1	150
GND_S	194	HAD21	120	HC2	128
HA0	163	HAD22	119	HC3	117
HA1	150	HAD23	118	HCLK	148
HA10	164	HAD24	116	HD0	162
HA2	128	HAD25	115	HD1	161
HA3	173	HAD26	114	HD10	125
HA4	172	HAD27	113	HD11	124
HA5	171	HAD28	110	HD12	121
HA6	170	HAD29	109	HD13	120
HA7	167	HAD3	170	HD14	119
HA8	166	HAD30	108	HD15	118
HA9	165	HAD31	107	HD16	116
HAD0	173	HAD4	167	HD17	115
HAD1	172	HAD5	166	HD18	114
HAD10	160	HAD6	165	HD19	113
HAD11	159	HAD7	164	HD2	160
HAD12	154	HAD8	162	HD20	110
HAD13	153	HAD9	161	HD21	109

3.2 TQFP Package Mechanical Drawing





Notes:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Datum plane **-H-** is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
4. Datums **-L-**, **-M-**, and **-N-** to be determined at datum plane **-H-**.
5. Dimensions **S** and **V** to be determined at seating place **-T-**.
6. Dimensions **A** and **B** do not include mold protrusion. Allowable protrusion is 0.25 per side. Dimensions **A** and **B** do include mold mismatch and are determined at datum plane **-H-**.
7. Dimension d does not include dambar protrusion. Dambar protrusion shall not cause the lead width to exceed 0.35 minimum space between protrusion and adjacent lead 0.07.

	Millimeters	
DIM	MIN	MAX
A	28.00 BSC	
A1	14.00 BSC	
B	28.00 BSC	
B1	14.00 BSC	
C	---	1.60
C1	0.05	---
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.10	0.20
S	30.00 BSC	
S1	15.00 BSC	
U	0.09	0.16
V	30.00 REF	
V1	15.00 REF	
W	0.20 REF	
Z	1.00 REF	
q	0	7
q1	0	---
q2	12 REF	

Figure 3-3. DSP56301 Mechanical Information, 208-pin TQFP Package

Table 3-3. DSP56301 MAP-BGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
E14	MODA/$\overline{IRQA}$	G7	GND	H16	D8
E15	D22	G8	GND	J1	SC11 or PD1
E16	D21	G9	GND	J2	SC12 or PD2
F1	HAD1, HA4, or PB1	G10	GND	J3	TXD or PE1
F2	HAD0, HA3, or PB0	G11	GND	J4	SC10 or PD0
F3	HAD3, HA6, or PB3	G12	V_{CC}	J5	V_{CC}
F4	V_{CC}	G13	D12	J6	GND
F5	V_{CC}	G14	D15	J7	GND
F6	GND	G15	D16	J8	GND
F7	GND	G16	D14	J9	GND
F8	GND	H1	SCLK or PE2	J10	GND
F9	GND	H2	$\overline{HINTA}$	J11	GND
F10	GND	H3	TIO0	J12	V_{CC}
F11	GND	H4	V_{CC}	J13	V_{CC}
F12	V_{CC}	H5	V_{CC}	J14	D5
F13	D18	H6	GND	J15	D10
F14	D19	H7	GND	J16	D7
F15	D20	H8	GND	K1	STD1 or PD5
F16	D17	H9	GND	K2	SCK1 or PD3
G1	TIO1	H10	GND	K3	SCK0 or PC3
G2	RXD or PE0	H11	GND	K4	SRD0 or PC4
G3	TIO2	H12	V_{CC}	K5	V_{CC}
G4	V_{CC}	H13	D11	K6	GND
G5	V_{CC}	H14	D9	K7	GND
G6	GND	H15	D13	K8	GND

Table 3-4. DSP56301 MAP-BGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND	H7	HA10	D2	HAD23	A11
GND	H8	HA2	B9	HAD24	A12
GND	H9	HA3	F2	HAD25	B12
GND	J10	HA4	F1	HAD26	C12
GND	J11	HA5	E1	HAD27	A13
GND	J6	HA6	F3	HAD28	D12
GND	J7	HA7	E2	HAD29	B13
GND	J8	HA8	D1	HAD3	F3
GND	J9	HA9	E3	HAD30	A14
GND	K10	HAD0	F2	HAD31	B14
GND	K11	HAD1	F1	HAD4	E2
GND	K6	HAD10	D4	HAD5	D1
GND	K7	HAD11	C2	HAD6	E3
GND	K8	HAD12	C3	HAD7	D2
GND	K9	HAD13	C4	HAD8	C1
GND	L10	HAD14	B3	HAD9	D3
GND	L11	HAD15	A3	HAEN	B4
GND	L6	HAD16	A8	$\overline{HBE0}$	E4
GND	L7	HAD17	A9	$\overline{HBE1}$	C5
GND	L8	HAD18	C9	$\overline{HBE2}$	B9
GND	L9	HAD19	B10	$\overline{HBE3}$	C11
GND_{P1}	T6	HAD2	E1	$\overline{HBS}$	C7
GND_{P}	P6	HAD20	A10	HC0	E4
HA0	E4	HAD21	C10	HC1	C5
HA1	C5	HAD22	B11	HC2	B9

Table 3-4. DSP56301 MAP-BGA Signal Identification by Name (Continued)

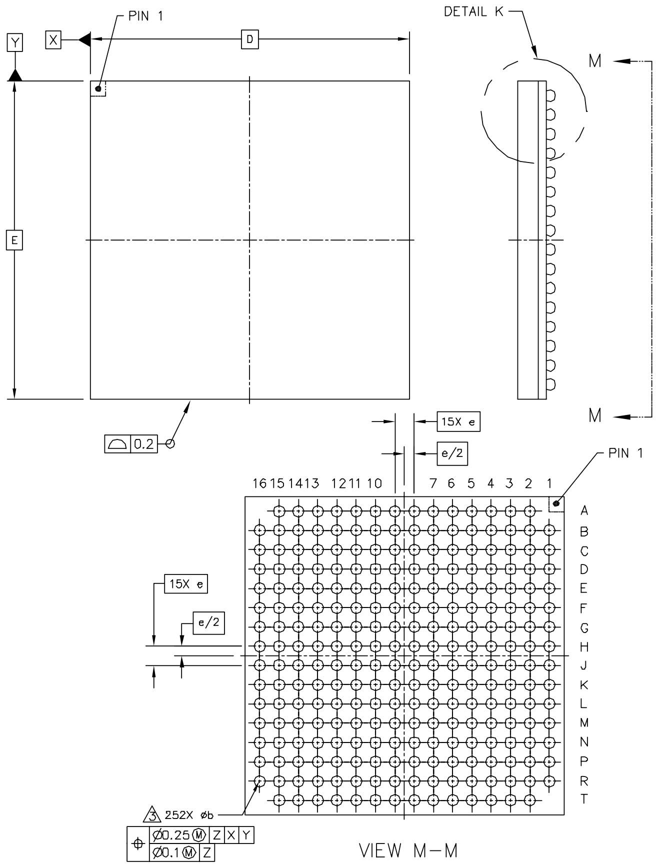
Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
NC	R15	PB6	E3	$\overline{RAS3}$	P8
NC	R16	PB7	D2	$\overline{RD}$	T9
NC	T2	PB8	C1	$\overline{RESET}$	T4
NC	T15	PB9	D3	RXD	G2
$\overline{NMI}$	P5	PC0	M1	SC00	M1
PB0	F2	PC1	L4	SC01	L4
PB1	F1	PC2	L3	SC02	L3
PB10	D4	PC3	K3	SC10	J4
PB11	C2	PC4	K4	SC11	J1
PB12	C3	PC5	L2	SC12	J2
PB13	C4	PCAP	T5	SCK0	K3
PB14	B3	PD0	J4	SCK1	K2
PB15	A3	PD1	J1	SCLK	H1
PB16	E4	PD2	J2	SRD0	K4
PB17	C5	PD3	K2	SRD1	L1
PB18	B9	PD4	L1	STD0	L2
PB19	C11	PD5	K1	STD1	K1
PB2	E1	PE0	G2	$\overline{TA}$	N5
PB20	D8	PE1	J3	TCK	N1
PB21	A7	PE2	H1	TDI	N2
PB22	B7	PINIT	P5	TDO	M3
PB23	C7	PVCL	D6	TIO0	H3
PB3	F3	$\overline{RAS0}$	P3	TIO1	G1
PB4	E2	$\overline{RAS1}$	R3	TIO2	G3
PB5	D1	$\overline{RAS2}$	R7	TMS	M4

Table 3-4. DSP56301 MAP-BGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
$\overline{TRST}$	P1	V_{CC}	F5	V_{CC}	M10
TXD	J3	V_{CC}	G12	V_{CC}	M11
V_{CC}	D10	V_{CC}	G4	V_{CC}	M12
V_{CC}	D11	V_{CC}	G5	V_{CC}	M5
V_{CC}	D5	V_{CC}	H12	V_{CC}	M6
V_{CC}	D9	V_{CC}	H4	V_{CC}	M7
V_{CC}	E10	V_{CC}	H5	V_{CC}	M8
V_{CC}	E11	V_{CC}	J12	V_{CC}	M9
V_{CC}	E12	V_{CC}	J13	V_{CC}	N11
V_{CC}	E13	V_{CC}	J5	V_{CC}	N12
V_{CC}	E5	V_{CC}	K12	V_{CC}	N6
V_{CC}	E6	V_{CC}	K13	V_{CC}	N7
V_{CC}	E7	V_{CC}	K5	V_{CC}	N8
V_{CC}	E8	V_{CC}	L12	V_{CCP}	R5
V_{CC}	E9	V_{CC}	L13	$\overline{WR}$	T8
V_{CC}	F12	V_{CC}	L5	XTAL	R8
V_{CC}	F4				

Note: NC stands for Not Connected. The following pin groups are shorted to each other:
—pins A2, B1, and B2
—pins A15, B15, B16, C14, C15, C16, and D14
—pins N3, R1, R2, and T2
—pins N16, P13, P15, R15, R16, and T15
Do not connect any line, component, trace, or via to these pins.

3.4 MAP-BGA Package Mechanical Drawing



Notes:

1. Dimensions are in millimeters.
2. Interpret dimensions and tolerances per ASME Y14.5M, 1994.
3. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane Z.
4. Datum Z (seating plane) is defined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

	Millimeters	
DIM	MIN	MAX
A	1.6	1.9
A1	0.50	0.70
A2	1.16 REF	
b	0.60	0.90
D	21.00 BSC	
E	21.00 BSC	
e	1.27 BSC	

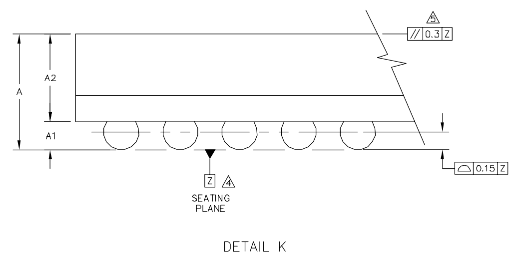


Figure 3-6. DSP56301 Mechanical Information, 252-pin MAP-BGA Package

Power Consumption Benchmark A

The following benchmark program permits evaluation of DSP power usage in a test situation. It enables the PLL, disables the external clock, and uses repeated multiply-accumulate (MAC) instructions with a set of synthetic DSP application data to emulate intensive sustained DSP operation.

```
;**************************************************************************
;**************************************************************************
;*                                                    *
;* CHECKS   Typical Power Consumption                               *
;*                                                  *
;**************************************************************************

       page   200,55,0,0,0
       nolist

I_VEC EQU$000000; Interrupt vectors for program debug only
START EQU$8000 ; MAIN (external) program starting address
INT_PROG EQU$100 ; INTERNAL program memory starting address
INT_XDAT EQU$0 ; INTERNAL X-data memory starting address
INT_YDAT EQU$0 ; INTERNAL Y-data memory starting address

       INCLUDE "ioequ.asm"
       INCLUDE "intequ.asm"

       list

       org    P:START
;
       movep #$0123FF,x:M_BCR; BCR: Area 3 : 1 w.s (SRAM)
; Area 2 : 0 w.s (SSRAM)
; Default: 1 w.s (SRAM)
;
       movep  #$0d0000,x:M_PCTL; XTAL disable
; PLL enable
; CLKOUT disable
;
;Load the program
;
       move   #INT_PROG,r0
       move   #PROG_START,r1
       do     #(PROG_END-PROG_START),PLOAD_LOOP
       move   p:(r1)+,x0
       move   x0,p:(r0)+
       nop
PLOAD_LOOP
;
; Load the X-data
;
       move   #INT_XDAT,r0
       move   #XDAT_START,r1
```

```
        do      #(XDAT_END-XDAT_START),XLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,x:(r0)+
XLOAD_LOOP
;
;Load the Y-data
;
        move    #INT_YDAT,r0
        move    #YDAT_START,r1
        do      #(YDAT_END-YDAT_START),YLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,y:(r0)+
YLOAD_LOOP
;

        jmp     INT_PROG

PROG_START
        move    #$0,r0
        move    #$0,r4
        move    #$3f,m0
        move    #$3f,m4
;
        clr     a
        clr     b
        move    #$0,x0
        move    #$0,x1
        move    #$0,y0
        move    #$0,y1
        bset    #4,omr          ; ebd
;
sbr     dor     #60,_end
        mac     x0,y0,ax:(r0)+,x1     y:(r4)+,y1
        mac     x1,y1,ax:(r0)+,x0     y:(r4)+,y0
        add     a,b
        mac     x0,y0,ax:(r0)+,x1
        mac     x1,y1,a               y:(r4)+,y0
        move    b1,x:$ff
_end
        bra     sbr
        nop
        nop
        nop
        nop
PROG_END
        nop
        nop


XDAT_START
;       org     x:0
        dc      $262EB9
        dc      $86F2FE
        dc      $E56A5F
        dc      $616CAC
        dc      $8FFD75
        dc      $9210A
        dc      $A06D7B
        dc      $CEA798
        dc      $8DFBF1
        dc      $A063D6
```