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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	80MHz
Non-Volatile Memory	ROM (9kB)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	252-BGA
Supplier Device Package	252-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56301vf80

DSP56301	PCI Bus	Universal Bus	Port B GPIO	Host Port (HP) Reference
Host Interface (HI32)/ Port B Signals	HAD0	HA3	PB0	HP0
	HAD1	HA4	PB1	HP1
	HAD2	HA5	PB2	HP2
	HAD3	HA6	PB3	HP3
	HAD4	HA7	PB4	HP4
	HAD5	HA8	PB5	HP5
	HAD6	HA9	PB6	HP6
	HAD7	HA10	PB7	HP7
	HAD8	HD0	PB8	HP8
	HAD9	HD1	PB9	HP9
	HAD10	HD2	PB10	HP10
	HAD11	HD3	PB11	HP11
	HAD12	HD4	PB12	HP12
	HAD13	HD5	PB13	HP13
	HAD14	HD6	PB14	HP14
	HAD15	HD7	PB15	HP15
	HC0/$\overline{\text{HBE0}}$	HA0	PB16	HP16
	HC1/$\overline{\text{HBE1}}$	HA1	PB17	HP17
	HC2/$\overline{\text{HBE2}}$	HA2	PB18	HP18
	HC3/$\overline{\text{HBE3}}$	Tie to pull-up or V_{CC}	PB19	HP19
	$\overline{\text{HTRDY}}$	$\overline{\text{HDBEN}}$	PB20	HP20
	$\overline{\text{HIRDY}}$	$\overline{\text{HDBDR}}$	PB21	HP21
	$\overline{\text{HDEVSEL}}$	$\overline{\text{HSA}}$K	PB22	HP22
	HLOCK	$\overline{\text{HBS}}$	PB23	HP23
	$\overline{\text{HPAR}}$	$\overline{\text{HDAK}}$	Internal disconnect	HP24
	$\overline{\text{HPERR}}$	HDRQ	Internal disconnect	HP25
	$\overline{\text{HGNT}}$	$\overline{\text{HAEN}}$	Internal disconnect	HP26
	$\overline{\text{HREQ}}$	$\overline{\text{HTA}}$	Internal disconnect	HP27
	$\overline{\text{HSERR}}$	$\overline{\text{HIRQ}}$	Internal disconnect	HP28
	HSTOP	$\overline{\text{HWR}}$/$\overline{\text{HRW}}$	Internal disconnect	HP29
	$\overline{\text{HIDSEL}}$	$\overline{\text{HRD}}$/$\overline{\text{HDS}}$	Internal disconnect	HP30
	$\overline{\text{HFRAME}}$	Tie to pull-up or V_{CC}	Internal disconnect	HP31
	HCLK	Tie to pull-up or V_{CC}	Internal disconnect	HP32
	HAD16	HD8	Internal disconnect	HP33
	HAD17	HD9	Internal disconnect	HP34
	HAD18	HD10	Internal disconnect	HP35
	HAD19	HD11	Internal disconnect	HP36
	HAD20	HD12	Internal disconnect	HP37
	HAD21	HD13	Internal disconnect	HP38
	HAD22	HD14	Internal disconnect	HP39
	HAD23	HD15	Internal disconnect	HP40
	HAD24	HD16	Internal disconnect	HP41
	HAD25	HD17	Internal disconnect	HP42
	HAD26	HD18	Internal disconnect	HP43
	HAD27	HD19	Internal disconnect	HP44
	HAD28	HD20	Internal disconnect	HP45
	HAD29	HD21	Internal disconnect	HP46
	HAD30	HD22	Internal disconnect	HP47
	HAD31	HD23	Internal disconnect	HP48
	$\overline{\text{HRST}}$	$\overline{\text{HRST}}$	Internal disconnect	HP49
	HINTA	HINTA	Internal disconnect	HP50
	PVCL	Leave unconnected	Leave unconnected	PVCL

Note: HPxx is a reference only and is not a signal name. GPIO references formerly designated as HIOxx have been renamed PBxx for consistency with other Freescale DSPs.

Figure 1-2. Host Interface/Port B Detail Signal Diagram

Table 1-5. Phase Lock Loop Signals (Continued)

Signal Name	Type	State During Reset	Signal Description
PINIT/$\overline{\text{NMI}}$	Input	Input	**PLL Initial/Non-Maskable Interrupt** During assertion of $\overline{\text{RESET}}$, the value of PINIT/$\overline{\text{NMI}}$ is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After $\overline{\text{RESET}}$ deassertion and during normal instruction processing, the PINIT/$\overline{\text{NMI}}$ Schmitt-trigger input is a negative-edge-triggered Non-Maskable Interrupt (NMI) request internally synchronized to CLKOUT. PINIT/$\overline{\text{NMI}}$ can tolerate 5 V.

1.5 External Memory Expansion Port (Port A)

Note: When the DSP56301 enters a low-power stand-by mode (Stop or Wait), it releases bus mastership and tri-states the relevant Port A signals: A[0–23], D[0–23], AA0/$\overline{\text{RAS0}}$–AA3/$\overline{\text{RAS3}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BB}}$, $\overline{\text{CAS}}$, BCLK, and $\overline{\text{BCLK}}$. If hardware refresh of external DRAM is enabled, Port A exits the Wait mode to allow the refresh to occur and then returns to the Wait mode.

1.5.1 External Address Bus

Table 1-6. External Address Bus Signals

Signal Name	Type	State During Reset	Signal Description
A[0–23]	Output	Tri-stated	**Address Bus** When the DSP is the bus master, A[0–23] specify the address for external program and data memory accesses. Otherwise, the signals are tri-stated. To minimize power dissipation, A[0–23] do not change state when external memory spaces are not being accessed.

1.5.2 External Data Bus

Table 1-7. External Data Bus Signals

Signal Name	Type	State During Reset	Signal Description
D[0–23]	Input/Output	Tri-stated	**Data Bus** When the DSP is the bus master, D[0–23] provide the bidirectional data bus for external program and data memory accesses. Otherwise, D[0–23] are tri-stated.

1.6 Interrupt and Mode Control

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After RESET is deasserted, these inputs are hardware interrupt request lines.

Table 1-9. Interrupt and Mode Control

Signal Name	Type	State During Reset	Signal Description
MODA	Input	Input	**Mode Select A** Selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input IRQA during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the RESET signal is deasserted.
IRQA	Input		**External Interrupt Request A** Internally synchronized to CLKOUT. If IRQA is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting IRQA to exit the Wait state. If the processor is in the Stop stand-by state and IRQA is asserted, the processor exits the Stop state. These inputs are 5 V tolerant.
MODB	Input	Input	**Mode Select B** Selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input IRQB during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the RESET signal is deasserted.
IRQB	Input		**External Interrupt Request B** Internally synchronized to CLKOUT. If IRQB is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting IRQB to exit the Wait state. If the processor is in the Stop stand-by state and IRQC is asserted, the processor will exit the Stop state. These inputs are 5 V tolerant.
MODC	Input	Input	**Mode Select C** Selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input IRQC during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the RESET signal is deasserted.
IRQC	Input		**External Interrupt Request C** Internally synchronized to CLKOUT. If IRQC is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting IRQC to exit the Wait state. If the processor is in the Stop stand-by state and IRQC is asserted, the processor exits the Stop state. These inputs are 5 V tolerant.

Table 1-11. Host Interface (Continued)

Signal Name	Type	State During Reset	Signal Description
$\overline{\text{HSERR}}$	Output, open drain	Tri-stated	**Host System Error** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host System Error signal.
$\overline{\text{HIRQ}}$	Output, open drain		**Host Interrupt Request** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Interrupt Request signal. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
$\overline{\text{HSTOP}}$	Input/ Output	Tri-stated	**Host Stop** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Stop signal.
$\overline{\text{HWR}}$/HRW	Input		**Host Write/Host Read-Write** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Write/Host Read-Write Schmitt-trigger signal. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
HIDSEL	Input	Input	**Host Initialization Device Select** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Initialization Device Select signal.
$\overline{\text{HRD}}$/$\overline{\text{HDS}}$	Input		**Host Read/Host Data Strobe** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Data Read/Host Data Strobe Schmitt-trigger signal. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
$\overline{\text{HFRAME}}$	Input/ Output	Tri-stated	**Host Frame** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host cycle Frame signal. **Non-PCI bus** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this signal must be connected to a pull-up resistor or directly to V_{CC}. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.

Table 1-11. Host Interface (Continued)

Signal Name	Type	State During Reset	Signal Description
HCLK	Input	Input	**Host Clock** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Bus Clock input. **Non-PCI bus** When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal must be connected to a pull-up resistor or directly to V_{CC}. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
HAD[16–31] HD[8–23]	Input/Output Input/Output	Tri-stated	**Host Address/Data 16–31** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, these signals are lines 16–31 of the Address/Data bus. **Host Data 8–23** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, these signals are lines 8–23 of the Data bus. **Port B** When the HI32 is configured as GPIO through the DCTR, these signals are internally disconnected. These inputs are 5 V tolerant.
$\overline{\text{HRST}}$ HRST	Input Input	Tri-stated	**Hardware Reset** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Hardware Reset input. **Hardware Reset** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Hardware Reset Schmitt-trigger signal. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
$\overline{\text{HINTA}}$	Output, open drain	Tri-stated	**Host Interrupt A** When the HI function is selected, this signal is the Interrupt A open-drain output. **Port B** When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected. This input is 5 V tolerant.
PVCL	Input	Input	**PCI Voltage Clamp** When the HI32 is programmed to interface with a PCI bus and the HI function is selected and the PCI bus uses a 3 V signal environment, connect this pin to V_{CC} (3.3 V) to enable the high voltage clamping required by the PCI specifications. In all other cases, including a 5 V PCI signal environment, leave the input unconnected.

Table 2-5. Clock Operation

No.	Characteristics	Symbol	80 MHz		100 MHz	
			Min	Max	Min	Max
1	Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 3 ns maximum.	Ef	0	80.0 MHz	0	100.0 MHz
2	EXTAL input high[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_H	 5.84 ns 5.31 ns	 ∞ 157.0 µs	 4.67 ns 4.25 ns	 ∞ 157.0 µs
3	EXTAL input low[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_L	 5.84 ns 5.31 ns	 ∞ 157.0 µs	 4.67 ns 4.25 ns	 ∞ 157.0 µs
4	EXTAL cycle time[2] • With PLL disabled • With PLL enabled	ET_C	 12.50 ns 12.50 ns	 ∞ 273.1 µs	 10.00 ns 10.00 ns	 ∞ 273.1 µs
5	CLKOUT change from EXTAL fall with PLL disabled		4.3 ns	11.0 ns	4.3 ns	11.0 ns
6	a. CLKOUT rising edge from EXTAL rising edge with PLL enabled (MF = 1 or 2 or 4, PDF = 1, Ef > 15 MHz)[3,5] b. CLKOUT falling edge from EXTAL falling edge with PLL enabled (MF ≤ 4, PDF ≠ 1, Ef / PDF > 15 MHz)[3,5]		0.0 ns 0.0 ns	1.8 ns 1.8 ns	0.0 ns 0.0 ns	1.8 ns 1.8 ns
7	Instruction cycle time = $I_{CYC} = T_C$[4] (see **Table 2-4**) (46.7%–53.3% duty cycle) • With PLL disabled • With PLL enabled	I_{CYC}	 25.0 ns 12.50 ns	 ∞ 8.53 µs	 20.0 ns 10.00 ns	 ∞ 8.53 µs

Notes:
1. Measured at 50 percent of the input transition
2. The maximum value for PLL enabled is given for minimum VCO frequency (see **Table 2-6**) and maximum MF.
3. Periodically sampled and not 100 percent tested
4. The maximum value for PLL enabled is given for minimum VCO frequency and maximum DF.
5. The skew is not guaranteed for any other MF value.
6. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correction operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

2.5.3 Phase Lock Loop (PLL) Characteristics

Table 2-6. PLL Characteristics

Characteristics	80 MHz		100 MHz		Unit
	Min	Max	Min	Max	
Voltage Controlled Oscillator (VCO) frequency when PLL enabled (MF × E_f × 2/PDF)	30	160	30	200	MHz
PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP}) • @ MF ≤ 4 • @ MF > 4	 (MF × 580) – 100 MF × 830	 (MF × 780) – 140 MF × 1470	 (MF × 580) – 100 MF × 830	 (MF × 780) – 140 MF × 1470	 pF pF

Note: C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}). The recommended value in pF for C_{PCAP} can be computed from one of the following equations:
(680 × MF) – 120, for MF ≤ 4, or
1100 × MF, for MF > 4.

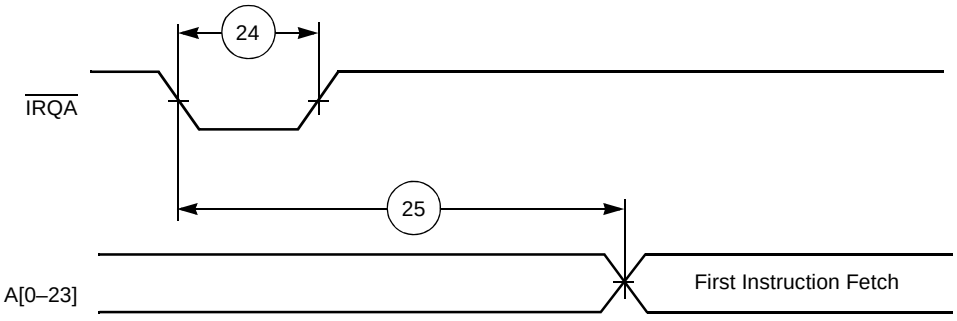


Figure 2-9. Recovery from Stop State Using $\overline{\text{IRQA}}$

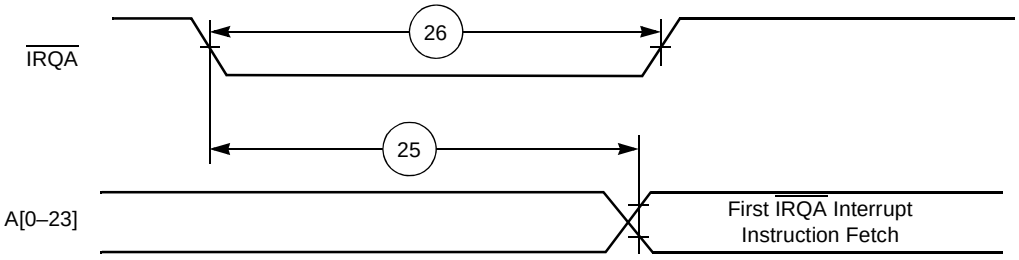


Figure 2-10. Recovery from Stop State Using $\overline{\text{IRQA}}$ Interrupt Service

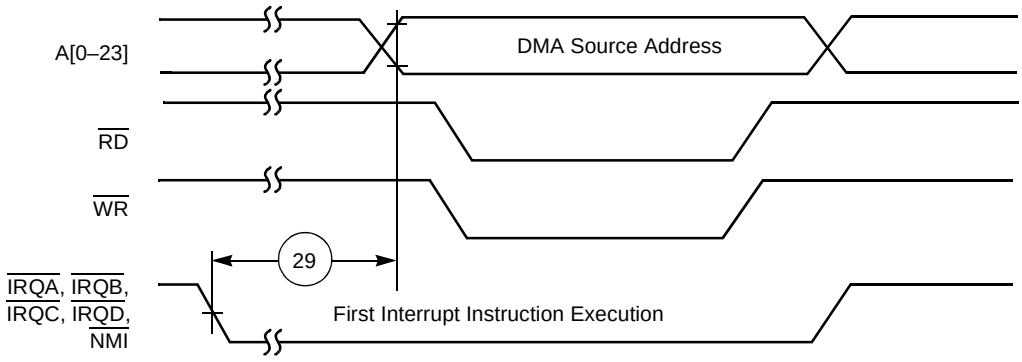
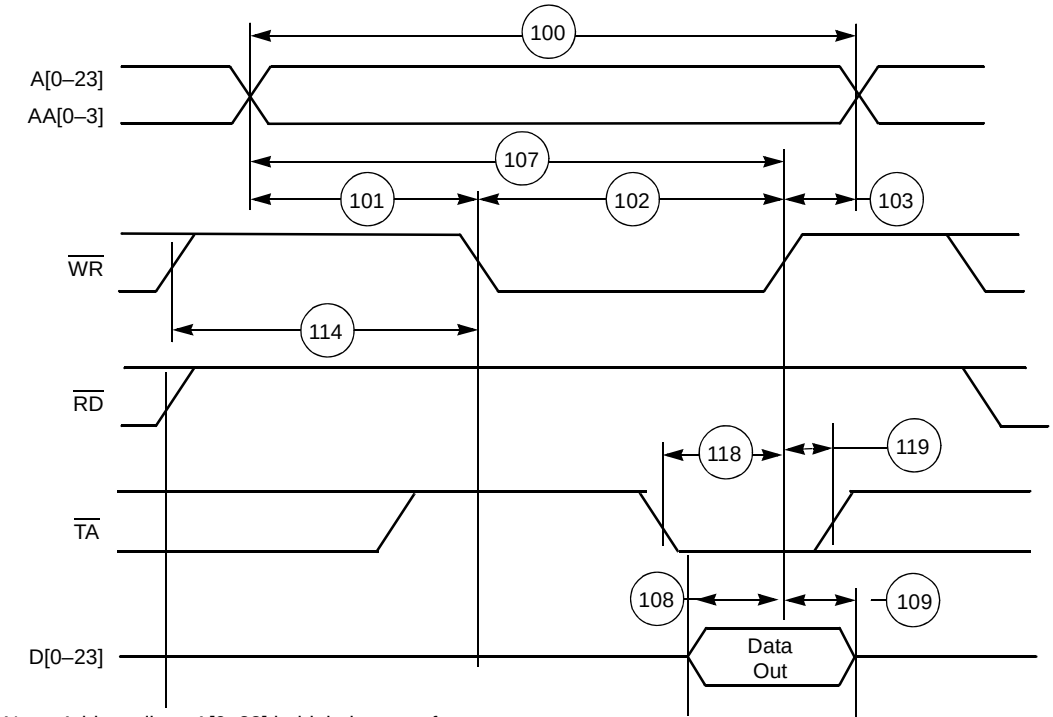


Figure 2-11. External Memory Access (DMA Source) Timing

2.5.5 External Memory Expansion Port (Port A)



Note: Address lines A[0–23] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-13. SRAM Write Access

2.5.5.2 DRAM Timing

The selection guides in **Figure 2-14** and **Figure 2-17** are for primary selection only. Final selection should be based on the timing in the following tables. For example, the selection guide suggests that four wait states must be used for 100 MHz operation in Page Mode DRAM. However, using the information in the appropriate table, a designer could choose to evaluate whether fewer wait states might be used by determining which timing prevents operation at 100 MHz, by running the chip at a slightly lower frequency (for example, 95 MHz), by using faster DRAM (if it becomes available), and by manipulating control factors such as capacitive and resistive load to improve overall system performance.

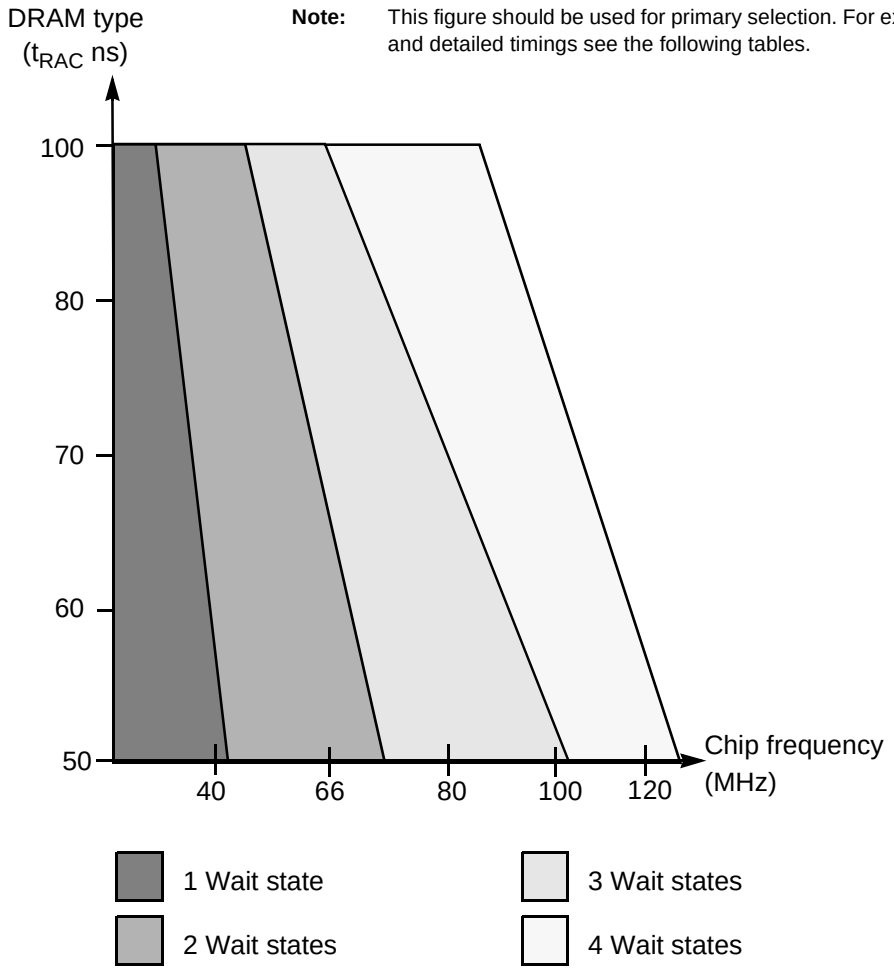


Figure 2-14. DRAM Page Mode Wait States Selection Guide

Table 2-9. DRAM Page Mode Timings, Two Wait States[1, 2, 3, 7]

No.	Characteristics	Symbol	Expression	80 MHz		Unit
				Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction		$3 \times T_C$	37.5	—	ns
	Page mode cycle time for mixed (read and write) accesses	t_{PC}	$2.75 \times T_C$	34.4	—	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$1.5 \times T_C - 6.5$	—	12.3	ns
133	Column address valid to data valid (read)	t_{AA}	$2.5 \times T_C - 6.5$	—	24.8	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$1.75 \times T_C - 4.0$	17.9	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$3.25 \times T_C - 4.0$	36.6	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$1.5 \times T_C - 4.0$	14.8	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[5] BRW[1–0] = 00 BRW[1–0] = 01 BRW[1–0] = 10 BRW[1–0] = 11	t_{CRP}	 Not supported $3.5 \times T_C - 6.0$ $4.5 \times T_C - 6.0$ $6.5 \times T_C - 6.0$	 — 37.8 50.3 75.3	 — — — —	 ns ns ns ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.25 \times T_C - 4.0$	11.6	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	8.5	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$1.75 \times T_C - 4.0$	17.9	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$3 \times T_C - 4.0$	33.5	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 4$	11.6	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.5 \times T_C - 3.7$	2.6	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$1.5 \times T_C - 4.2$	14.6	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$2.5 \times T_C - 4.5$	26.8	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$2.75 \times T_C - 4.3$	30.1	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$2.5 \times T_C - 4.3$	27.0	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.25 \times T_C - 3.0$	0.1	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$1.75 \times T_C - 4.0$	17.9	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$T_C - 4.3$	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$2.5 \times T_C - 4.0$	27.3	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$1.75 \times T_C - 6.5$	—	15.4	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 1.5$	7.9	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.1	ns

Notes:
1. The number of wait states for Page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for the DSP56301.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (for example, t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1–0] (DRAM Control Register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
6. $\overline{RD}$ deassertion always occurs after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
7. At this time, there are no DRAMs fast enough to fit with two wait states Page mode @ 100MHz (see **Table 2-14**). However, DRAM speeds are approaching two-wait-state compatibility.

Table 2-10. DRAM Page Mode Timings, Three Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction		$4 \times T_C$	50.0	—	40.0	—	ns
	Page mode cycle time for mixed (read and write) accesses	t_{PC}	$3.5 \times T_C$	43.7	—	35.0	—	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$2 \times T_C - 5.7$	—	19.3	—	14.3	ns
133	Column address valid to data valid (read)	t_{AA}	$3 \times T_C - 5.7$	—	31.8	—	24.3	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$2.5 \times T_C - 4.0$	27.3	—	21.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$4.5 \times T_C - 4.0$	52.3	—	41.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2 \times T_C - 4.0$	21.0	—	16.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion[5] • BRW[1–0] = 00 • BRW[1–0] = 01 • BRW[1–0] = 10 • BRW[1–0] = 11	t_{CRP}	 Not supported $3.75 \times T_C - 6.0$ $4.75 \times T_C - 6.0$ $6.75 \times T_C - 6.0$	 — 40.9 53.4 78.4	 — — — —	 — 31.5 41.5 61.5	 — — — —	 ns ns ns ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.5 \times T_C - 4.0$	14.8	—	11.0	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	8.5	—	6.0	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$2.5 \times T_C - 4.0$	27.3	—	21.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	46.0	—	36.0	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 4.0$	11.6	—	8.5	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.75 \times TC - 4.0$	5.4	—	3.5	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$2.25 \times T_C - 4.2$	23.9	—	18.3	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$3.5 \times T_C - 4.5$	39.3	—	30.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$3.75 \times T_C - 4.3$	42.6	—	33.2	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.25 \times T_C - 4.3$	36.3	—	28.2	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.8$	2.0	—	0.2	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$2.5 \times T_C - 4.0$	27.3	—	21.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	11.3	—	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$3.5 \times T_C - 4.0$	39.8	—	31.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$2.5 \times T_C - 5.7$	—	25.6	—	19.3	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 1.5$	7.9	—	6.0	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for Page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56301.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (for example, t_{PC} equals $4 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1–0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of page-access.
6. $\overline{RD}$ deassertion always occurs after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

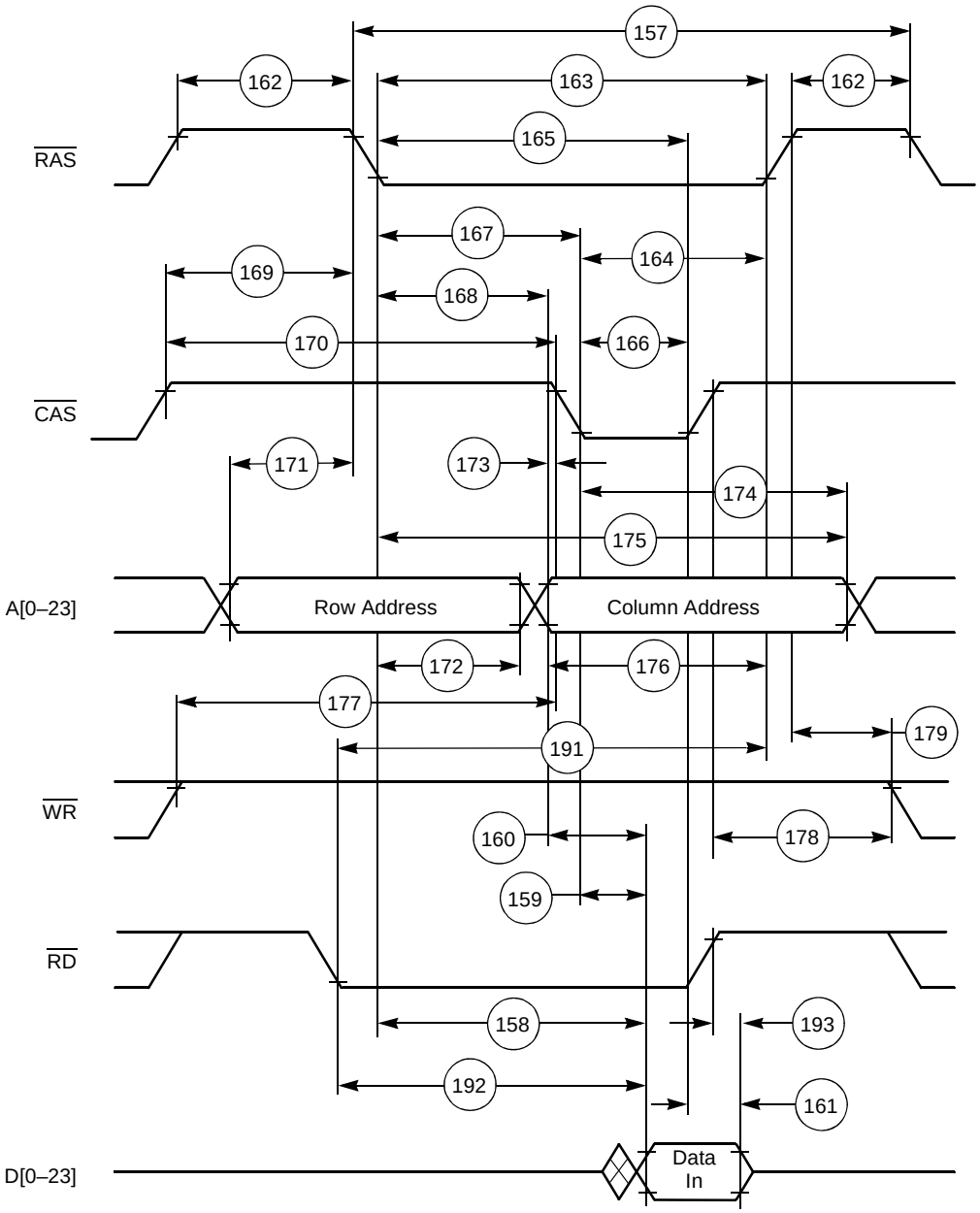
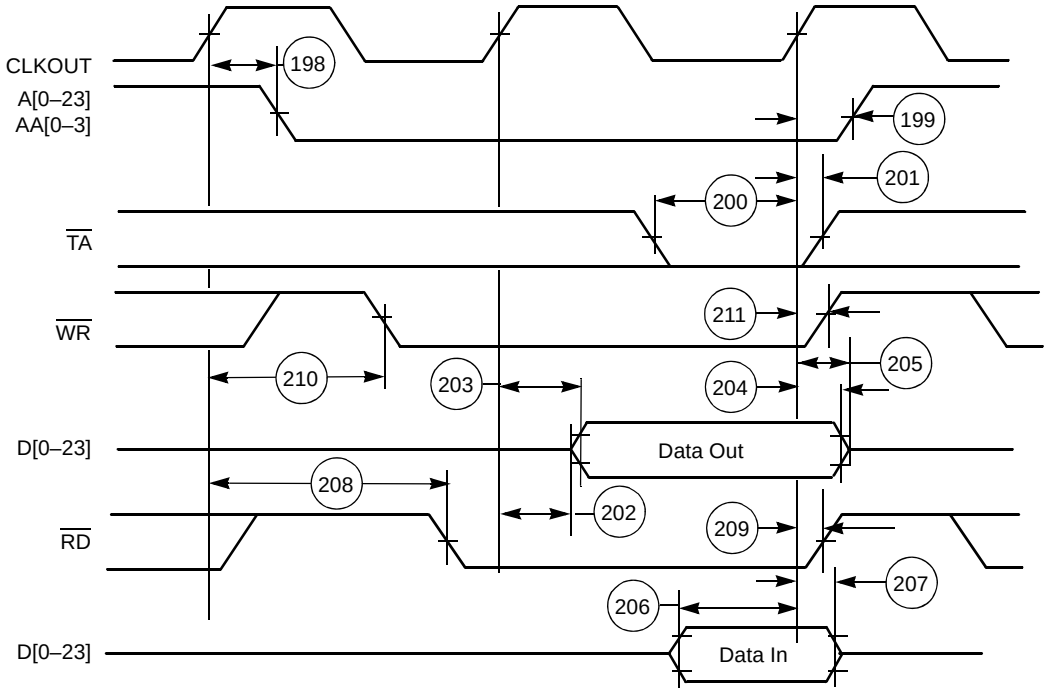
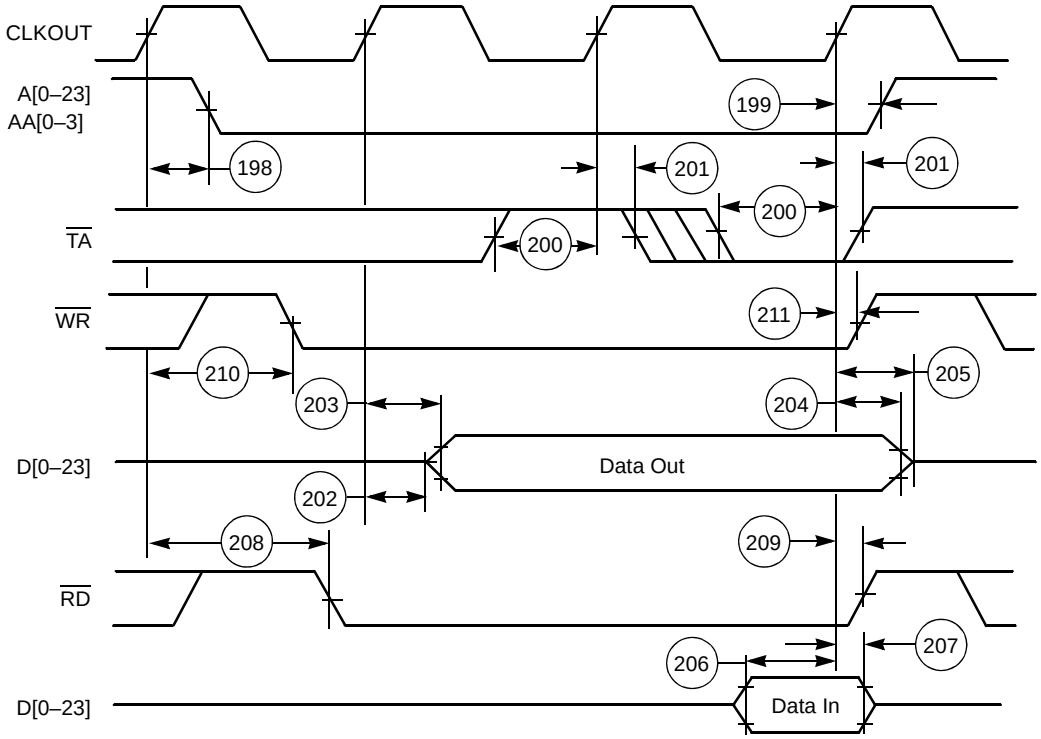


Figure 2-18. DRAM Out-of-Page Read Access



Note: Address lines A[0–23] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-21. Synchronous Bus Timings 1 WS (BCR Controlled)



Note: Address lines A[0–23] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-22. Synchronous Bus Timings 2 WS ($\overline{TA}$ Controlled)

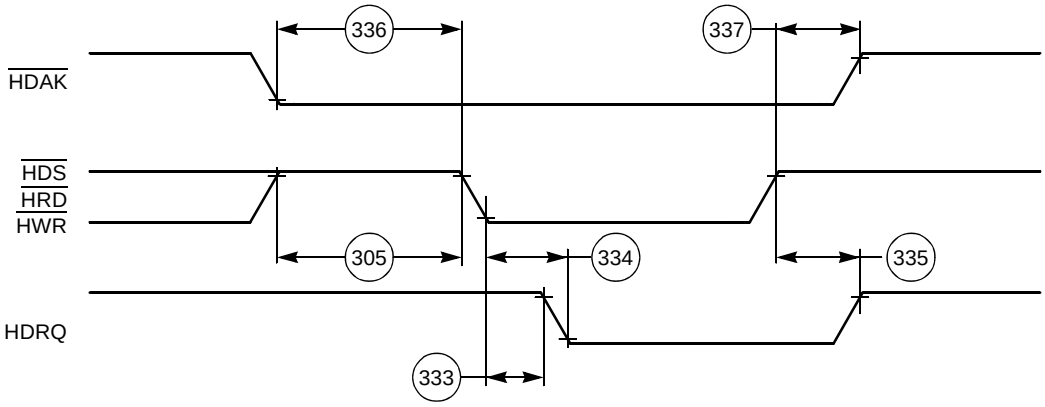


Figure 2-28. Universal Bus Mode DMA Access Timing

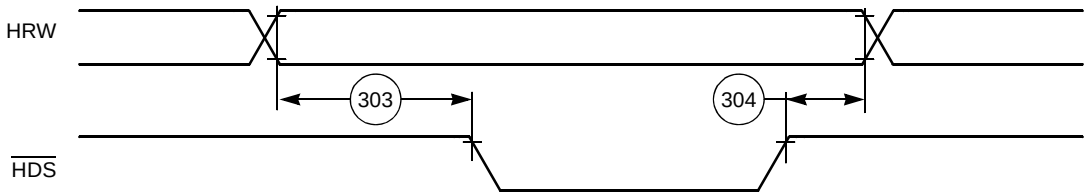


Figure 2-29. HRW to HDS Timing

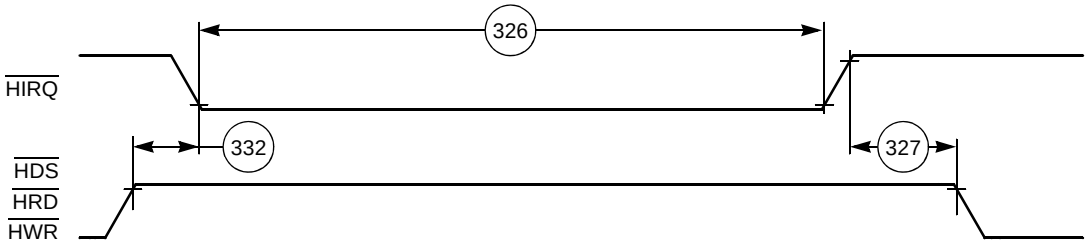


Figure 2-30. HIRQ Pulse Width (HIRH = 0)

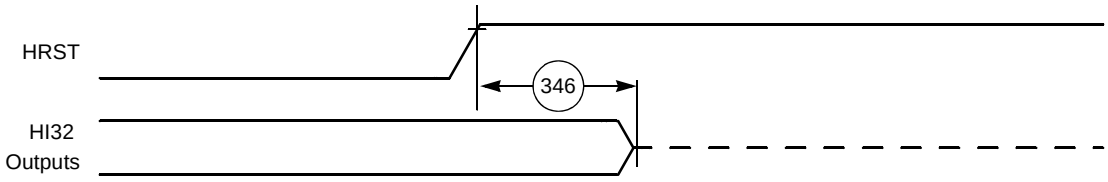


Figure 2-31. HRST Timing

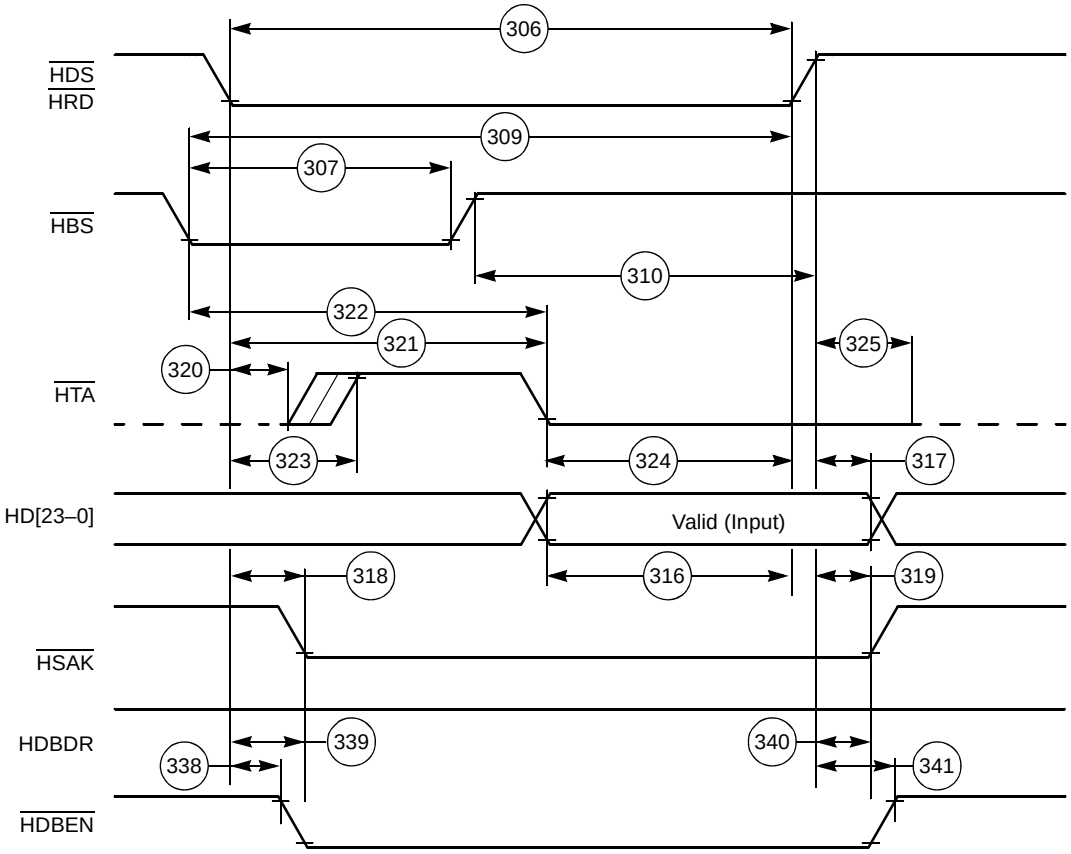


Figure 2-33. Write Timing

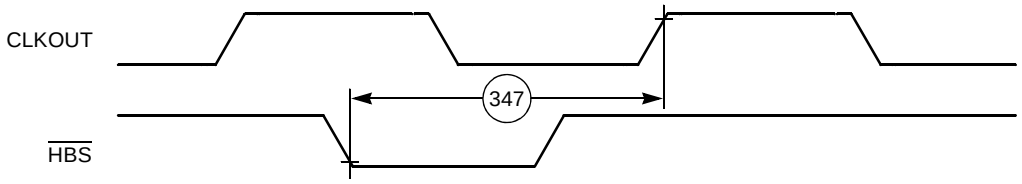


Figure 2-34. $\overline{\text{HBS}}$ Synchronous Timing

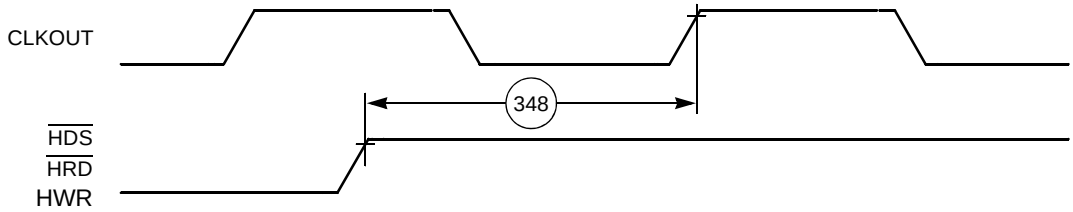


Figure 2-35. Data Strobe Synchronous Timing

3.1 TQFP Package Description

Top and bottom views of the TQFP package are shown in **Figure 3-1** and **Figure 3-2** with their pin-outs.

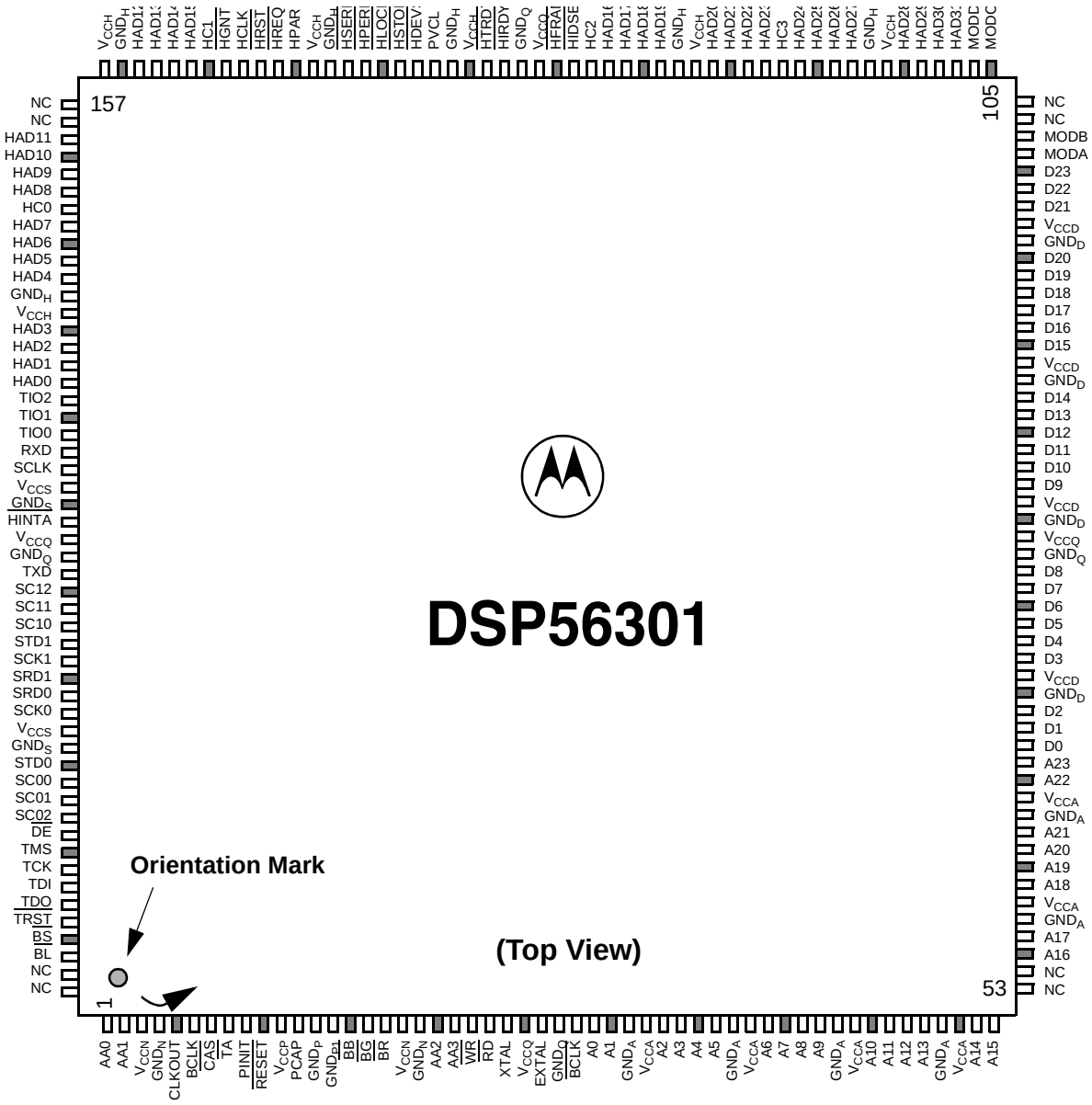
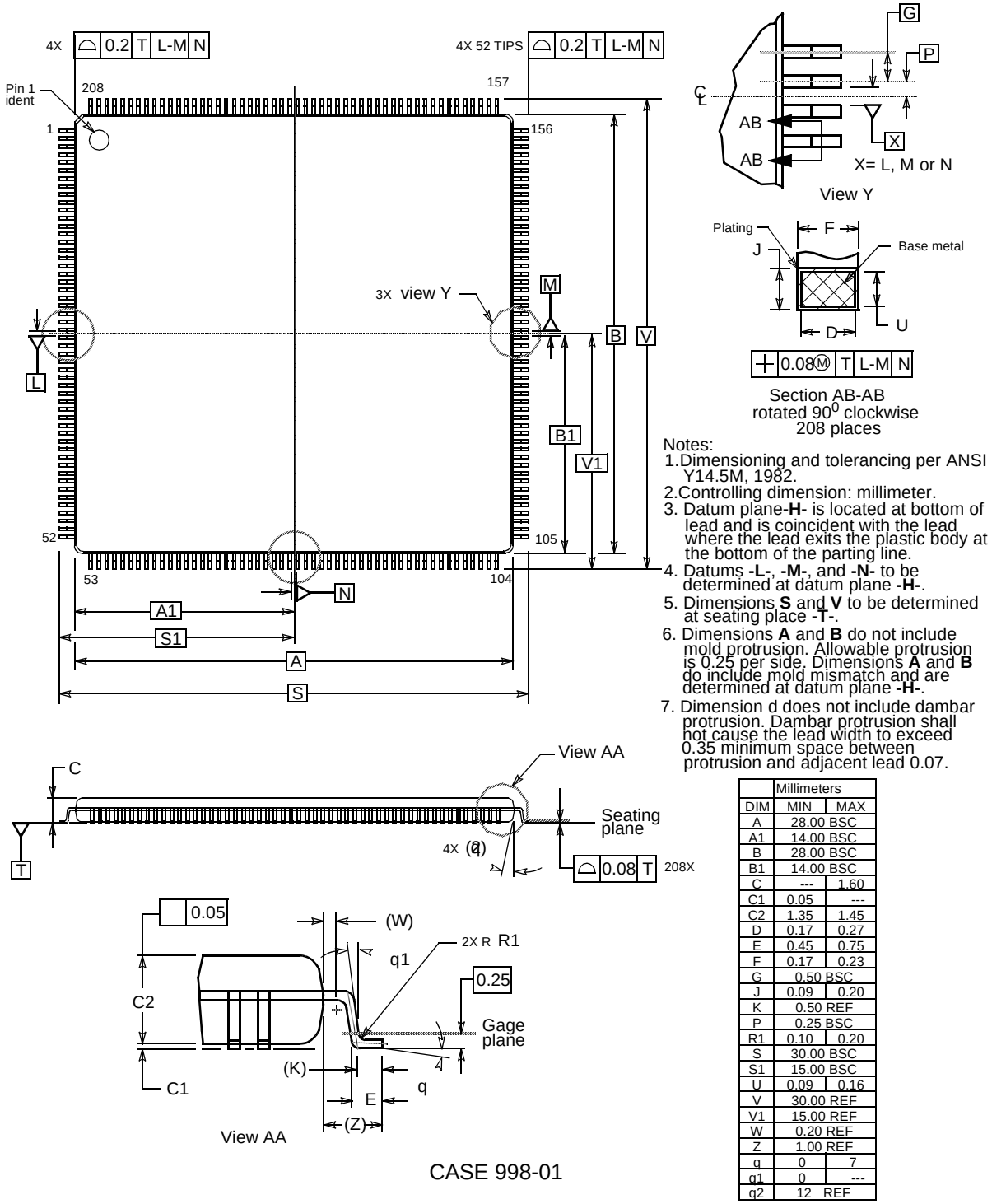


Figure 3-1. DSP56301 Thin Quad Flat Pack (TQFP), Top View

3.2 TQFP Package Mechanical Drawing



Notes:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Datum plane **-H-** is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
4. Datums **-L-**, **-M-**, and **-N-** to be determined at datum plane **-H-**.
5. Dimensions **S** and **V** to be determined at seating place **-T-**.
6. Dimensions **A** and **B** do not include mold protrusion. Allowable protrusion is 0.25 per side. Dimensions **A** and **B** do include mold mismatch and are determined at datum plane **-H-**.
7. Dimension d does not include dambar protrusion. Dambar protrusion shall not cause the lead width to exceed 0.35 minimum space between protrusion and adjacent lead 0.07.

	Millimeters	
DIM	MIN	MAX
A	28.00 BSC	
A1	14.00 BSC	
B	28.00 BSC	
B1	14.00 BSC	
C	---	1.60
C1	0.05	---
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.10	0.20
S	30.00 BSC	
S1	15.00 BSC	
U	0.09	0.16
V	30.00 REF	
V1	15.00 REF	
W	0.20 REF	
Z	1.00 REF	
q	0	7
q1	0	---
q2	12 REF	

Figure 3-3. DSP56301 Mechanical Information, 208-pin TQFP Package

Table 3-3. DSP56301 MAP-BGA Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A2	NC	B12	HAD25 or HD17	D5	V_{CC}
A3	HAD15, HD7, or PB15	B13	HAD29 or HD21	D6	PVCL
A4	HCLK	B14	HAD31 or HD23	D7	$\overline{\text{HSTOP}}$ or $\overline{\text{HWR}}$/HRW
A5	HPAR or $\overline{\text{HDAK}}$	B15	NC	D8	$\overline{\text{HTRDY}}$, $\overline{\text{HDBEN}}$, or PB20
A6	$\overline{\text{HPERR}}$ or HDRQ	B16	NC	D9	V_{CC}
A7	$\overline{\text{HIRDY}}$, $\overline{\text{HDBDR}}$, or PB21	C1	HAD8, HD0, or PB8	D10	V_{CC}
A8	HAD16 or HD8	C2	HAD11, HD3, or PB11	D11	V_{CC}
A9	HAD17 or HD9	C3	HAD12, HD4, or PB12	D12	HAD28 or HD20
A10	HAD20 or HD12	C4	HAD13, HD5, or PB13	D13	MODC/$\overline{\text{IRQC}}$
A11	HAD23 or HD15	C5	HC1/$\overline{\text{HBE1}}$, HA1, or PB17	D14	NC
A12	HAD24 or HD16	C6	$\overline{\text{HREQ}}$ or $\overline{\text{HTA}}$	D15	MODB/$\overline{\text{IRQB}}$
A13	HAD27 or HD19	C7	$\overline{\text{HLOCK}}$, $\overline{\text{HBS}}$, or PB23	D16	D23
A14	HAD30 or HD22	C8	$\overline{\text{HFRAME}}$	E1	HAD2, HA5, or PB2
A15	NC	C9	HAD18 or HD10	E2	HAD4, HA7, or PB4
B1	NC	C10	HAD21 or HD13	E3	HAD6, HA9, or PB6
B2	NC	C11	HC3/$\overline{\text{HBE3}}$ or PB19	E4	HC0/$\overline{\text{HBE0}}$, HA0, or PB16
B3	HAD14, HD6, or PB14	C12	HAD26 or HD18	E5	V_{CC}
B4	$\overline{\text{HGNT}}$ or HAEN	C13	MODD/$\overline{\text{IRQD}}$	E6	V_{CC}
B5	$\overline{\text{HRST}}$/HRST	C14	NC	E7	V_{CC}
B6	$\overline{\text{HSERR}}$ or $\overline{\text{HIRQ}}$	C15	NC	E8	V_{CC}
B7	$\overline{\text{HDEVSEL}}$, $\overline{\text{HSAK}}$, or PB22	C16	NC	E9	V_{CC}
B8	HIDSEL or $\overline{\text{HRD}}$/$\overline{\text{HDS}}$	D1	HAD5, HA8, or PB5	E10	V_{CC}
B9	HC2/$\overline{\text{HBE2}}$, HA2, or PB18	D2	HAD7, HA10, or PB7	E11	V_{CC}
B10	HAD19 or HD11	D3	HAD9, HD1, or PB9	E12	V_{CC}
B11	HAD22 or HD14	D4	HAD10, HD2, or PB10	E13	V_{CC}

Table 3-3. DSP56301 MAP-BGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
R4	$\overline{\text{CAS}}$	R13	A11	T7	$\overline{\text{BR}}$
R5	V_{CCP}	R14	A14	T8	$\overline{\text{WR}}$
R6	$\overline{\text{BB}}$	R15	NC	T9	$\overline{\text{RD}}$
R7	AA2/$\overline{\text{RAS2}}$	R16	NC	T10	A0
R8	XTAL	T2	NC	T11	A4
R9	$\overline{\text{BCLK}}$	T3	BCLK	T12	A7
R10	A3	T4	$\overline{\text{RESET}}$	T13	A10
R11	A6	T5	PCAP	T14	A13
R12	A9	T6	GND_{P1}	T15	NC

Notes:

1. Signal names are based on configured functionality. Most connections supply a single signal. Some connections provide a signal with dual functionality, such as the MODx/$\overline{\text{IRQx}}$ pins that select an operating mode after $\overline{\text{RESET}}$ is deasserted, but act as interrupt lines during operation. Some signals have configurable polarity; these names are shown with and without overbars, such as $\overline{\text{HAS}}$/HAS. Some connections have two or more configurable functions; names assigned to these connections indicate the function for a specific configuration. For example, connection N2 is data line H7 in non-multiplexed bus mode, data/address line HAD7 in multiplexed bus mode, or GPIO line PB7 when the GPIO function is enabled for this pin. Unlike the TQFP package, most of the GND pins are connected internally in the center of the connection array and act as heat sink for the chip. Therefore, except for GND_P and GND_{P1} that support the PLL, other GND signals do not support individual subsystems in the chip.
2. NC stands for Not Connected. The following pin groups are shorted to each other:
   — pins A2, B1, and B2
   — pins A15, B15, B16, C14, C15, C16, and D14
   — pins N3, R1, R2, and T2
   — pins N16, P13, P15, R15, R16, and T15
   Do not connect any line, component, trace, or via to these pins.

```
M_SCRE EQU 8      ; SCI Receiver Enable
M_SCTE EQU 9      ; SCI Transmitter Enable
M_ILIE EQU 10     ; Idle Line Interrupt Enable
M_SCRIE EQU 11     ; SCI Receive Interrupt Enable
M_SCTIE EQU 12     ; SCI Transmit Interrupt Enable
M_TMIE EQU 13     ; Timer Interrupt Enable
M_TIR EQU 14     ; Timer Interrupt Rate
M_SCKP EQU 15     ; SCI Clock Polarity
M_REIE EQU 16     ; SCI Error Interrupt Enable (REIE)

;       SCI Status Register Bit Flags

M_TRNE EQU 0      ; Transmitter Empty
M_TDRE EQU 1      ; Transmit Data Register Empty
M_RDRF EQU 2      ; Receive Data Register Full
M_IDLE EQU 3      ; Idle Line Flag
M_OR EQU 4      ; Overrun Error Flag
M_PE EQU 5      ; Parity Error
M_FE EQU 6      ; Framing Error Flag
M_R8 EQU 7      ; Received Bit 8 (R8) Address

;       SCI Clock Control Register

M_CD EQU $FFF   ; Clock Divider Mask (CD0-CD11)
M_COD EQU 12     ; Clock Out Divider
M_SCP EQU 13     ; Clock Prescaler
M_RCM EQU 14     ; Receive Clock Mode Source Bit
M_TCM EQU 15     ; Transmit Clock Source Bit

;------------------------------------------------------------------------
;
;      EQUATES for Synchronous Serial Interface (SSI)
;
;------------------------------------------------------------------------

;
;       Register Addresses Of SSI0
M_TX00 EQU $FFFFBC; SSI0 Transmit Data Register 0
M_TX01 EQU $FFFFBB; SSIO Transmit Data Register 1
M_TX02 EQU $FFFFBA; SSIO Transmit Data Register 2
M_TSR0 EQU $FFFFB9; SSI0 Time Slot Register
M_RX0 EQU $FFFFB8; SSI0 Receive Data Register
M_SSISR0 EQU $FFFFB7; SSI0 Status Register
M_CRB0 EQU $FFFFB6; SSI0 Control Register B
M_CRA0 EQU $FFFFB5; SSI0 Control Register A
M_TSMA0 EQU $FFFFB4; SSI0 Transmit Slot Mask Register A
M_TSMB0 EQU $FFFFB3; SSI0 Transmit Slot Mask Register B
M_RSMA0 EQU $FFFFB2; SSI0 Receive Slot Mask Register A
M_RSMB0 EQU $FFFFB1; SSI0 Receive Slot Mask Register B

;       Register Addresses Of SSI1
M_TX10 EQU $FFFFAC; SSI1 Transmit Data Register 0
M_TX11 EQU $FFFFAB; SSI1 Transmit Data Register 1
M_TX12 EQU $FFFFAA; SSI1 Transmit Data Register 2
M_TSR1 EQU $FFFFA9; SSI1 Time Slot Register
M_RX1 EQU $FFFFA8; SSI1 Receive Data Register
M_SSISR1 EQU $FFFFA7; SSI1 Status Register
M_CRB1 EQU $FFFFA6; SSI1 Control Register B
M_CRA1 EQU $FFFFA5; SSI1 Control Register A
M_TSMA1 EQU $FFFFA4; SSI1 Transmit Slot Mask Register A
```