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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 13x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f058c8u6

3.14.2 General-purpose timers (TIM2, 3, 14, 15, 16, 17)

There are six synchronizable general-purpose timers embedded in the STM32F058C8/R8/T8 devices (see *Table 6* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3

STM32F058C8/R8/T8 devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate withTIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

3.14.3 Basic timer TIM6

This timer is mainly used for DAC trigger generation. It can also be used as a generic 16-bit time base.

3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop mode. It can be used

either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- maskable system interrupt generation when the counter reaches 0
- programmable clock source (HCLK or HCLK/8)

3.15 Real-time clock (RTC) and backup registers

The RTC and the five backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset.

The RTC is an independent BCD timer/counter. Its main features are the following:

- calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- programmable alarm with wake up from Stop mode capability
- on-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop mode on tamper event detection
- timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop mode on timestamp event detection
- reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

The RTC clock sources can be:

- a 32.768 kHz external crystal
- a resonator or oscillator
- the internal low-power RC oscillator (typical frequency of 40 kHz)
- the high-speed external clock divided by 32

3.16 Inter-integrated circuit interface (I^2C)

Up to two I^2C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s) and Fast mode (up to 400 kbit/s) and, I2C1 also supports Fast Mode Plus (up to 1 Mbit/s) with extra output drive.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). They also include programmable analog and digital noise filters.

Table 7. Comparison of I^2C analog and digital filters

Aspect	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2Cx peripheral clocks
Benefits	Available in Stop mode	–Extra filtering capability vs. standard requirements –Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C peripherals can be served by the DMA controller.

Refer to *Table 8* for the differences between I2C1 and I2C2.

Table 8. STM32F058C8/R8/T8 I^2C implementation

I^2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus (up to 1 Mbit/s) with extra output drive I/Os	X	-
Independent clock	X	-

Table 12. Pin definitions (continued)

Pin number				Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	UFBGA64	UFQFPN48	WLCSP36					Alternate functions	Additional functions
56	A4	40	A3	PB4	I/O	FT	-	SPI1_MISO, I2S1_MCK, TIM3_CH1, TSC_G5_IO2, EVENTOUT	-
57	C4	41	E6	PB5	I/O	FT	-	SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	-
58	D3	42	C4	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_IO3	-
59	C3	43	A4	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, TIM17_CH1N, TSC_G5_IO4	-
60	B4	44	B4	BOOT0	I	B	-	Boot memory selection	
61	B3	45	-	PB8	I/O	FTf	(5)	I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC	-
62	A3	46	-	PB9	I/O	FTf	(5)	I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT	-
63	D5	47	D6	VSS	S	-	-	Ground	
64	E5	48	A5	VDD	S	-	-	Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After the first RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the main reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the reference manual.
3. Distinct VSSA pin is not available on WLCSP36 package. The pin number corresponds to the VSS pin to which VSSA pad of the silicon die is connected.
4. This pin is powered by V_{DDA}.
5. On the WLCSP36 package, PB8, PB9, PB10, PB11, PB12, PB13, PB14 and PB15 must be set to defined levels by software, as their corresponding pads on the silicon die are left unconnected. Apply the same recommendations as for unconnected pins.
6. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.

Table 14. Alternate functions selected through GPIOB_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	TSC_G3_IO2
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TSC_G3_IO3
PB3	SPI1_SCK, I2S1_CK	EVENTOUT	TIM2_CH2	TSC_G5_IO1
PB4	SPI1_MISO, I2S1_MCK	TIM3_CH1	EVENTOUT	TSC_G5_IO2
PB5	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	TSC_G5_IO3
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	TSC_G5_IO4
PB8	CEC	I2C1_SCL	TIM16_CH1	TSC_SYNC
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT
PB10	CEC	I2C2_SCL	TIM2_CH3	TSC_SYNC
PB11	EVENTOUT	I2C2_SDA	TIM2_CH4	TSC_G6_IO1
PB12	SPI2_NSS	EVENTOUT	TIM1_BKIN	TSC_G6_IO2
PB13	SPI2_SCK		TIM1_CH1N	TSC_G6_IO3
PB14	SPI2_MISO	TIM15_CH1	TIM1_CH2N	TSC_G6_IO4
PB15	SPI2_MOSI	TIM15_CH2	TIM1_CH3N	TIM15_CH1N

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 1.8 V and V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 8. Pin loading conditions

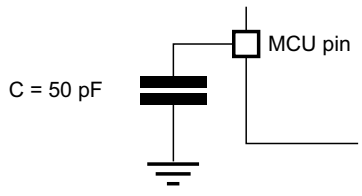


Figure 9. Pin input voltage

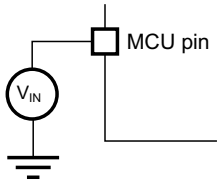


Table 17. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD power lines (source)(1)	120	mA
ΣI_{VSS}	Total current out of sum of all VSS ground lines (sink)(1)	-120	
$I_{VDD(PIN)}$	Maximum current into each VDD power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each VSS ground pin (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	80	
	Total output current sourced by sum of all I/Os and control pins(2)	-80	
$I_{INJ(PIN)}$(3)	Injected current on POR, B, FT and FTf pins	-5/+0(4)	
	Injected current on TC and RST pin	± 5	
	Injected current on TTa pins(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 16: Voltage characteristics* for the maximum allowed input voltage values.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device. See note (2) below *Table 52: ADC accuracy*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 18. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 22. Typical and maximum current consumption from V_{DD} at 1.8 V (continued)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Sleep mode	HSE bypass, PLL on	48 MHz	12.5	13.7	14.4	14.9	2.7	2.9	3.0	3.2	mA
			32 MHz	8.8	9.3	9.7	10.1	1.8	2.0	2.2	2.3	
			24 MHz	6.8	7.3	7.7	8.1	1.5	1.5	1.6	1.7	
		HSE bypass, PLL off	8 MHz	2.2	2.6	2.8	3.0	0.5	0.6	0.6	0.6	
			1 MHz	0.3	0.4	0.4	0.5	0.1	0.2	0.2	0.2	
		HSI clock, PLL on	48 MHz	12.6	13.8	14.5	15.1	2.8	2.9	3.1	3.3	
			32 MHz	8.8	9.5	9.8	10.2	1.9	2.1	2.2	2.4	
			24 MHz	6.9	7.4	7.8	8.1	1.5	1.6	1.7	1.8	
		HSI clock, PLL off	8 MHz	2.3	2.7	2.9	3.1	0.5	0.6	0.7	0.8	

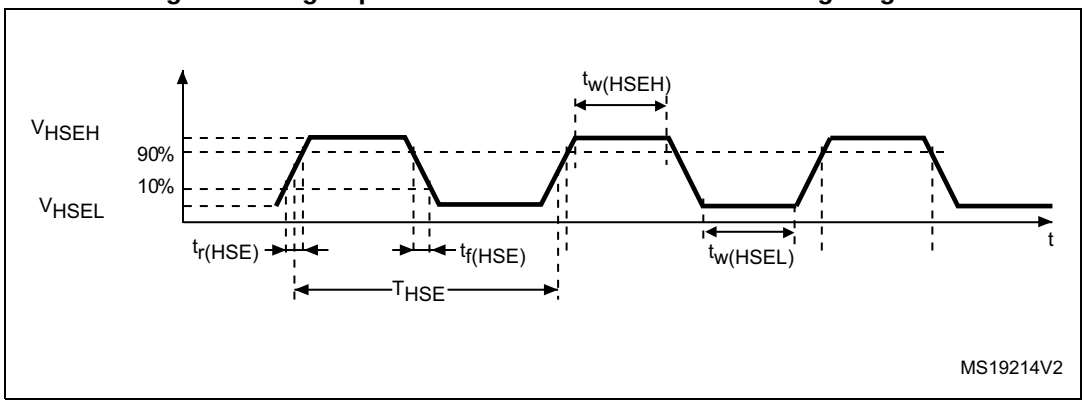
1. Data based on characterization results, not tested in production unless otherwise specified.

Table 23. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	VDDA = 2.4 V				VDDA = 3.6 V				Unit
				Typ	Max @ TA(2)			Typ	Max @ TA(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run or Sleep mode, code executing from Flash memory or RAM	External clock (HSE bypass)	48 MHz	148	169	179	183	162	183	195	198	µA
			32 MHz	103	121	126	128	111	129	135	138	
			24 MHz	81	96	100	103	87	102	106	108	
			8 MHz	1.0	3.0	3.0	3.0	2.0	3.0	3.0	4.0	
			1 MHz	1.0	2.0	2.0	2.0	2.0	2.0	3.0	3.0	
		Internal clock (HSI)	48 MHz	218	240	251	255	242	263	275	278	
			32 MHz	172	191	199	202	191	209	215	218	
			24 MHz	150	168	173	175	166	183	190	192	
			8 MHz	70	80	82	83	82	91	94	95	

1. Current consumption from the VDDA supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, IDDA is independent from the frequency.
2. Data based on characterization results, not tested in production unless otherwise specified.

Figure 12. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

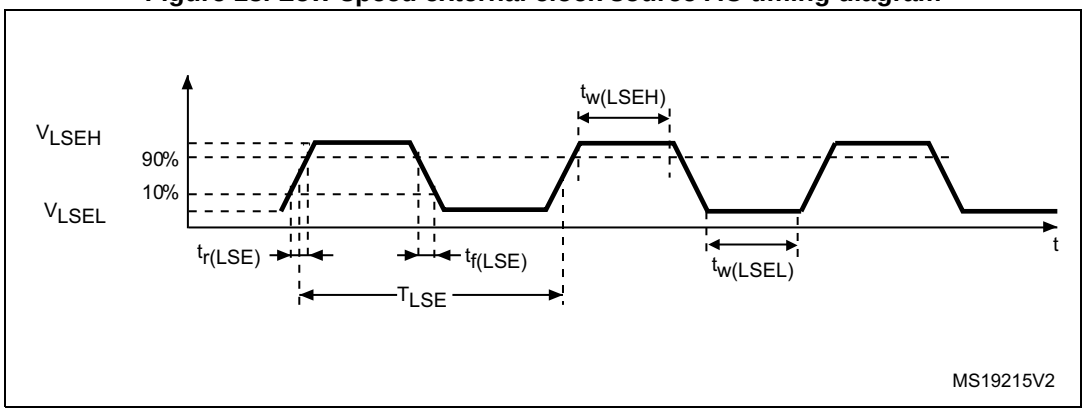
The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 13*.

Table 31. Low-speed external user clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	50	

1. Guaranteed by design, not tested in production.

Figure 13. Low-speed external clock source AC timing diagram



Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 41. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/48 MHz	
S_{EMI}	Peak level	V_{DD} = 1.8 V, T_A = 25 °C, LQFP64 package compliant with IEC 61967-2	0.1 to 30 MHz	0	dBµV
			30 to 130 MHz	22	
			130 MHz to 1 GHz	16	
			EMI Level	3.5	-

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Figure 18. TC and TTa I/O input characteristics

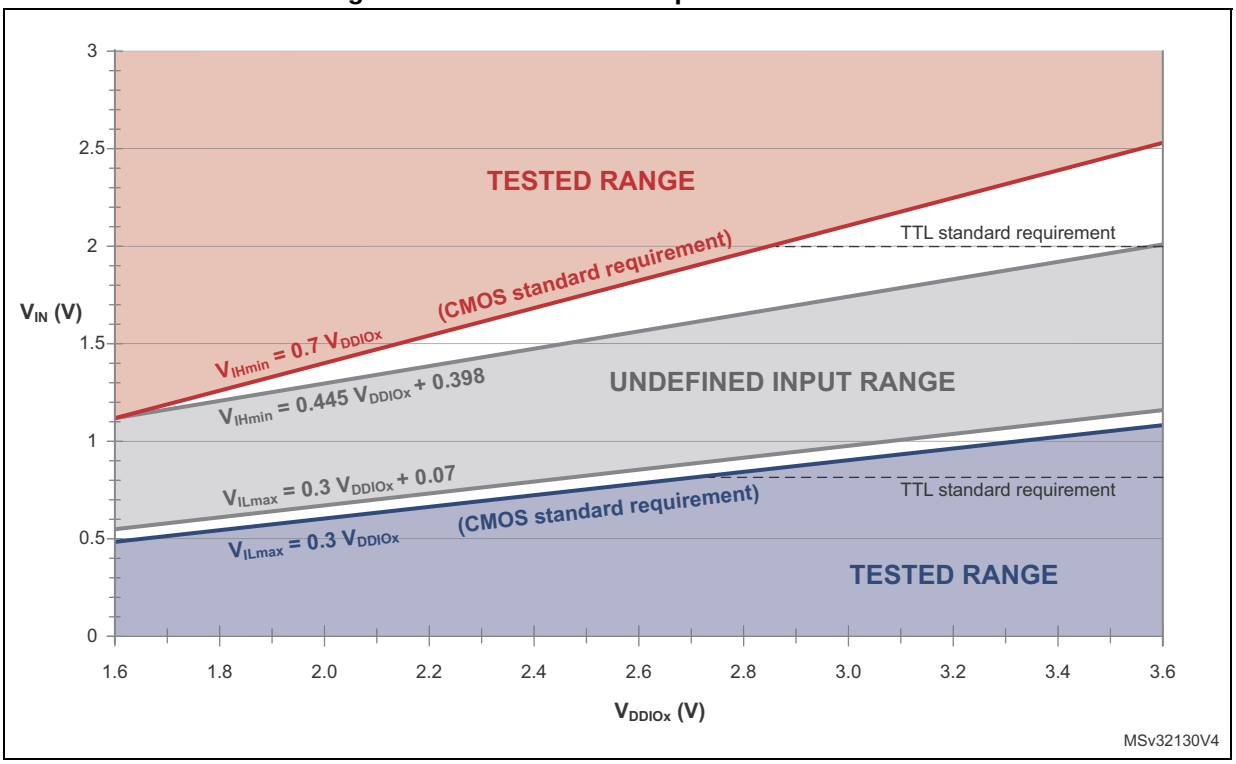
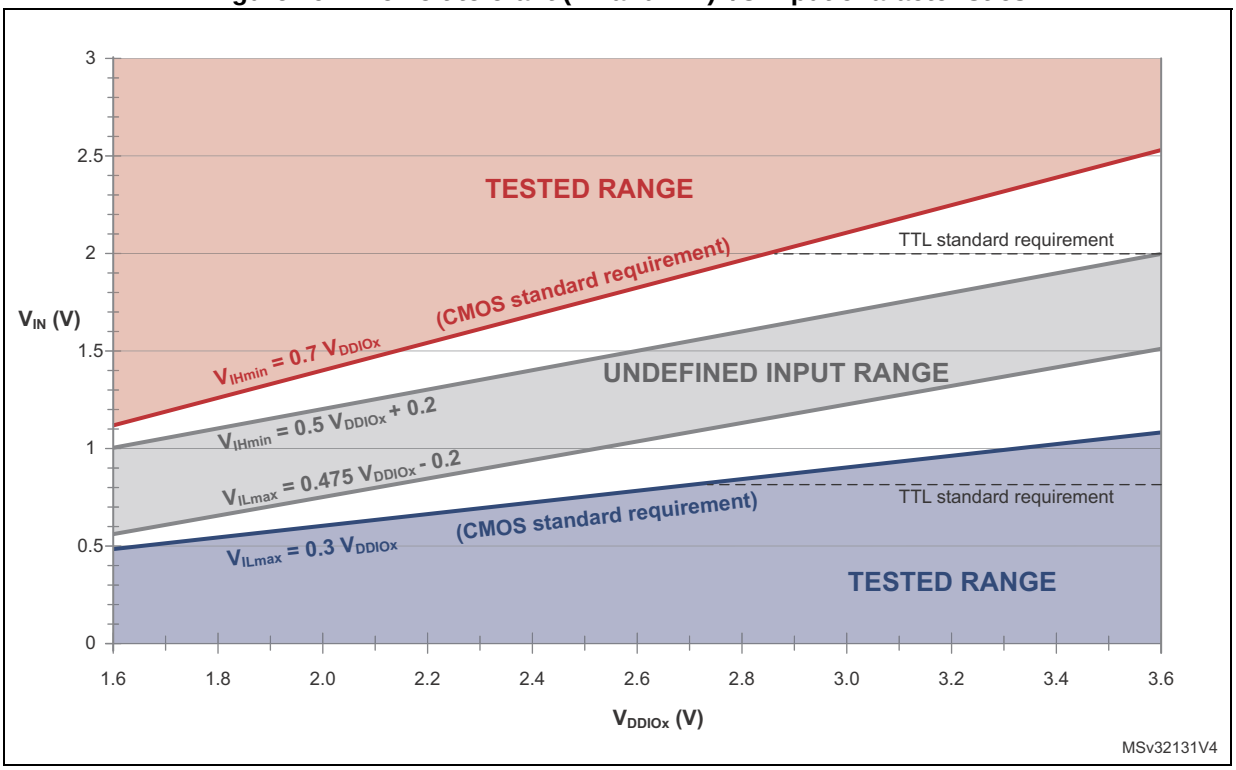


Figure 19. Five volt tolerant (FT and FTf) I/O input characteristics



6.3.14 NRST and NPOR pin characteristics

NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

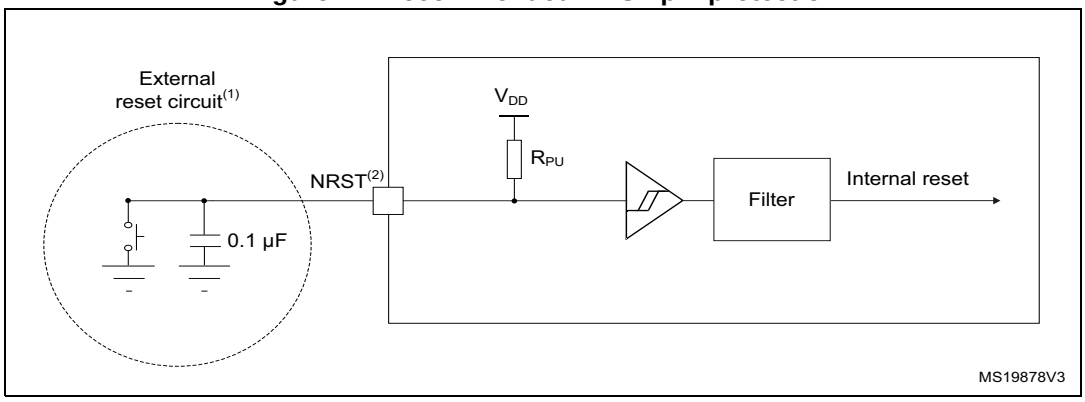
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 19: General operating conditions*.

Table 48. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3\ V_{DD}+0.07^{(1)}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.445\ V_{DD}+0.398^{(1)}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	100(1)	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	-	700(1)	-	-	ns

1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 21. Recommended NRST pin protection



1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 48: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.

NPOR pin characteristics

The NPOR pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor to the V_{DDA}, R_{PU}.

Unless otherwise specified, the parameters given in *Table 49* below are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19: General operating conditions*.

Table 60. I^2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI/I^2S characteristics

Unless otherwise specified, the parameters given in *Table 61* for SPI or in *Table 62* for I^2S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 19: General operating conditions*.

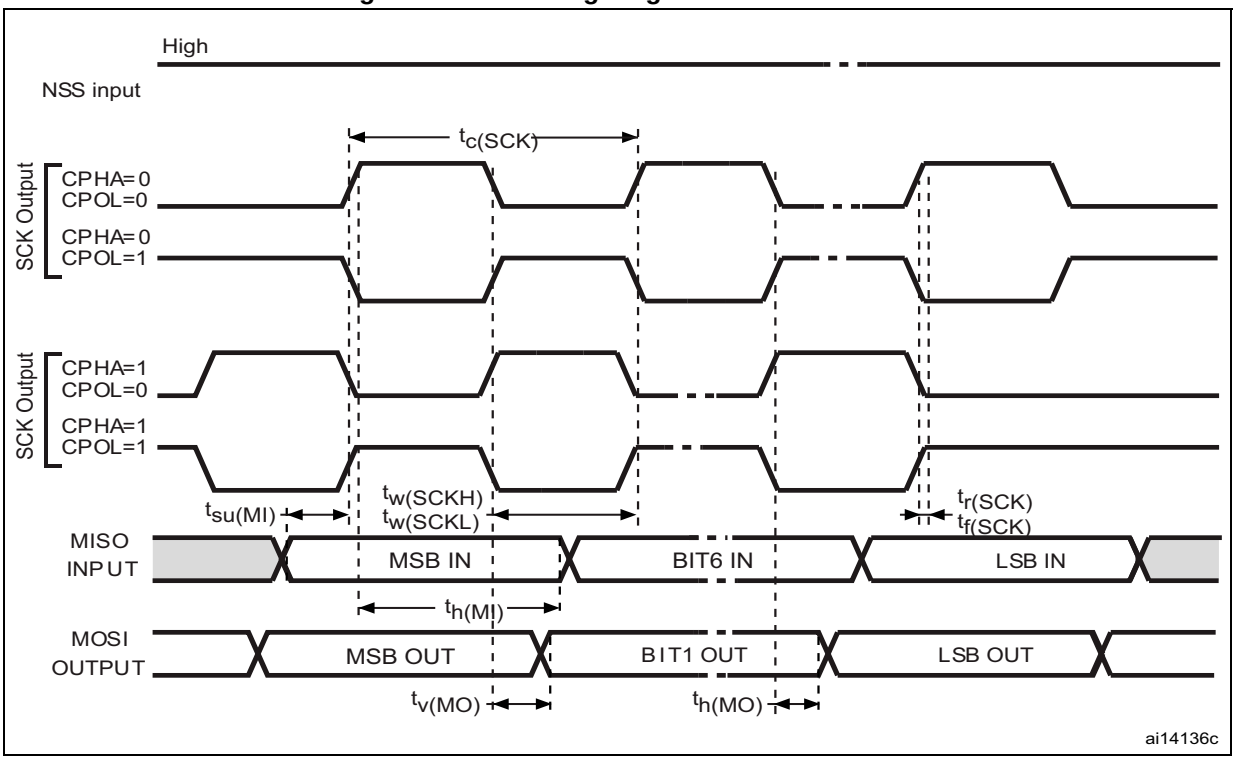
Refer to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^2S).

Table 61. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2Tpclk + 10	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	
		Slave mode	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	4	-	
$t_{h(SI)}$		Slave mode	5	-	
$t_{a(SO)}$(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	3Tpclk	
$t_{dis(SO)}$(3)	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	22.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	6	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	11.5	-	
$t_{h(MO)}$		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 28. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 62. I^2S characteristics(1)

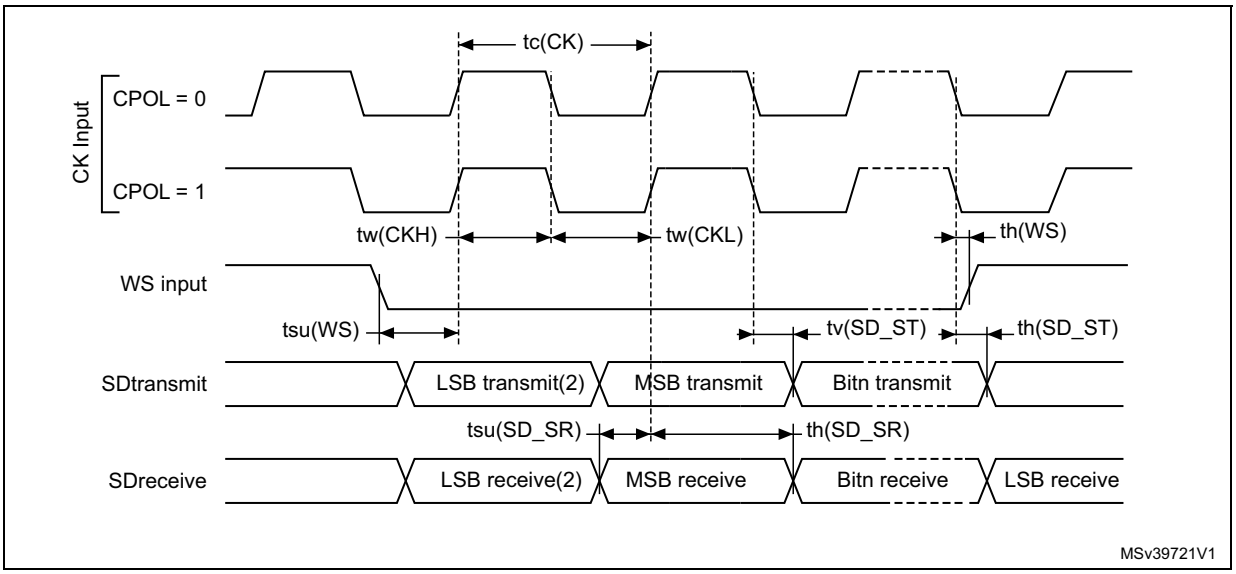
Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.597	1.601	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$	I^2S clock rise time	Capacitive load C_L = 15 pF	-	10	ns
$t_{f(CK)}$	I^2S clock fall time		-	12	
$t_{w(CKH)}$	I^2S clock high time	Master f_{PCLK}= 16 MHz, audio frequency = 48 kHz	306	-	
$t_{w(CKL)}$	I^2S clock low time		312	-	
$t_{v(WS)}$	WS valid time	Master mode	2	-	
$t_{h(WS)}$	WS hold time	Master mode	2	-	
$t_{su(WS)}$	WS setup time	Slave mode	7	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
DuCy(SCK)	I^2S slave input clock duty cycle	Slave mode	25	75	%

Table 62. I²S characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	6	-	ns
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$(2)	Data input hold time	Master receiver	4	-	
$t_{h(SD\_SR)}$(2)		Slave receiver	0.5	-	
$t_{v(SD\_MT)}$(2)	Data output valid time	Master transmitter	-	4	
$t_{v(SD\_ST)}$(2)		Slave transmitter	-	31	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter	0	-	
$t_{h(SD\_ST)}$		Slave transmitter	13	-	

1. Data based on design simulation and/or characterization results, not tested in production.
2. Depends on f_{PCLK}. For example, if f_{PCLK} = 8 MHz, then T_{PCLK} = 1/f_{PLCLK} = 125 ns.

Figure 29. I²S slave timing diagram (Philips protocol)



1. Measurement points are done at CMOS levels: 0.3 × V_{DDIOx} and 0.7 × V_{DDIOx}.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 63. UFBGA64 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
b	0.170	0.280	0.330	0.0067	0.0110	0.0130
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	3.450	3.500	3.550	0.1358	0.1378	0.1398
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	3.450	3.500	3.550	0.1358	0.1378	0.1398
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 32. Recommended footprint for UFBGA64 package

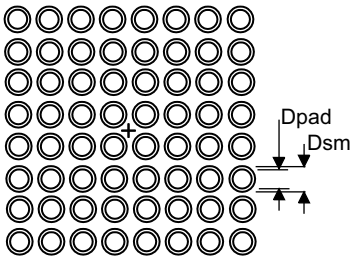


Table 64. UFBGA64 recommended PCB design rules

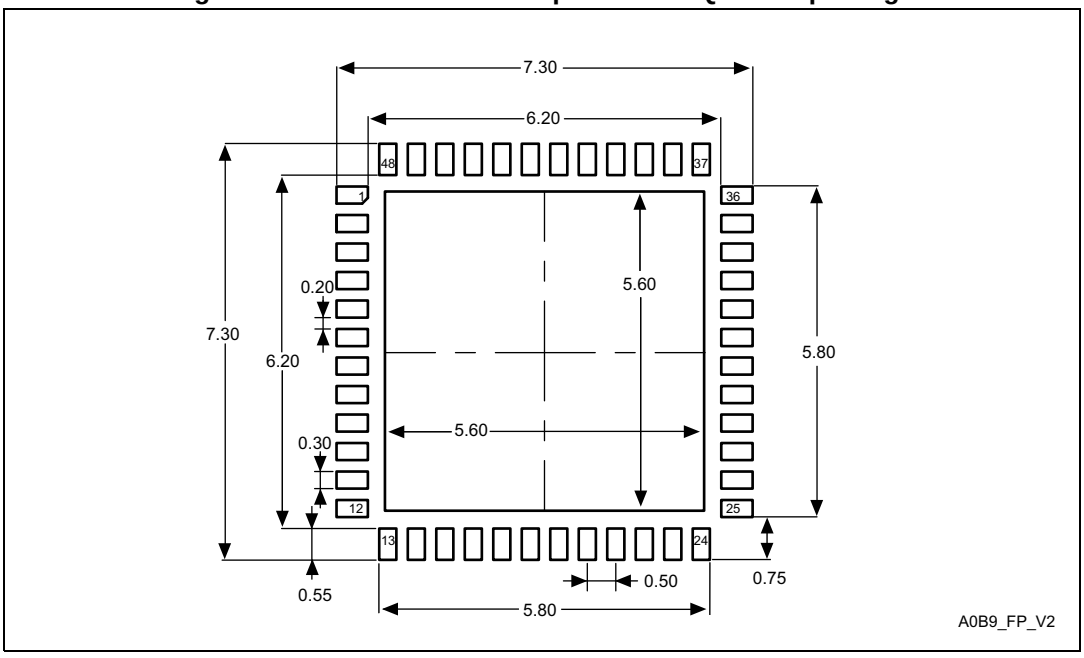
Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

Table 66. UFQFPN48 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 38. Recommended footprint for UFQFPN48 package



1. Dimensions are expressed in millimeters.

Table 67. WLCSP36 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
F	-	0.3025	-	-	0.0119	-
G	-	0.3515	-	-	0.0138	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 41. Recommended pad footprint for WLCSP36 package

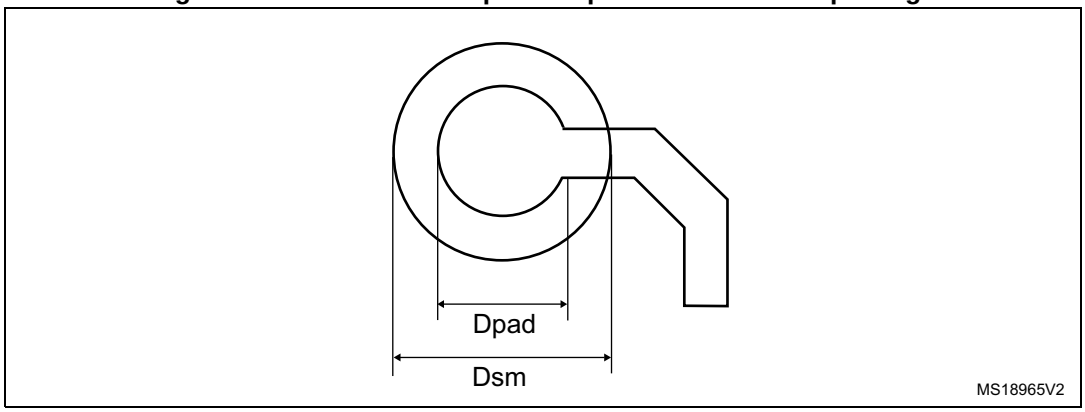


Table 68. WLCSP36 recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	260 µm max. (circular) 220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed