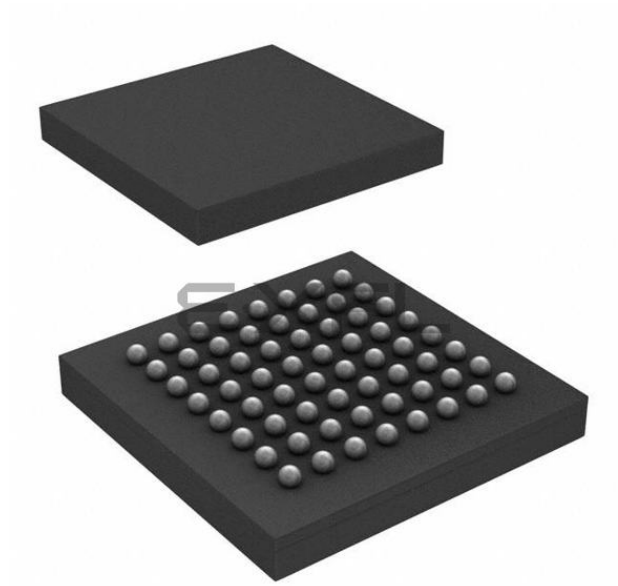


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 19x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA
Supplier Device Package	64-UFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f058r8h6

List of tables

2 Description

The STM32F058C8/R8/T8 microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (64 Kbytes of Flash memory and 8 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (up to two I^2Cs, up to two SPIs, one I^2S, one HDMI CEC and up to two USARTs), one 12-bit ADC, one 12-bit DAC, six 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F058C8/R8/T8 microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges at a 1.8 V ± 8% power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F058C8/R8/T8 microcontrollers include devices in four different packages ranging from 36 pins to 64 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

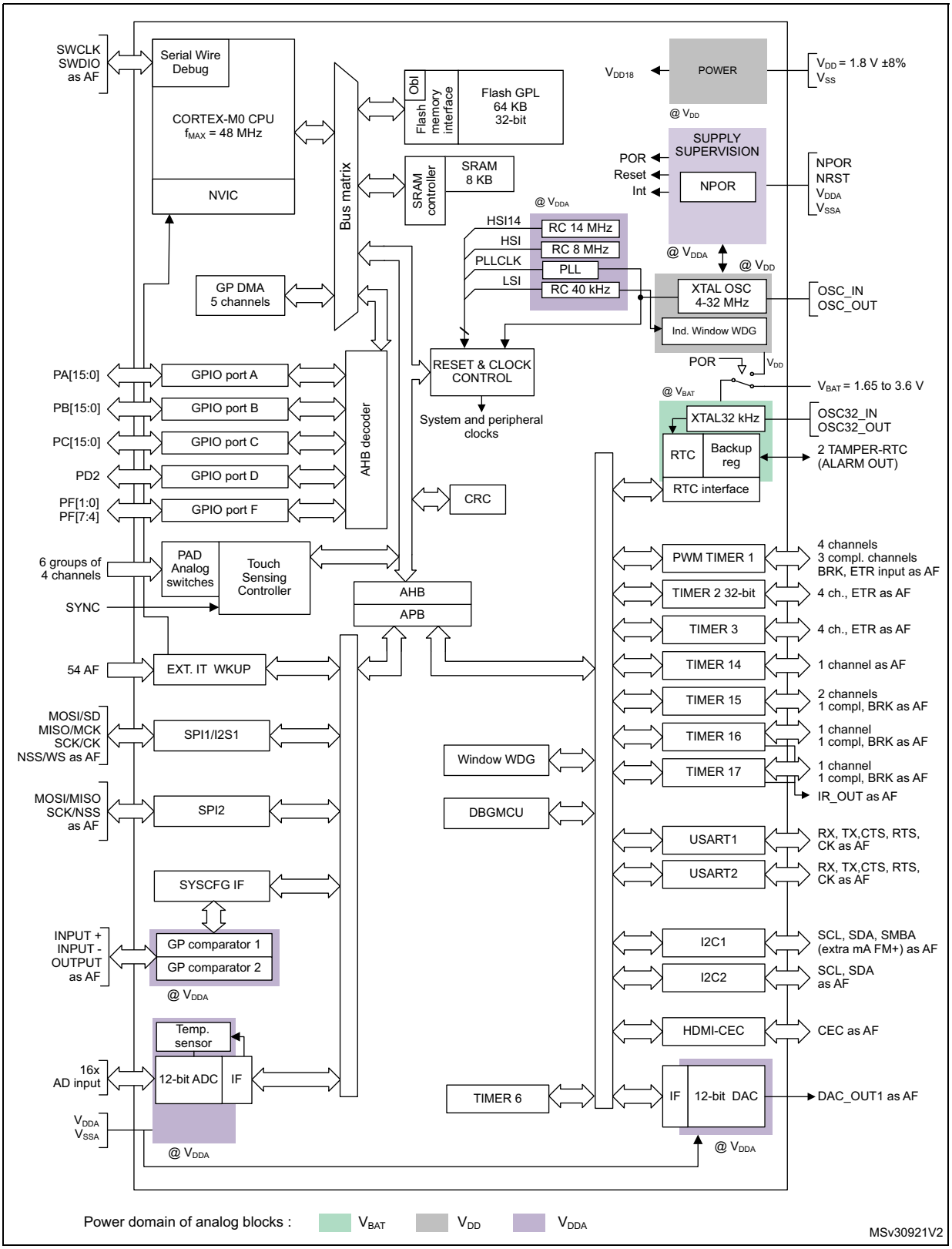
These features make the STM32F058C8/R8/T8 microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.

Table 1. STM32F058C8/R8/T8 family device features and peripheral counts

Peripheral		STM32F058T8	STM32F058C8	STM32F058R8
Flash memory (Kbyte)		64		
SRAM (Kbyte)		8		
Timers	Advanced control	1 (16-bit)		
	General purpose	5 (16-bit) 1 (32-bit)		
	Basic	1 (16-bit)		
Comm. interfaces	SPI [I^2S](1)	1 [1]	2 [1]	
	I^2C	2		
	USART	2		
	CEC	1		
12-bit ADC (number of channels)		1 (10 ext. + 3 int.)		1 (16 ext. + 3 int.)
12-bit DAC (number of channels)		1 (1)		
Analog comparator		2		
GPIOs		28	38	54
Capacitive sensing channels		13	16	17
Max. CPU frequency		48 MHz		
Operating voltage		V_{DD} = 1.8 V ± 8%, V_{DDA} = from V_{DD} to 3.6 V		
Operating temperature		Ambient operating temperature: -40°C to 85°C / -40°C to 105°C Junction temperature: -40°C to 105°C / -40°C to 125°C		
Packages		WLCSP36	UFQFPN48	LQFP64 UFBGA64

1. The SPI1 interface can be used either in SPI mode or in I^2S audio mode.

Figure 1. Block diagram



The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPIx, I2Sx, I2Cx, USARTx, all TIMx timers (except TIM14), DAC and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 54 GPIOs can be connected to the 16 external interrupt lines.

3.10 Analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter has up to 16 external and 3 internal (temperature

hardware touch sensing controller and only requires few external components to operate. For operation, one capacitive sensing GPIO in each group is connected to an external capacitor and cannot be used as effective touch sensing channel.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 4. Capacitive sensing GPIOs available on STM32F058C8/R8/T8 devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	4	TSC_G4_IO1	PA9
	TSC_G1_IO2	PA1		TSC_G4_IO2	PA10
	TSC_G1_IO3	PA2		TSC_G4_IO3	PA11
	TSC_G1_IO4	PA3		TSC_G4_IO4	PA12
2	TSC_G2_IO1	PA4	5	TSC_G5_IO1	PB3
	TSC_G2_IO2	PA5		TSC_G5_IO2	PB4
	TSC_G2_IO3	PA6		TSC_G5_IO3	PB6
	TSC_G2_IO4	PA7		TSC_G5_IO4	PB7
3	TSC_G3_IO1	PC5	6	TSC_G6_IO1	PB11
	TSC_G3_IO2	PB0		TSC_G6_IO2	PB12
	TSC_G3_IO3	PB1		TSC_G6_IO3	PB13
				TSC_G6_IO4	PB14

Table 5. No. of capacitive sensing channels available on STM32F058C8/R8/T8 devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F058R8	STM32F058C8	STM32F058T8
G1	3	3	3
G2	3	3	3
G3	2	1	1
G4	3	3	3
G5	3	3	3
G6	3	3	0
Number of capacitive sensing channels	17	16	13

The RTC clock sources can be:

- a 32.768 kHz external crystal
- a resonator or oscillator
- the internal low-power RC oscillator (typical frequency of 40 kHz)
- the high-speed external clock divided by 32

3.16 Inter-integrated circuit interface (I^2C)

Up to two I^2C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s) and Fast mode (up to 400 kbit/s) and, I2C1 also supports Fast Mode Plus (up to 1 Mbit/s) with extra output drive.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). They also include programmable analog and digital noise filters.

Table 7. Comparison of I^2C analog and digital filters

Aspect	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2Cx peripheral clocks
Benefits	Available in Stop mode	–Extra filtering capability vs. standard requirements –Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C peripherals can be served by the DMA controller.

Refer to *Table 8* for the differences between I2C1 and I2C2.

Table 8. STM32F058C8/R8/T8 I^2C implementation

I^2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus (up to 1 Mbit/s) with extra output drive I/Os	X	-
Independent clock	X	-

Table 8. STM32F058C8/R8/T8 I²C implementation (continued)

I²C features(1)	I2C1	I2C2
SMBus	X	-
Wakeup from STOP	X	-

1. X = supported.

3.17 Universal synchronous/asynchronous receiver/transmitter (USART)

The device embeds up to two universal synchronous/asynchronous receivers/transmitters (USART1, USART2) which communicate at speeds of up to 6 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 supports also SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and has a clock domain independent of the CPU clock, allowing to wake up the MCU from Stop mode.

The USART interfaces can be served by the DMA controller.

Table 9. STM32F058C8/R8/T8 USART implementation

USART modes/features(1)	USART1	USART2
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	X
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-
LIN mode	X	-
Dual clock domain and wakeup from Stop mode	X	-
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto baud rate detection	X	-
Driver Enable	X	X

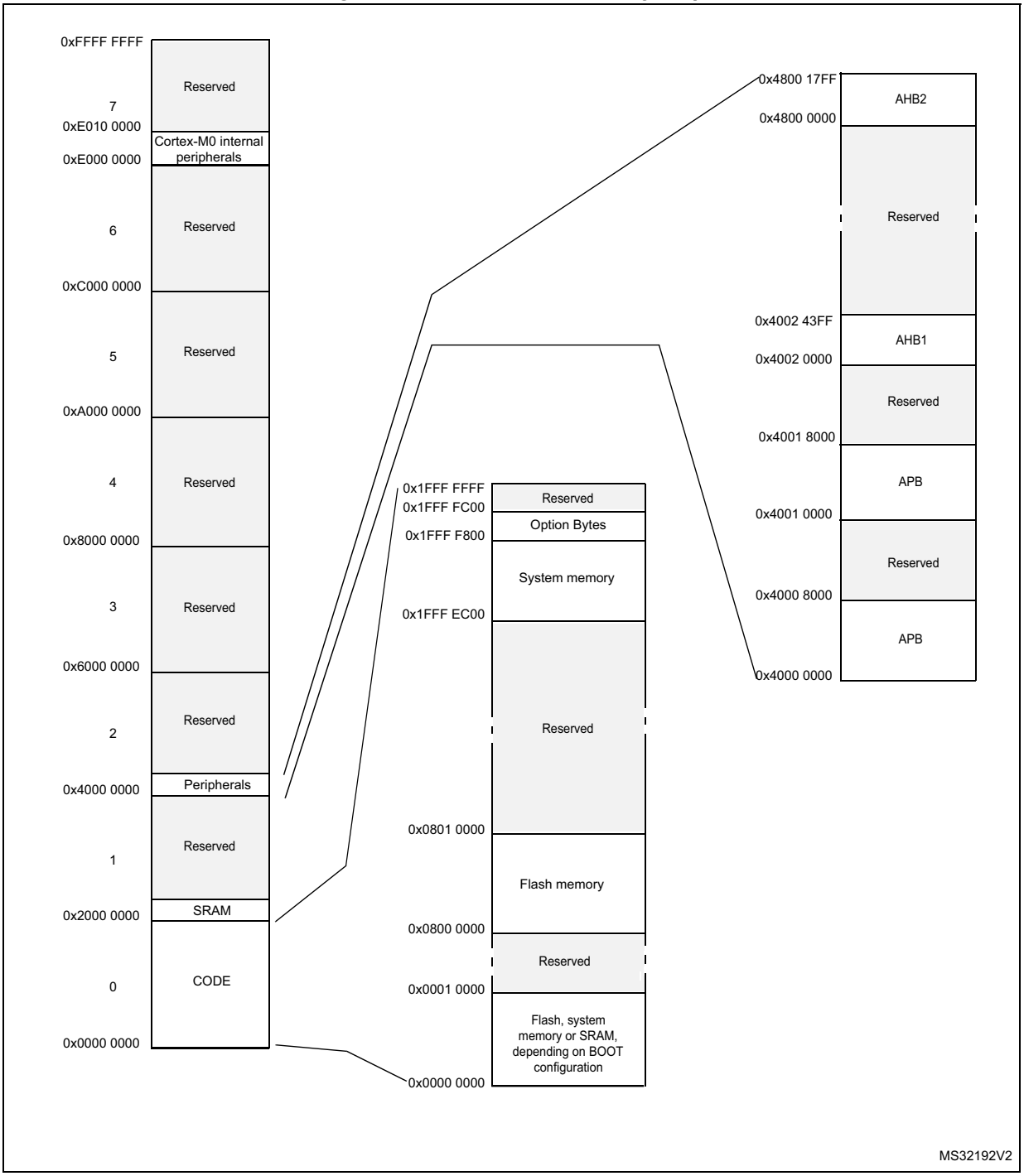
1. X = supported.

Table 13. Alternate functions selected through GPIOA_AFR registers for port A

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	USART2_CTS	TIM2_CH1_ETR	TSC_G1_IO1		-	-	COMP1_OUT
PA1	EVENTOUT	USART2_RTS	TIM2_CH2	TSC_G1_IO2			-	-
PA2	TIM15_CH1	USART2_TX	TIM2_CH3	TSC_G1_IO3	-	-	-	COMP2_OUT
PA3	TIM15_CH2	USART2_RX	TIM2_CH4	TSC_G1_IO4	-	-	-	-
PA4	SPI1_NSS, I2S1_WS	USART2_CK	-	TSC_G2_IO1	TIM14_CH1	-	-	-
PA5	SPI1_SCK, I2S1_CK	CEC	TIM2_CH1_ETR	TSC_G2_IO2	-	-	-	-
PA6	SPI1_MISO, I2S1_MCK	TIM3_CH1	TIM1_BKIN	TSC_G2_IO3		TIM16_CH1	EVENTOUT	COMP1_OUT
PA7	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM1_CH1N	TSC_G2_IO4	TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT		-	-	-
PA9	TIM15_BKIN	USART1_TX	TIM1_CH2	TSC_G4_IO1	-	-	-	-
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	TSC_G4_IO2	-	-	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	TSC_G4_IO3	-	-	-	COMP1_OUT
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	TSC_G4_IO4	-	-	-	COMP2_OUT
PA13	SWDIO	IR_OUT		-	-	-	-	-
PA14	SWCLK	USART2_TX	-	-	-	-	-	-
PA15	SPI1_NSS, I2S1_WS	USART2_RX	TIM2_CH1_ETR	EVENTOUT		-	-	-

5 Memory mapping

Figure 7. STM32F058x8 memory map



trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 28: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 28*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in *Table 16: Voltage characteristics*

Table 28. Peripheral current consumption

Peripheral		Typical consumption at 25 °C	Unit
AHB	BusMatrix(1)	5	µA/MHz
	DMA1	7	
	SRAM	1	
	Flash memory interface	14	
	CRC	2	
	GPIOA	9	
	GPIOB	12	
	GPIOC	2	
	GPIOD	1	
	GPIOF	1	
	TSC	6	
	All AHB peripherals	**55**	

Low-speed internal (LSI) RC oscillator

Table 36. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DDA(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.8 PLL characteristics

The parameters given in *Table 37* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19: General operating conditions*.

Table 37. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	8.0	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	48	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
$Jitter_{PLL}$	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

6.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 38. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = - 40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (1 KB) erase time	T_A = - 40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = - 40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

Input/output AC characteristics

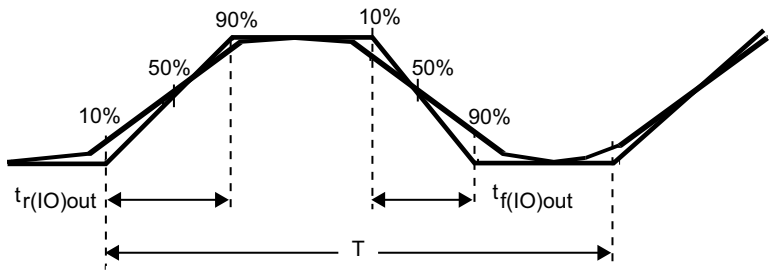
The definition and values of input/output AC characteristics are given in *Figure 20* and *Table 47*, respectively. Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 19: General operating conditions*.

Table 47. I/O AC characteristics(1)(2)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF	-	1	MHz
	$t_{f(IO)out}$	Output fall time		-	125	ns
	$t_{r(IO)out}$	Output rise time		-	125	
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF	-	4	MHz
	$t_{f(IO)out}$	Output fall time		-	62.5	ns
	$t_{r(IO)out}$	Output rise time		-	62.5	
11	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF	-	10	MHz
	$t_{f(IO)out}$	Output fall time		-	25	ns
	$t_{r(IO)out}$	Output rise time		-	25	
Fm+ configuration (4)	$f_{max(IO)out}$	Maximum frequency(3)	CL = 50 pF	-	0.5	MHz
	$t_{f(IO)out}$	Output fall time		-	16	ns
	$t_{r(IO)out}$	Output rise time		-	44	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxxx RM0091 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in *Figure 20*.
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxxx reference manual RM0091 for a detailed description of Fm+ I/O configuration.

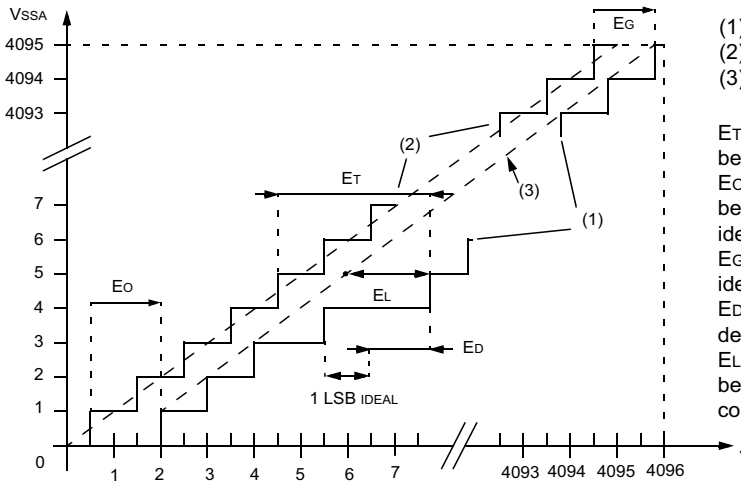
Figure 20. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \le \frac{2}{3}T$ and if the duty cycle is (45-55%)
when loaded by C_L (see the table *I/O AC characteristics definition*)

MS32132V3

Figure 22. ADC accuracy characteristics

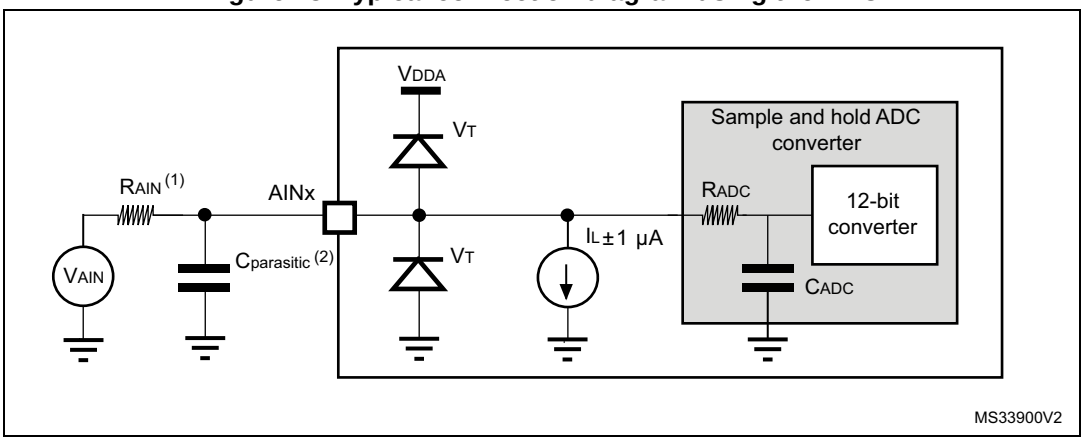


(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

E_T = Total Unajusted Error: maximum deviation between the actual and ideal transfer curves.
E_O = Offset Error: maximum deviation between the first actual transition and the first ideal one.
E_G = Gain Error: deviation between the last ideal transition and the last actual one.
E_D = Differential Linearity Error: maximum deviation between actual steps and the ideal ones.
E_L = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

MS19880V2

Figure 23. Typical connection diagram using the ADC



MS33900V2

1. Refer to *Table 50: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 10: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.16 DAC electrical specifications

Table 53. DAC characteristics

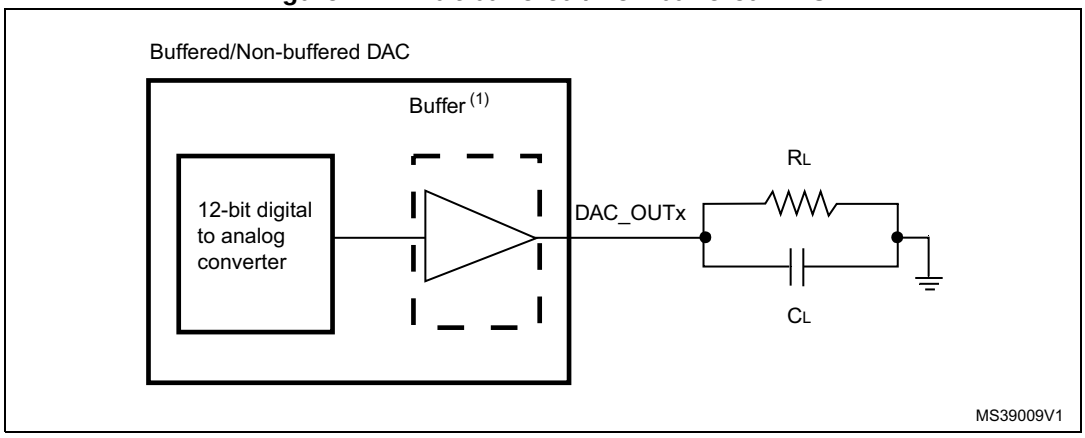
Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage for DAC ON	2.4	-	3.6	V	-
R_{LOAD}(1)	Resistive load with buffer ON	5	-	-	kΩ	Load connected to V_{SSA}
		25	-	-	kΩ	Load connected to V_{DDA}
R_O(1)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(1)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{DDA} = 3.6 V and (0x155) and (0xEAB) at V_{DDA} = 2.4 V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{DDA} – 1LSB	V	
I_{DDA}(1)	DAC DC current consumption in quiescent mode(2)	-	-	600	µA	With no load, middle code (0x800) on the input
		-	-	700	µA	With no load, worst code (0xF1C) on the input
DNL(3)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration
		-	-	±2	LSB	Given for the DAC in 12-bit configuration
INL(3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration
		-	-	±4	LSB	Given for the DAC in 12-bit configuration
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{DDA}/2)	-	-	±10	mV	-
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{DDA} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{DDA} = 3.6 V

Table 53. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Gain error(3)	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$(3)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}(3)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Guaranteed by design, not tested in production.
2. The DAC is in “quiescent mode” when it keeps the value steady on the output so no dynamic consumption is involved.
3. Data based on characterization results, not tested in production.

Figure 24. 12-bit buffered / non-buffered DAC



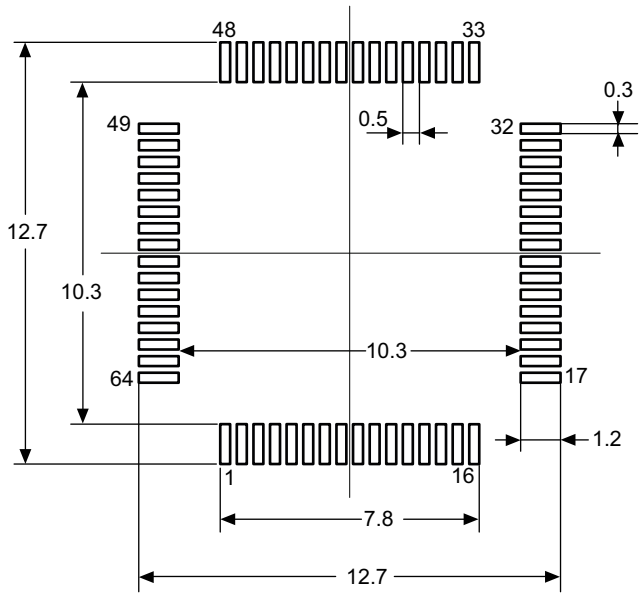
1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 65. LQFP64 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 35. Recommended footprint for LQFP64 package



1. Dimensions are expressed in millimeters.