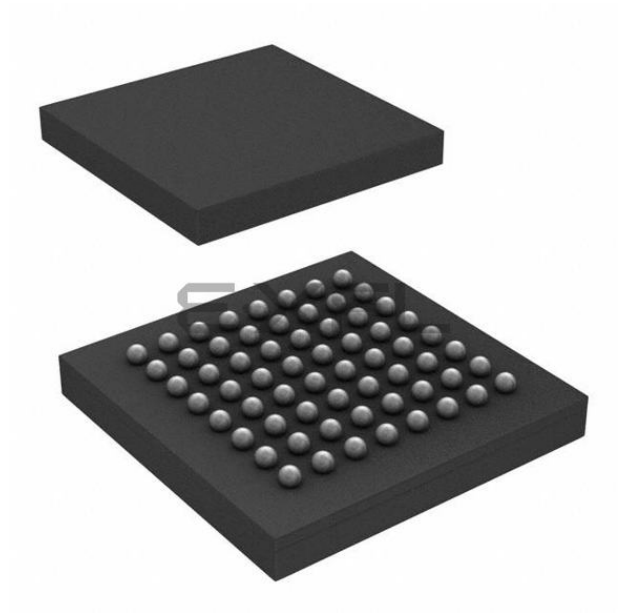

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 19x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA
Supplier Device Package	64-UFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f058r8h6tr

List of tables

3 Functional overview

Figure 1 shows the general block diagram of the STM32F058C8/R8/T8 devices.

3.1 ARM®-Cortex®-M0 core

The ARM® Cortex®-M0 is a generation of ARM 32-bit RISC processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The STM32F058C8/R8/T8 devices embed ARM core and are compatible with all ARM tools and software.

3.2 Memories

The device has the following features:

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 64 Kbytes of embedded Flash memory for programs and data
  - Option bytes

  The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex®-M0 serial wire) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- boot from User Flash memory
- boot from System Memory
- boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15 or PA9/PA10.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop mode.

3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

3.10.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.11 Digital-to-analog converter (DAC)

The 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This digital Interface supports the following features:

- Left or right data alignment in 12-bit mode
- Synchronized update capability
- DMA capability
- External triggers for conversion

Five DAC trigger inputs are used in the device. The DAC is triggered through the timer trigger outputs and the DAC interface is generating its own DMA requests.

3.12 Comparators (COMP)

The device embeds two fast rail-to-rail low-power comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pins
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).Refer to *Table 21: Embedded internal reference voltage* for the value and precision of the internal reference voltage.

Both comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

3.13 Touch sensing controller (TSC)

The STM32F058C8/R8/T8 devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 17 capacitive sensing channels distributed over 6 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists in charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the

Table 12. Pin definitions (continued)

Pin number				Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	UFBGA64	UFQFPN48	WLCSP36					Alternate functions	Additional functions
36	F7	28	-	PB15	I/O	FT	(5)	SPI2_MOSI, TIM1_CH3N, TIM15_CH1N, TIM15_CH2	RTC_REFIN
37	F6	-	-	PC6	I/O	FT	-	TIM3_CH1	-
38	E7	-	-	PC7	I/O	FT	-	TIM3_CH2	-
39	E8	-	-	PC8	I/O	FT	-	TIM3_CH3	-
40	D8	-	-	PC9	I/O	FT	-	TIM3_CH4	-
41	D7	29	E2	PA8	I/O	FT	-	USART1_CK, TIM1_CH1, EVENTOUT, MCO	-
42	C7	30	D1	PA9	I/O	FT	-	USART1_TX, TIM1_CH2, TIM15_BKIN, TSC_G4_IO1	-
43	C6	31	C1	PA10	I/O	FT	-	USART1_RX, TIM1_CH3, TIM17_BKIN, TSC_G4_IO2	-
44	C8	32	C2	PA11	I/O	FT	-	USART1_CTS, TIM1_CH4, COMP1_OUT, TSC_G4_IO3, EVENTOUT	-
45	B8	33	A1	PA12	I/O	FT	-	USART1_RTS, TIM1_ETR, COMP2_OUT, TSC_G4_IO4, EVENTOUT	-
46	A8	34	B1	PA13 (SWDIO)	I/O	FT	**(6)**	IR_OUT, SWDIO	-
47	D6	35	-	PF6	I/O	FT	-	I2C2_SCL	-
48	E6	36	-	PF7	I/O	FT	-	I2C2_SDA	-
49	A7	37	B2	PA14 (SWCLK)	I/O	FT	(6)	USART2_TX, SWCLK	-
50	A6	38	A2	PA15	I/O	FT	-	SPI1_NSS, I2S1_WS, USART2_RX, TIM2_CH1_ETR, EVENTOUT	-
51	B7	-	-	PC10	I/O	FT	-	-	-
52	B6	-	-	PC11	I/O	FT	-	-	-
53	C5	-	-	PC12	I/O	FT	-	-	-
54	B5	-	-	PD2	I/O	FT	-	TIM3_ETR	-
55	A5	39	B3	PB3	I/O	FT	-	SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT	-

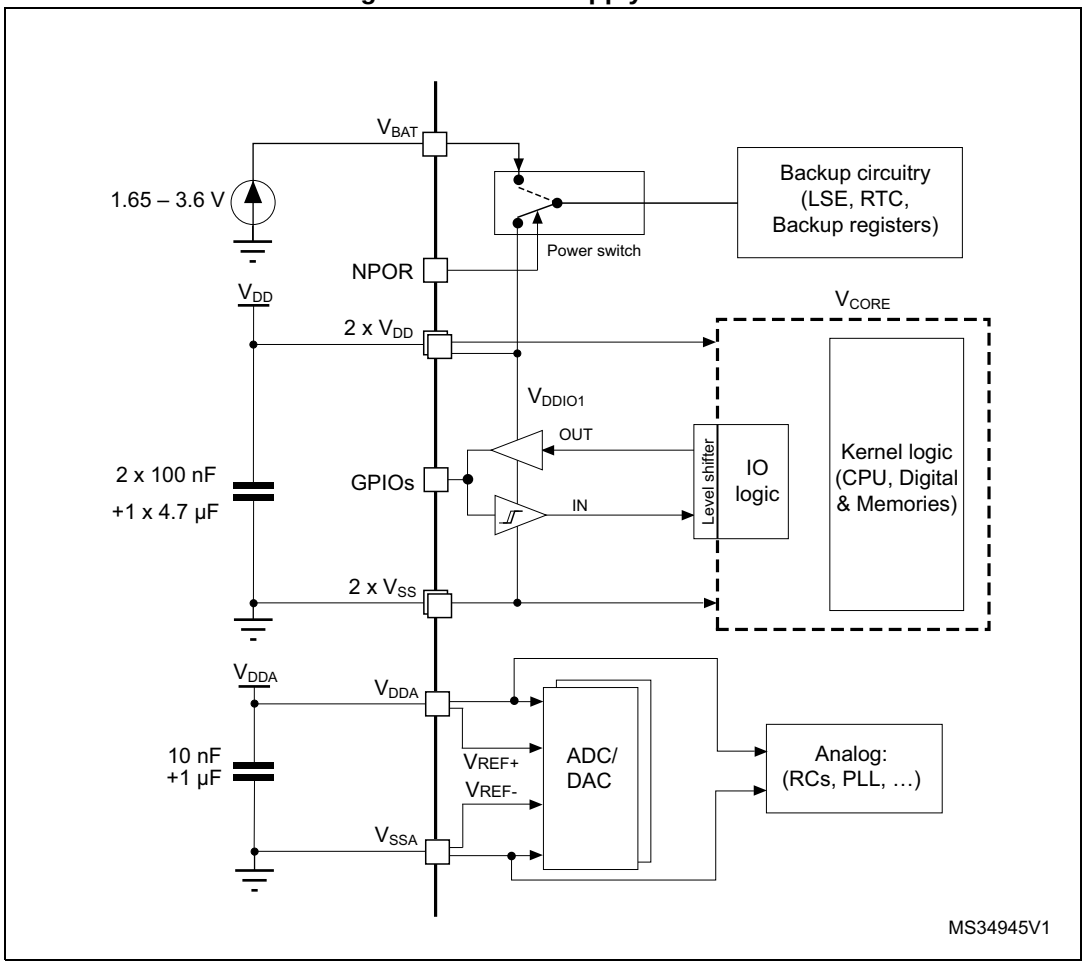
Table 12. Pin definitions (continued)

Pin number				Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	UFBGA64	UFQFPN48	WLCSP36					Alternate functions	Additional functions
56	A4	40	A3	PB4	I/O	FT	-	SPI1_MISO, I2S1_MCK, TIM3_CH1, TSC_G5_IO2, EVENTOUT	-
57	C4	41	E6	PB5	I/O	FT	-	SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	-
58	D3	42	C4	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_IO3	-
59	C3	43	A4	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, TIM17_CH1N, TSC_G5_IO4	-
60	B4	44	B4	BOOT0	I	B	-	Boot memory selection	
61	B3	45	-	PB8	I/O	FTf	(5)	I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC	-
62	A3	46	-	PB9	I/O	FTf	(5)	I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT	-
63	D5	47	D6	VSS	S	-	-	Ground	
64	E5	48	A5	VDD	S	-	-	Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After the first RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the main reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the reference manual.
3. Distinct VSSA pin is not available on WLCSP36 package. The pin number corresponds to the VSS pin to which VSSA pad of the silicon die is connected.
4. This pin is powered by V_{DDA}.
5. On the WLCSP36 package, PB8, PB9, PB10, PB11, PB12, PB13, PB14 and PB15 must be set to defined levels by software, as their corresponding pads on the silicon die are left unconnected. Apply the same recommendations as for unconnected pins.
6. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.

6.1.6 Power supply scheme

Figure 10. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Table 22. Typical and maximum current consumption from V_{DD} at 1.8 V (continued)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Sleep mode	HSE bypass, PLL on	48 MHz	12.5	13.7	14.4	14.9	2.7	2.9	3.0	3.2	mA
			32 MHz	8.8	9.3	9.7	10.1	1.8	2.0	2.2	2.3	
			24 MHz	6.8	7.3	7.7	8.1	1.5	1.5	1.6	1.7	
		HSE bypass, PLL off	8 MHz	2.2	2.6	2.8	3.0	0.5	0.6	0.6	0.6	
			1 MHz	0.3	0.4	0.4	0.5	0.1	0.2	0.2	0.2	
		HSI clock, PLL on	48 MHz	12.6	13.8	14.5	15.1	2.8	2.9	3.1	3.3	
			32 MHz	8.8	9.5	9.8	10.2	1.9	2.1	2.2	2.4	
			24 MHz	6.9	7.4	7.8	8.1	1.5	1.6	1.7	1.8	
		HSI clock, PLL off	8 MHz	2.3	2.7	2.9	3.1	0.5	0.6	0.7	0.8	

1. Data based on characterization results, not tested in production unless otherwise specified.

Table 23. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	VDDA = 2.4 V				VDDA = 3.6 V				Unit
				Typ	Max @ TA(2)			Typ	Max @ TA(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run or Sleep mode, code executing from Flash memory or RAM	External clock (HSE bypass)	48 MHz	148	169	179	183	162	183	195	198	µA
			32 MHz	103	121	126	128	111	129	135	138	
			24 MHz	81	96	100	103	87	102	106	108	
			8 MHz	1.0	3.0	3.0	3.0	2.0	3.0	3.0	4.0	
			1 MHz	1.0	2.0	2.0	2.0	2.0	2.0	3.0	3.0	
		Internal clock (HSI)	48 MHz	218	240	251	255	242	263	275	278	
			32 MHz	172	191	199	202	191	209	215	218	
			24 MHz	150	168	173	175	166	183	190	192	
			8 MHz	70	80	82	83	82	91	94	95	

1. Current consumption from the VDDA supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, IDDA is independent from the frequency.
2. Data based on characterization results, not tested in production unless otherwise specified.

Table 24. Typical and maximum consumption in Stop mode

Symbol	Parameter	Conditions	Typ. @ V_{DD} = 1.8 V							Max			Unit
			V_{DDA} = 1.8 V	V_{DDA} = 2.0 V	V_{DDA} = 2.4 V	V_{DDA} = 2.7 V	V_{DDA} = 3.0 V	V_{DDA} = 3.3 V	V_{DDA} = 3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	All oscillators OFF	0.5							2.3	15	36	µA
I_{DDA}			0.8	0.8	0.8	0.9	0.9	1.0	1.1	1.6	3.6	3.4	

Table 25. Typical and maximum current consumption from the V_{BAT} supply

Symbol	Parameter	Conditions	Typ @ V_{BAT}						Max(1)			Unit
			1.65 V	1.8 V	2.4 V	2.7 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_VBAT}	RTC domain supply current	LSE & RTC ON; “Xtal mode”: lower driving capability; LSEDRV[1:0] = '00'	0.5	0.5	0.6	0.7	0.8	0.9	1.0	1.3	1.7	µA
		LSE & RTC ON; “Xtal mode” higher driving capability; LSEDRV[1:0] = '11'	0.8	0.8	0.9	1.0	1.1	1.2	1.3	1.6	2.1	

1. Data based on characterization results, not tested in production.

Typical current consumption

The MCU is placed under the following conditions:

- V_{DD} = V_{DDA} = 1.8 V
- All I/O pins are in analog input configuration
- The Flash memory access time is adjusted to f_{HCLK} frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, f_{PCLK} = f_{HCLK}
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 32*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 32. HSE oscillator characteristics

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
I_{DD}	HSE current consumption	During startup(3)	-	-	8.5	mA
		V_{DD} = 1.8 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.4	-	
		V_{DD} = 1.8 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.5	-	
		V_{DD} = 1.8 V, Rm = 30 Ω, CL = 5 pF@32 MHz	-	0.8	-	
		V_{DD} = 1.8 V, Rm = 30 Ω, CL = 10 pF@32 MHz	-	1	-	
		V_{DD} = 1.8 V, Rm = 30 Ω, CL = 20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

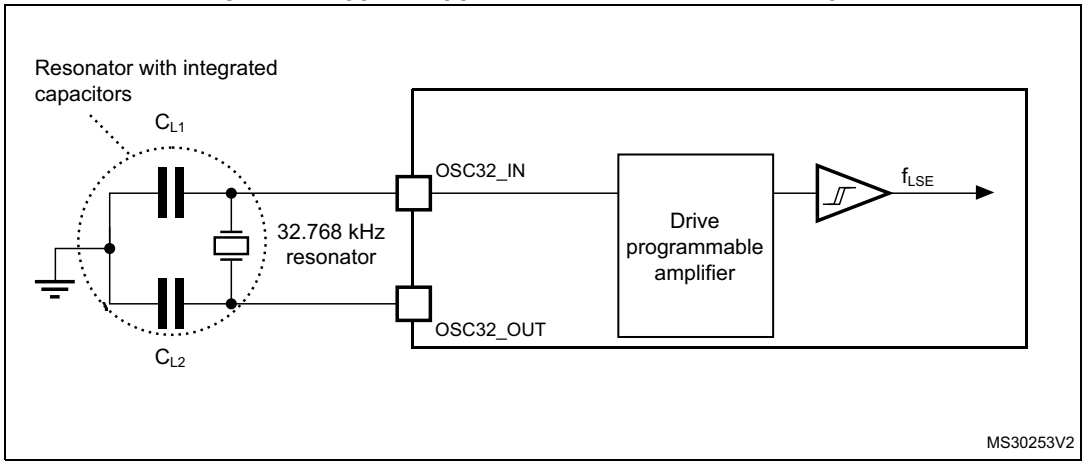
1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 14*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 15. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.7 Internal clock source characteristics

The parameters given in *Table 34* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19: General operating conditions*. The provided curves are characterization results, not tested in production.

Table 49. NPOR pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NPOR)}$	NPOR Input low level voltage	-	-	-	0.475 V_{DDA} - 0.2(1)	V
$V_{IH(NPOR)}$	NPOR Input high level voltage	-	0.5 V_{DDA} + 0.2(1)	-	-	
$V_{hys(NPOR)}$	NPOR Schmitt trigger voltage hysteresis	-	-	100(1)	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

6.3.15 12-bit ADC characteristics

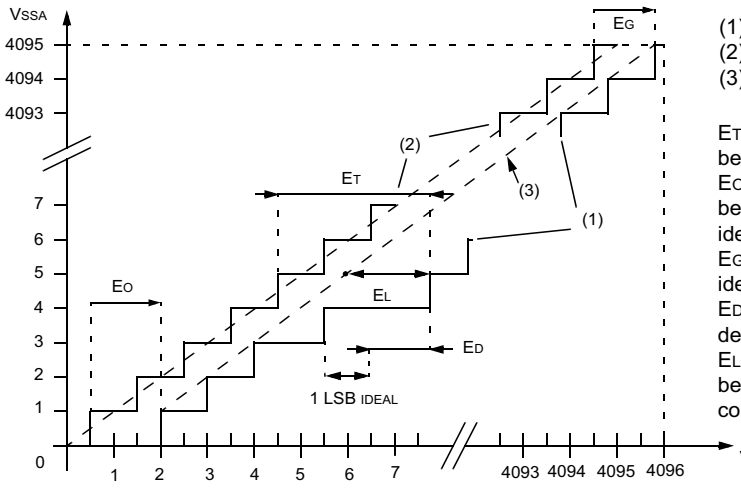
Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the conditions summarized in *Table 19: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 50. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	-	2.4	-	3.6	V
$I_{DDA\ (ADC)}$	Current consumption of the ADC(1)	V_{DDA} = 3.3 V	-	0.9	-	mA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	12-bit resolution	0.043	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz, 12-bit resolution	-	-	823	kHz
		12-bit resolution	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 51* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)(3)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$

Figure 22. ADC accuracy characteristics

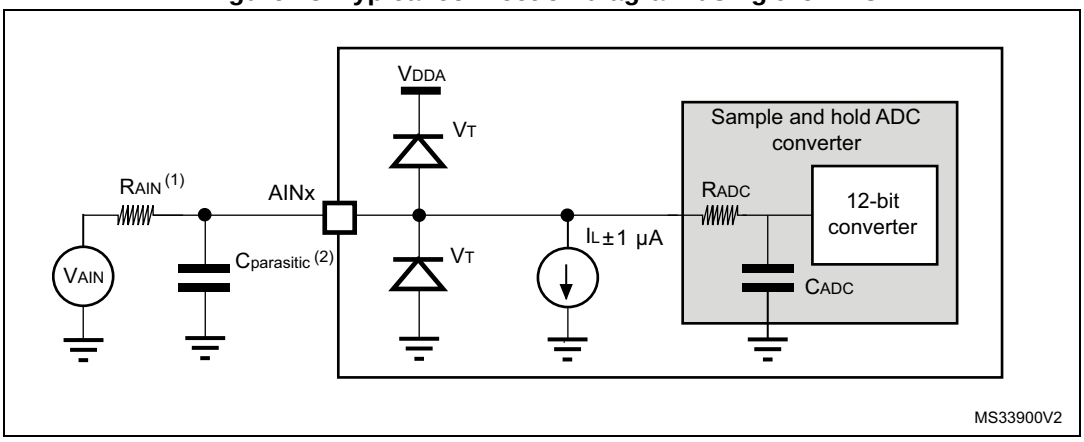


(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

E_T = Total Unajusted Error: maximum deviation between the actual and ideal transfer curves.
E_O = Offset Error: maximum deviation between the first actual transition and the first ideal one.
E_G = Gain Error: deviation between the last ideal transition and the last actual one.
E_D = Differential Linearity Error: maximum deviation between actual steps and the ideal ones.
E_L = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

MS19880V2

Figure 23. Typical connection diagram using the ADC



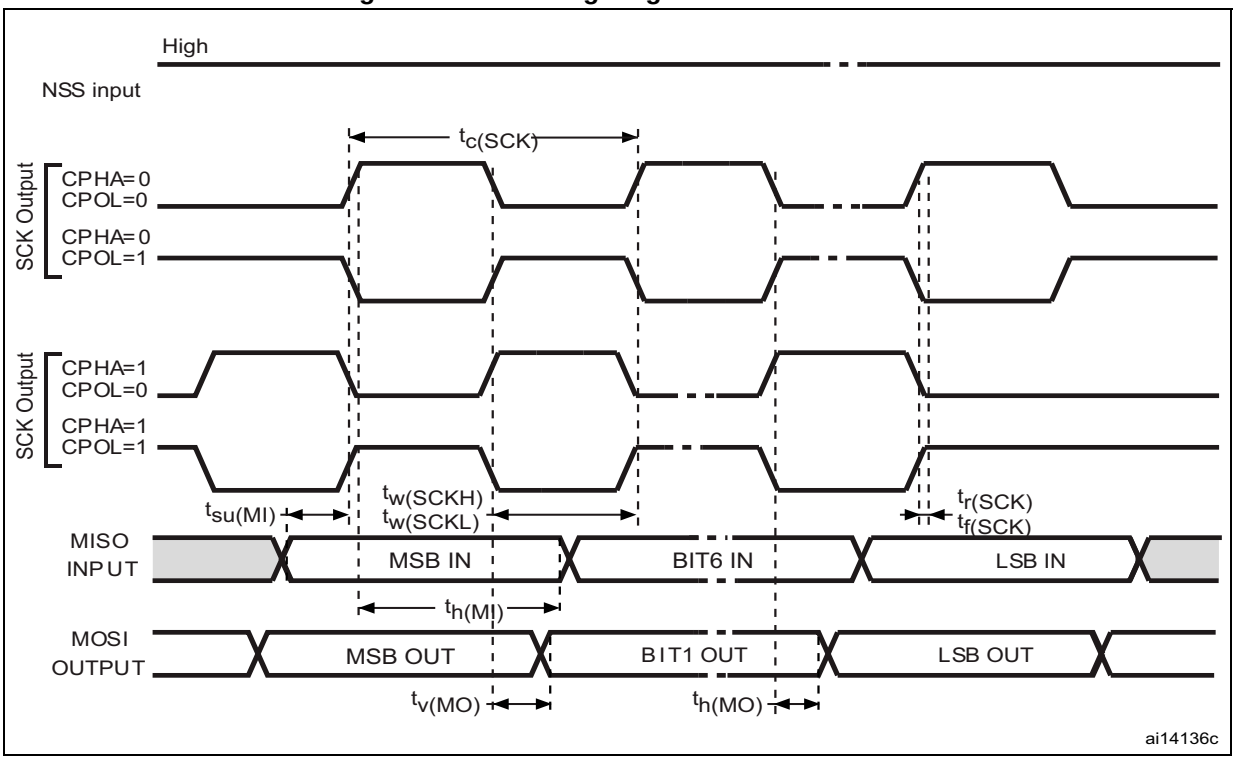
MS33900V2

1. Refer to *Table 50: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 10: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

Figure 28. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 62. I^2S characteristics(1)

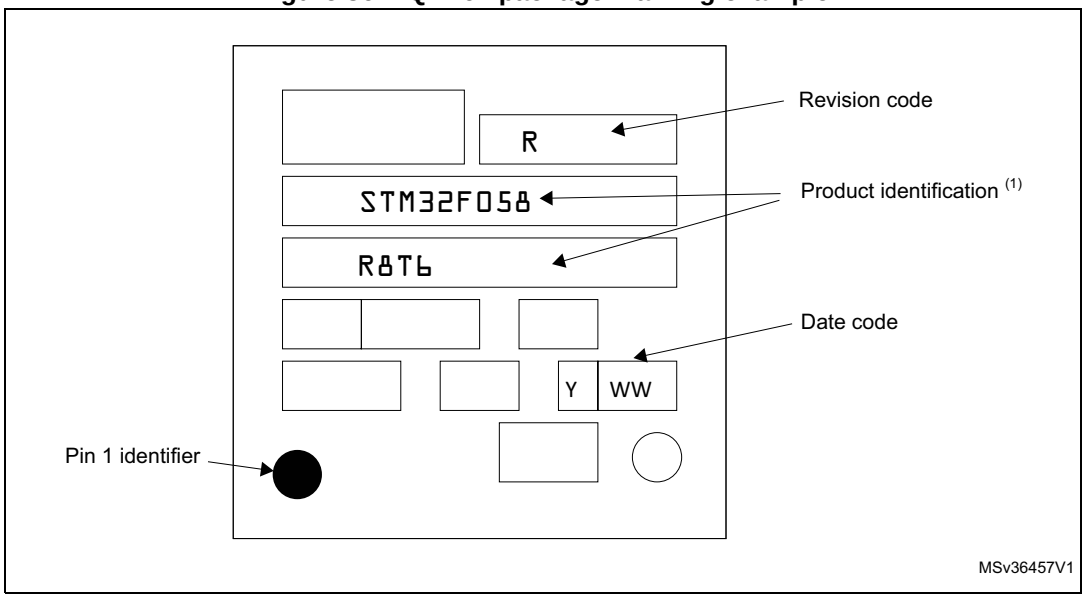
Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.597	1.601	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$	I^2S clock rise time	Capacitive load C_L = 15 pF	-	10	ns
$t_{f(CK)}$	I^2S clock fall time		-	12	
$t_{w(CKH)}$	I^2S clock high time	Master f_{PCLK}= 16 MHz, audio frequency = 48 kHz	306	-	
$t_{w(CKL)}$	I^2S clock low time		312	-	
$t_{v(WS)}$	WS valid time	Master mode	2	-	
$t_{h(WS)}$	WS hold time	Master mode	2	-	
$t_{su(WS)}$	WS setup time	Slave mode	7	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
DuCy(SCK)	I^2S slave input clock duty cycle	Slave mode	25	75	%

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 36. LQFP64 package marking example

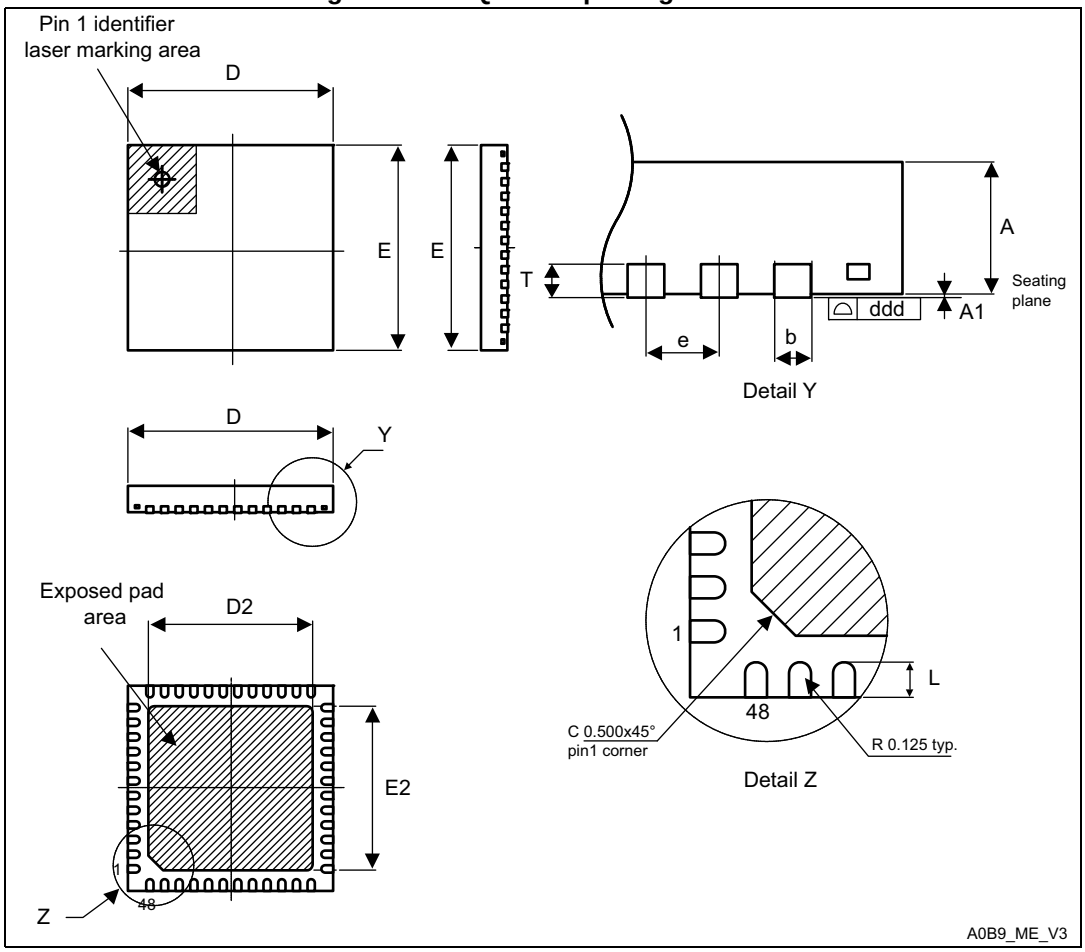


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.3 UFQFPN48 package information

UFQFPN48 is a 48-lead, 7x7 mm, 0.5 mm pitch, ultra-thin fine-pitch quad flat package.

Figure 37. UFQFPN48 package outline



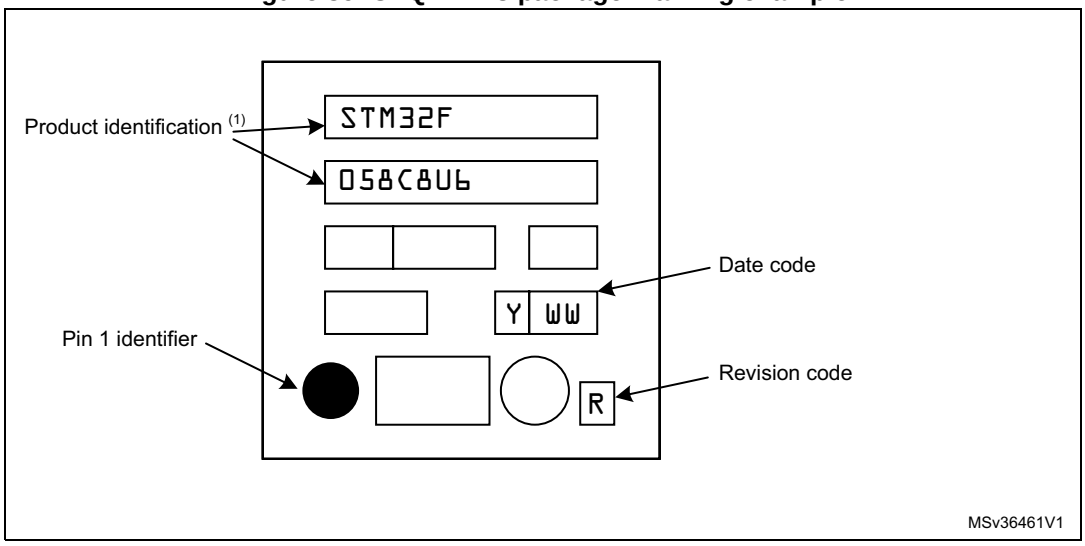
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 39. UFQFPN48 package marking example



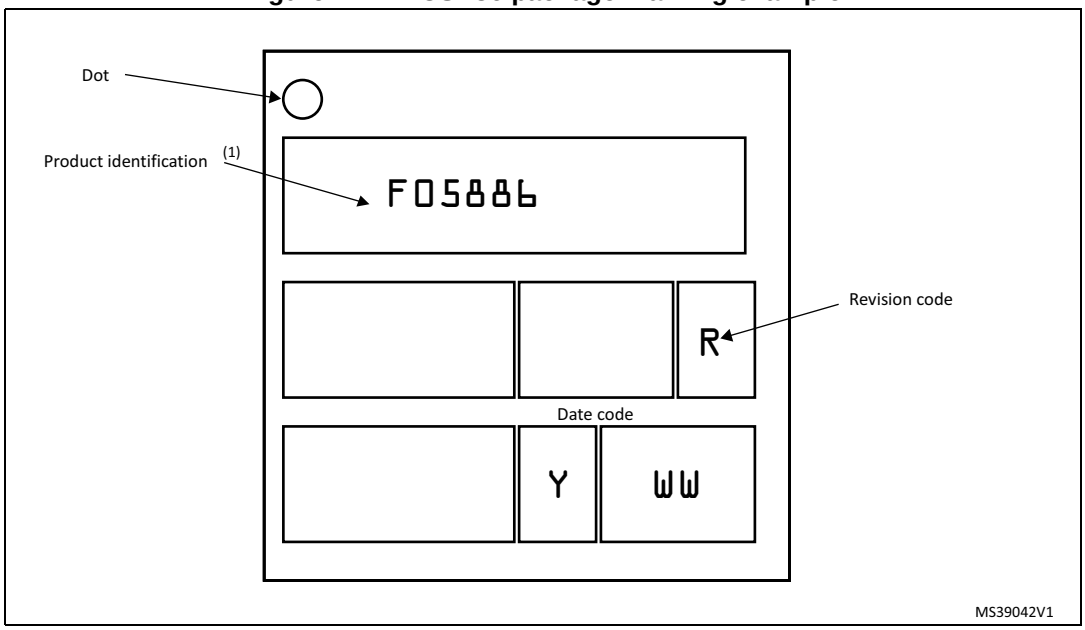
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

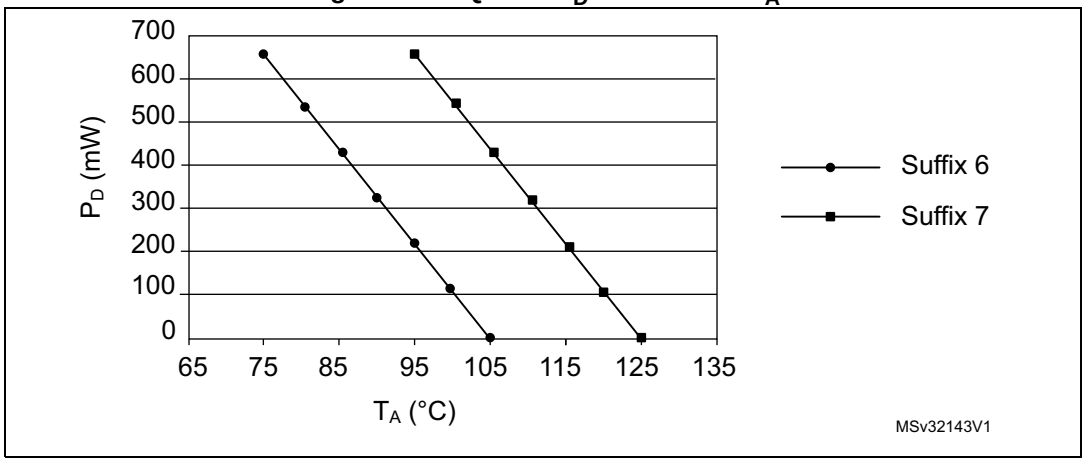
Figure 42. WLCSP36 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Refer to *Figure 43* to select the required temperature range (suffix 6 or 7) according to your ambient temperature or power requirements.

Figure 43. LQFP64 P_D max versus T_A



8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 70. Ordering information scheme

Example: STM32 F 058 R 8 T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

058 = STM32F058xx

Pin count

T = 36 pins

C = 48 pins

R = 64 pins

User code memory size

8 = 64 Kbyte

Package

H = UFBGA

T = LQFP

U = UFQFPN

Y = WLCSP

Temperature range

6 = –40 °C to +85 °C

7 = –40 °C to +105 °C

Options

xxx = code ID of programmed parts (includes packing type)

TR = tape and reel packing

blank = tray packing