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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 13x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-UFBGA, WLCSP
Supplier Device Package	36-WLCSP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f058t8y6tr

2 Description

The STM32F058C8/R8/T8 microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (64 Kbytes of Flash memory and 8 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (up to two I^2Cs, up to two SPIs, one I^2S, one HDMI CEC and up to two USARTs), one 12-bit ADC, one 12-bit DAC, six 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F058C8/R8/T8 microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges at a 1.8 V ± 8% power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F058C8/R8/T8 microcontrollers include devices in four different packages ranging from 36 pins to 64 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

These features make the STM32F058C8/R8/T8 microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.

Table 1. STM32F058C8/R8/T8 family device features and peripheral counts

<table>
<tr><th colspan="2">Peripheral</th><th>STM32F058T8</th><th>STM32F058C8</th><th>STM32F058R8</th></tr>
<tr><td colspan="2">Flash memory (Kbyte)</td><td colspan="3">64</td></tr>
<tr><td colspan="2">SRAM (Kbyte)</td><td colspan="3">8</td></tr>
<tr><td rowspan="3">Timers</td><td>Advanced control</td><td colspan="3">1 (16-bit)</td></tr>
<tr><td>General purpose</td><td colspan="3">5 (16-bit)
1 (32-bit)</td></tr>
<tr><td>Basic</td><td colspan="3">1 (16-bit)</td></tr>
<tr><td rowspan="4">Comm. interfaces</td><td>SPI [I^2S](1)</td><td>1 [1]</td><td colspan="2">2 [1]</td></tr>
<tr><td>I^2C</td><td colspan="3">2</td></tr>
<tr><td>USART</td><td colspan="3">2</td></tr>
<tr><td>CEC</td><td colspan="3">1</td></tr>
<tr><td colspan="2">12-bit ADC
(number of channels)</td><td colspan="2">1
(10 ext. + 3 int.)</td><td>1
(16 ext. + 3 int.)</td></tr>
<tr><td colspan="2">12-bit DAC
(number of channels)</td><td colspan="3">1
(1)</td></tr>
<tr><td colspan="2">Analog comparator</td><td colspan="3">2</td></tr>
<tr><td colspan="2">GPIOs</td><td>28</td><td>38</td><td>54</td></tr>
<tr><td colspan="2">Capacitive sensing channels</td><td>13</td><td>16</td><td>17</td></tr>
<tr><td colspan="2">Max. CPU frequency</td><td colspan="3">48 MHz</td></tr>
<tr><td colspan="2">Operating voltage</td><td colspan="3">V_{DD} = 1.8 V ± 8%, V_{DDA} = from V_{DD} to 3.6 V</td></tr>
<tr><td colspan="2">Operating temperature</td><td colspan="3">Ambient operating temperature: -40°C to 85°C / -40°C to 105°C
Junction temperature: -40°C to 105°C / -40°C to 125°C</td></tr>
<tr><td colspan="2">Packages</td><td>WLCSP36</td><td>UFQFPN48</td><td>LQFP64
UFBGA64</td></tr>
</table>

1. The SPI1 interface can be used either in SPI mode or in I^2S audio mode.

3 Functional overview

Figure 1 shows the general block diagram of the STM32F058C8/R8/T8 devices.

3.1 ARM®-Cortex®-M0 core

The ARM® Cortex®-M0 is a generation of ARM 32-bit RISC processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The STM32F058C8/R8/T8 devices embed ARM core and are compatible with all ARM tools and software.

3.2 Memories

The device has the following features:

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 64 Kbytes of embedded Flash memory for programs and data
  - Option bytes

  The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex®-M0 serial wire) and boot in RAM selection disabled

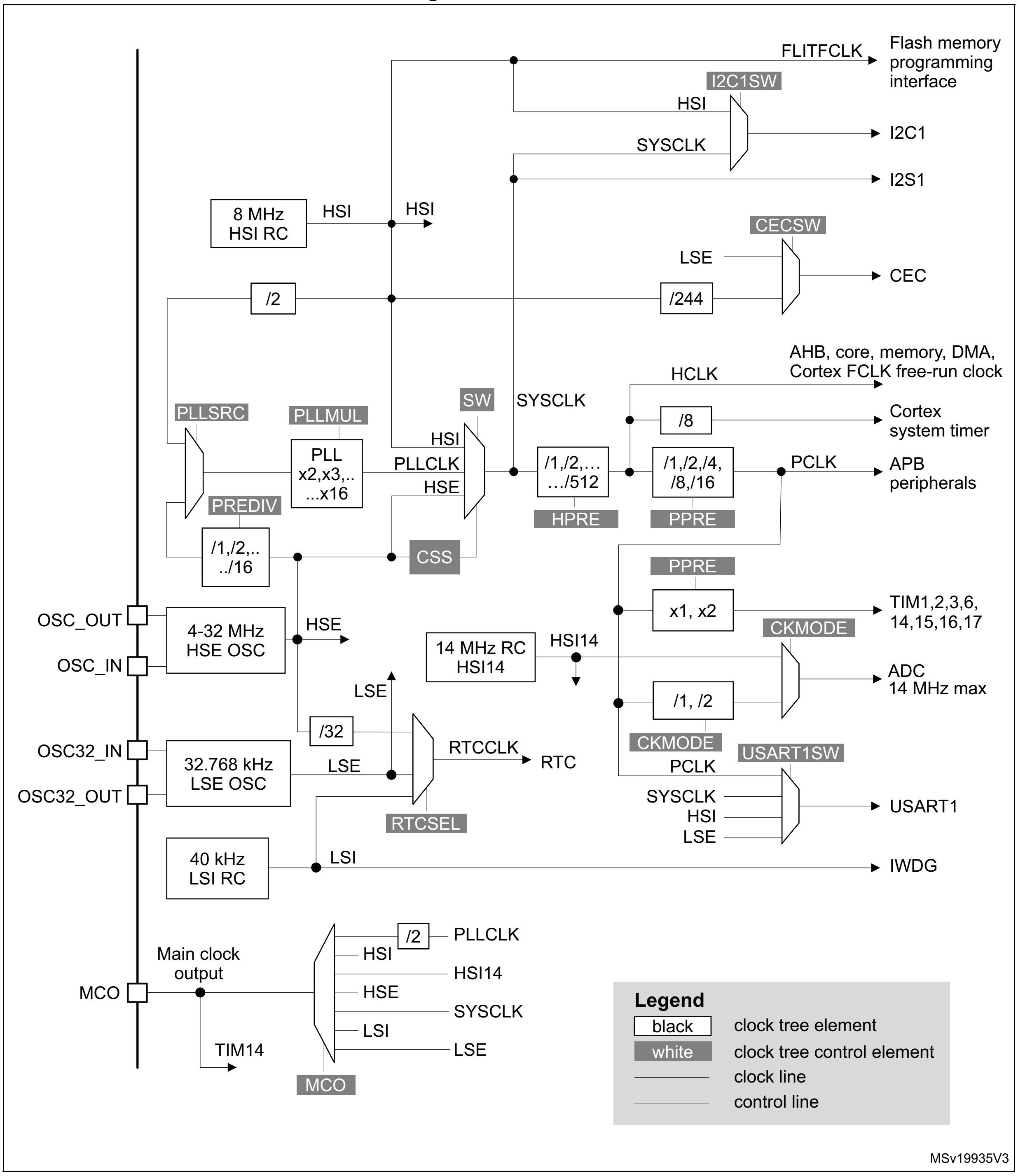
3.3 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- boot from User Flash memory
- boot from System Memory
- boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15 or PA9/PA10.

Figure 2. Clock tree



3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

3.14.2 General-purpose timers (TIM2, 3, 14, 15, 16, 17)

There are six synchronizable general-purpose timers embedded in the STM32F058C8/R8/T8 devices (see *Table 6* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3

STM32F058C8/R8/T8 devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate withTIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

3.14.3 Basic timer TIM6

This timer is mainly used for DAC trigger generation. It can also be used as a generic 16-bit time base.

3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop mode. It can be used

Table 12. Pin definitions

Pin number				Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	UFBGA64	UFQFPN48	WLCSP36					Alternate functions	Additional functions
1	B2	1	-	VBAT	S	-	-	Backup power supply	
2	A2	2	A6	PC13	I/O	TC	(1)(2)	-	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
3	A1	3	B6	PC14-OSC32_IN (PC14)	I/O	TC	(1)(2)	-	OSC32_IN
4	B1	4	C6	PC15-OSC32_OUT (PC15)	I/O	TC	(1)(2)	-	OSC32_OUT
5	C1	5	B5	PF0-OSC_IN (PF0)	I/O	FT	-	-	OSC_IN
6	D1	6	C5	PF1-OSC_OUT (PF1)	I/O	FT	-	-	OSC_OUT
7	E1	7	D5	NRST	I/O	RST	-	Device reset input / internal reset output (active low)	
8	E3	-	-	PC0	I/O	TTa	-	EVENTOUT	ADC_IN10
9	E2	-	-	PC1	I/O	TTa	-	EVENTOUT	ADC_IN11
10	F2	-	-	PC2	I/O	TTa	-	EVENTOUT	ADC_IN12
11	G1	-	-	PC3	I/O	TTa	-	EVENTOUT	ADC_IN13
12	F1	8	D6	VSSA	S	-	(3)	Analog ground	
13	H1	9	E5	VDDA	S	-	-	Analog power supply	
14	G2	10	F6	PA0	I/O	TTa	-	USART2_CTS, TIM2_CH1_ETR, COMP1_OUT, TSC_G1_IO1	ADC_IN0, COMP1_INM6, RTC_TAMP2, WKUP1
15	H2	11	D4	PA1	I/O	TTa	-	USART2_RTS, TIM2_CH2, TSC_G1_IO2, EVENTOUT	ADC_IN1, COMP1_INP
16	F3	12	E4	PA2	I/O	TTa	-	USART2_TX, TIM2_CH3, TIM15_CH1, COMP2_OUT, TSC_G1_IO3	ADC_IN2, COMP2_INM6
17	G3	13	F5	PA3	I/O	TTa	-	USART2_RX, TIM2_CH4, TIM15_CH2, TSC_G1_IO4	ADC_IN3, COMP2_INP
18	C2	-	-	PF4	I/O	FT	-	EVENTOUT	-
19	D2	-	-	PF5	I/O	FT	-	EVENTOUT	-

Table 15. STM32F058C8/R8/T8 peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	Reserved
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	Flash memory interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG + COMP
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

6.1.7 Current consumption measurement

Figure 11. Current consumption measurement scheme

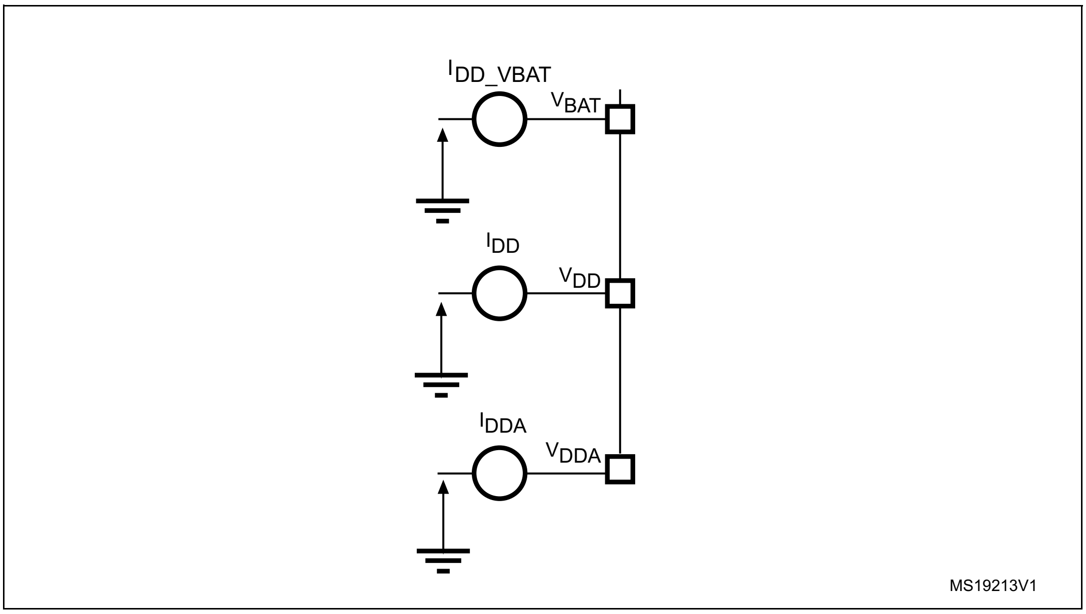


Table 20. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reference voltage

The parameters given in *Table 21* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 19: General operating conditions*.

Table 21. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.2	1.23	1.25	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10(1)	µs
$t_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	-	4(1)	-	-	µs
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DDA} = 3 V	-	-	10(1)	mV
T_{Coeff}	Temperature coefficient	-	- 100(1)	-	100(1)	ppm/°C
$T_{VREFINT\_RDY}$(2)	Internal reference voltage temporization	-	1.5	2.5	4.5	ms

1. Guaranteed by design, not tested in production.
2. Guaranteed by design, not tested in production. This parameter is the latency between the time when pin NPOR is set to 1 by the application and the time when the VREFINTRDYF status bit is set to 1 by the hardware.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 11: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Table 24. Typical and maximum consumption in Stop mode

Symbol	Parameter	Conditions	Typ. @ V_{DD} = 1.8 V							Max			Unit
			V_{DDA} = 1.8 V	V_{DDA} = 2.0 V	V_{DDA} = 2.4 V	V_{DDA} = 2.7 V	V_{DDA} = 3.0 V	V_{DDA} = 3.3 V	V_{DDA} = 3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	All oscillators OFF	0.5							2.3	15	36	µA
I_{DDA}			0.8	0.8	0.8	0.9	0.9	1.0	1.1	1.6	3.6	3.4	

Table 25. Typical and maximum current consumption from the V_{BAT} supply

Symbol	Parameter	Conditions	Typ @ V_{BAT}						Max[1]			Unit
			1.65 V	1.8 V	2.4 V	2.7 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_VBAT}	RTC domain supply current	LSE & RTC ON; “Xtal mode”: lower driving capability; LSEDRV[1:0] = '00'	0.5	0.5	0.6	0.7	0.8	0.9	1.0	1.3	1.7	µA
		LSE & RTC ON; “Xtal mode” higher driving capability; LSEDRV[1:0] = '11'	0.8	0.8	0.9	1.0	1.1	1.2	1.3	1.6	2.1	

1. Data based on characterization results, not tested in production.

Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA}$ = 1.8 V
- All I/O pins are in analog input configuration
- The Flash memory access time is adjusted to f_{HCLK} frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 28*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
  – with all peripherals clocked off
  – with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in *Table 16: Voltage characteristics*

Table 28. Peripheral current consumption

Peripheral		Typical consumption at 25 °C	Unit
AHB	BusMatrix(1)	5	µA/MHz
	DMA1	7	
	SRAM	1	
	Flash memory interface	14	
	CRC	2	
	GPIOA	9	
	GPIOB	12	
	GPIOC	2	
	GPIOD	1	
	GPIOF	1	
	TSC	6	
	All AHB peripherals	**55**	

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in Table 32. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 32. HSE oscillator characteristics

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
I_{DD}	HSE current consumption	During startup(3)	-	-	8.5	mA
		V_{DD} = 1.8 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.4	-	
		V_{DD} = 1.8 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.5	-	
		V_{DD} = 1.8 V, Rm = 30 Ω, CL = 5 pF@32 MHz	-	0.8	-	
		V_{DD} = 1.8 V, Rm = 30 Ω, CL = 10 pF@32 MHz	-	1	-	
		V_{DD} = 1.8 V, Rm = 30 Ω, CL = 20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see Figure 14). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

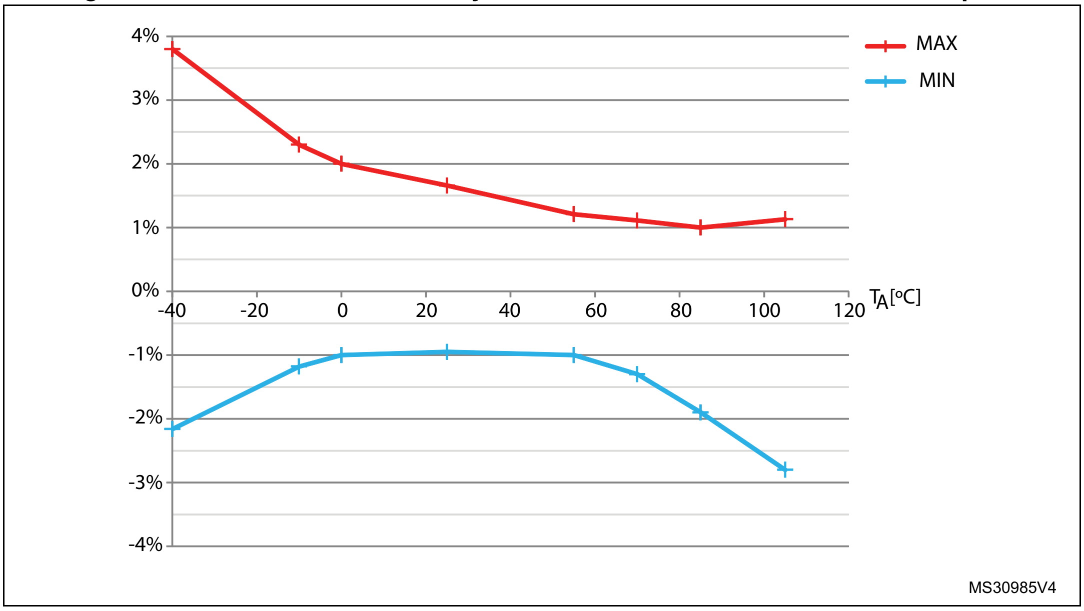
High-speed internal (HSI) RC oscillator

Table 34. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40 to 105°C	-2.8(3)	-	3.8(3)	%
		T_A = -10 to 85°C	-1.9(3)	-	2.3(3)	
		T_A = 0 to 85°C	-1.9(3)	-	2(3)	
		T_A = 0 to 70°C	-1.3(3)	-	2(3)	
		T_A = 0 to 55°C	-1(3)	-	2(3)	
		T_A = 25°C(4)	-1	-	1	
$t_{su(HSI)}$	HSI oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	100(2)	µA

1. V_{DDA} = 3.3 V, T_A = -40 to 105°C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered.

Figure 16. HSI oscillator accuracy characterization results for soldered parts



High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Table 35. HSI14 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI14}	Frequency	-	-	14	-	MHz
TRIM	HSI14 user-trimming step	-	-	-	1(2)	%
$DuCy_{(HSI14)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI14}	Accuracy of the HSI14 oscillator (factory calibrated)	T_A = –40 to 105 °C	–4.2(3)	-	5.1(3)	%
		T_A = –10 to 85 °C	–3.2(3)	-	3.1(3)	%
		T_A = 0 to 70 °C	–2.5(3)	-	2.3(3)	%
		T_A = 25 °C	–1	-	1	%
$t_{su(HSI14)}$	HSI14 oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI14)}$	HSI14 oscillator power consumption	-	-	100	150(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

Figure 17. HSI14 oscillator accuracy characterization results

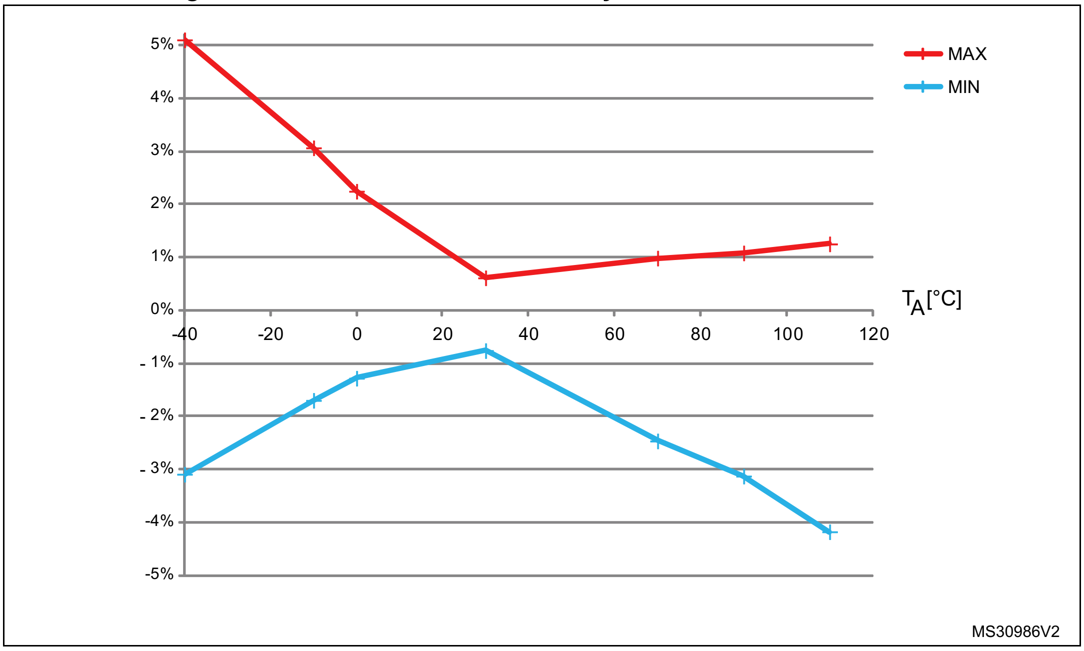


Table 44. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	–0	NA	mA
	Injected current on all FT, FTf and POR pins	–5	NA	
	Injected current on all TTa, TC and RESET pins	–5	+5	

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under the conditions summarized in *Table 19: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 45. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3\ V_{DDIOx}+0.07$(1)	V
		FT and FTf I/O	-	-	$0.475\ V_{DDIOx}-0.2$(1)	
		BOOT0	-	-	$0.3\ V_{DDIOx}-0.3$(1)	
		All I/Os except BOOT0 pin	-	-	$0.3\ V_{DDIOx}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445\ V_{DDIOx}+0.398$(1)	-	-	V
		FT and FTf I/O	$0.5\ V_{DDIOx}+0.2$(1)	-	-	
		BOOT0	$0.2\ V_{DDIOx}+0.95$(1)	-	-	
		All I/Os except BOOT0 pin	$0.7\ V_{DDIOx}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200(1)	-	mV
		FT and FTf I/O	-	100(1)	-	
		BOOT0	-	300(1)	-	
I_{lkg}	Input leakage current(2)	TC, FT and FTf I/O TTa in digital mode $V_{SS} \leq V_{IN} \leq V_{DDIOx}$	-	-	± 0.1	µA
		TTa in digital mode $V_{DDIOx} \leq V_{IN} \leq V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \leq V_{IN} \leq V_{DDA}$	-	-	± 0.2	
		FT and FTf I/O $V_{DDIOx} \leq V_{IN} \leq 5\ V$	-	-	10	

Table 45. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor (3)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)	$V_{IN} = - V_{DDIOx}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 44: I/O current injection susceptibility*.
3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 18* for standard I/Os, and in *Figure 19* for 5 V-tolerant I/Os. The following curves are design simulation results, not tested in production.

Figure 22. ADC accuracy characteristics

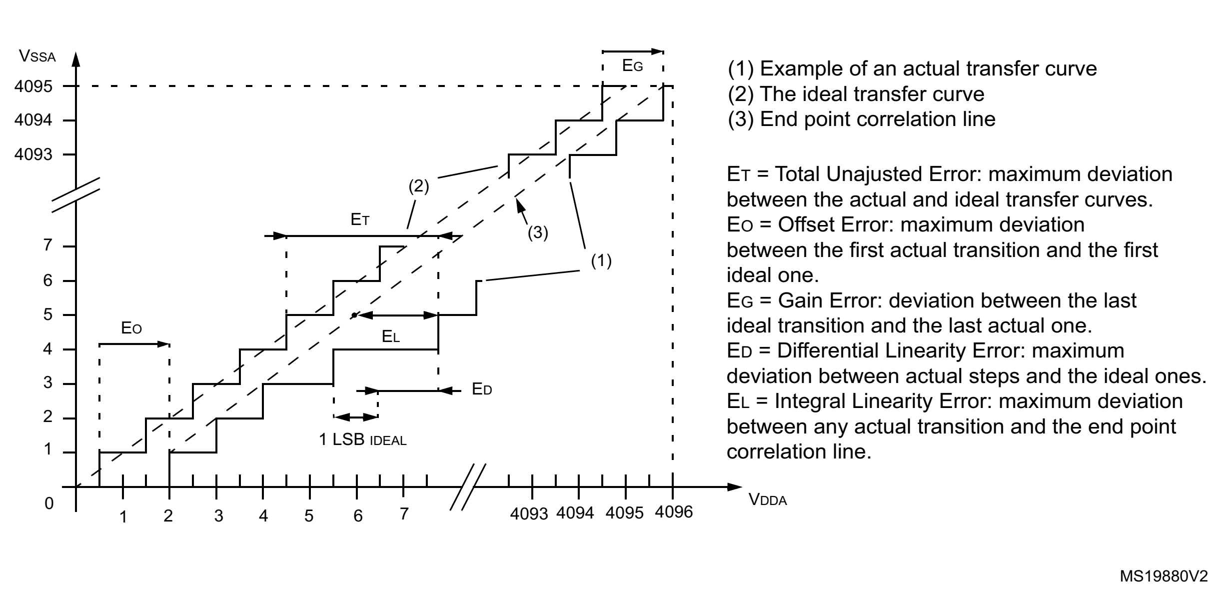
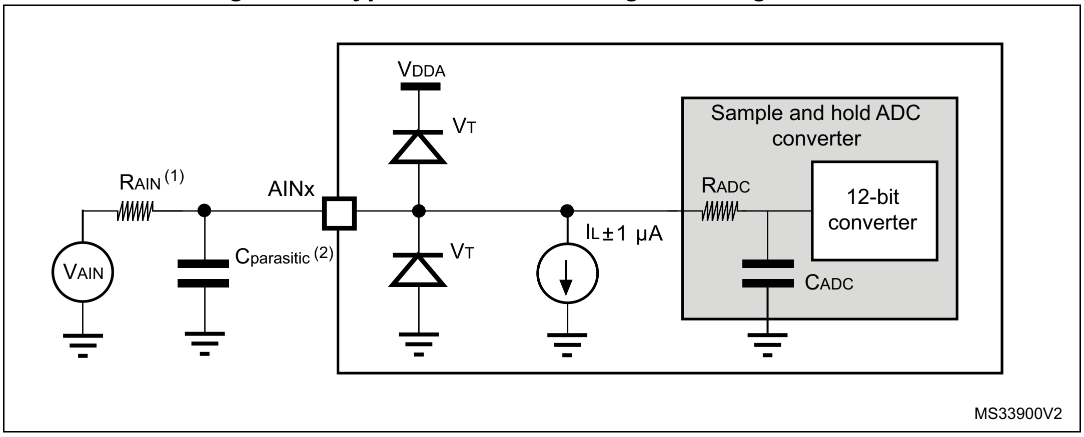


Figure 23. Typical connection diagram using the ADC



1. Refer to *Table 50: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 10: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.16 DAC electrical specifications

Table 53. DAC characteristics

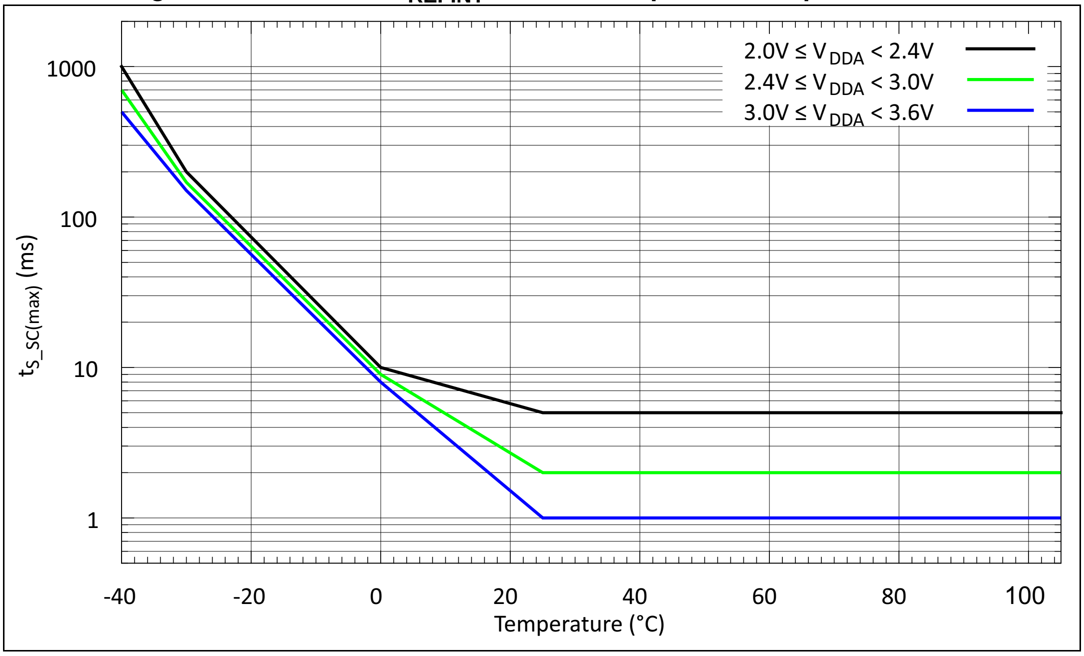
Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage for DAC ON	2.4	-	3.6	V	-
R_{LOAD} (1)	Resistive load with buffer ON	5	-	-	kΩ	Load connected to V_{SSA}
		25	-	-	kΩ	Load connected to V_{DDA}
R_O (1)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD} (1)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{DDA} = 3.6 V and (0x155) and (0xEAB) at V_{DDA} = 2.4 V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{DDA} – 1LSB	V	
I_{DDA} (1)	DAC DC current consumption in quiescent mode(2)	-	-	600	µA	With no load, middle code (0x800) on the input
		-	-	700	µA	With no load, worst code (0xF1C) on the input
DNL(3)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration
		-	-	±2	LSB	Given for the DAC in 12-bit configuration
INL(3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration
		-	-	±4	LSB	Given for the DAC in 12-bit configuration
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{DDA}/2$)	-	-	±10	mV	-
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{DDA} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{DDA} = 3.6 V

Table 54. Comparator characteristics (continued)

Symbol	Parameter	Conditions		Min(1)	Typ	Max(1)	Unit
V_{hys}	Comparator hysteresis	No hysteresis (COMPxHYST[1:0]=00)	-	-	0	-	mV
		Low hysteresis (COMPxHYST[1:0]=01)	High speed mode	3	8	13	
			All other power modes	5		10	
		Medium hysteresis (COMPxHYST[1:0]=10)	High speed mode	7	15	26	
			All other power modes	9		19	
		High hysteresis (COMPxHYST[1:0]=11)	High speed mode	18	31	49	
			All other power modes	19		40	

1. Data based on characterization results, not tested in production.
2. For more details and conditions see *Figure 25: Maximum V_{REFINT} scaler startup time from power down*.

Figure 25. Maximum V_{REFINT} scaler startup time from power down



6.3.18 Temperature sensor characteristics

Table 55. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	± 1	± 2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{30}	Voltage at 30 °C (± 5 °C)(2)	1.34	1.43	1.52	V
t_{START}(1)	ADC_IN16 buffer startup time	-	-	10	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	4	-	-	µs

1. Guaranteed by design, not tested in production.
2. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 2: Temperature sensor calibration values*.

6.3.19 V_{BAT} monitoring characteristics

Table 56. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	2 x 50	-	kΩ
Q	Ratio on V_{BAT} measurement	-	2	-	-
Er(1)	Error on Q	–1	-	+1	%
t_{S_vbat}(1)	ADC sampling time when reading the V_{BAT}	4	-	-	µs

1. Guaranteed by design, not tested in production.

6.3.20 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 57. TIMx characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	20.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}/2$	-	MHz
		$f_{TIMxCLK}$ = 48 MHz	-	24	-	MHz
t_{MAX_COUNT}	16-bit timer maximum period	-	-	2^{16}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	1365	-	µs
	32-bit counter maximum period	-	-	2^{32}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	89.48	-	s