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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I ² C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12dg128bcfu

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Section 1 Introduction

1.1 Overview

The MC9S12DT128B microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), 128K bytes of Flash EEPROM, 8K bytes of RAM, 2K bytes of EEPROM, two asynchronous serial communications interfaces (SCI), two serial peripheral interfaces (SPI), an 8-channel IC/OC enhanced capture timer, two 8-channel, 10-bit analog-to-digital converters (ADC), an 8-channel pulse-width modulator (PWM), a digital Byte Data Link Controller (BDLC), 29 discrete digital I/O channels (Port A, Port B, Port K and Port E), 20 discrete digital I/O lines with interrupt and wakeup capability, three CAN 2.0 A, B software compatible modules (MSCAN12), a Byteflight module and an Inter-IC Bus. The MC9S12DT128B has full 16-bit data paths throughout. However, the external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements.

1.2 Features

- HCS12 Core
 - 16-bit HCS12 CPU
 - i. Upward compatible with M68HC11 instruction set
 - ii. Interrupt stacking and programmer's model identical to M68HC11
 - iii. 20-bit ALU
 - iv. Instruction queue
 - v. Enhanced indexed addressing
 - MEBI (Multiplexed External Bus Interface)
 - MMC (Module Mapping Control)
 - INT (Interrupt control)
 - BKP (Breakpoints)
 - BDM (Background Debug Mode)
- CRG (Clock and Reset Generator)
 - Choice of low current Colpitts oscillator or standard Pierce Oscillator
 - PLL
 - COP watchdog
 - real time interrupt
 - clock monitor
- 8-bit and 4-bit ports with interrupt functionality

- SAE J1850 Class B Data Communications Network Interface
 - Compatible and ISO Compatible for Low-Speed (<125 Kbps) Serial Data Communications in Automotive Applications
- Inter-IC Bus (IIC)
 - Compatible with I2C Bus standard
 - Multi-master operation
 - Software programmable for one of 256 different serial clock frequencies
- 112-Pin LQFP and 80-Pin QFP package options
 - I/O lines with 5V input and drive capability
 - 5V A/D converter inputs
 - Operation at 50MHz equivalent to 25MHz Bus Speed
 - Development support
 - Single-wire background debug™ mode (BDM)
 - On-chip hardware breakpoints

1.3 Modes of Operation

User modes

- Normal and Emulation Operating Modes
 - Normal Single-Chip Mode
 - Normal Expanded Wide Mode
 - Normal Expanded Narrow Mode
 - Emulation Expanded Wide Mode
 - Emulation Expanded Narrow Mode
- Special Operating Modes
 - Special Single-Chip Mode with active Background Debug Mode
 - Special Test Mode (**Motorola use only**)
 - Special Peripheral Mode (**Motorola use only**)

Low power modes

- Stop Mode
- Pseudo Stop Mode
- Wait Mode

1.5 Device Memory Map

Table 1-1 and **Figure 1-2** show the device memory map of the MC9S12DT128B after reset. Note that after reset the EEPROM (\$0000 – \$07FF) is hidden by the register space (\$0000 - \$03FF) and the RAM (\$0000 - \$1FFF). The bottom 1K Bytes of RAM (\$0000 - \$03FF) are hidden by the register space.

Table 1-1 Device Memory Map

Address	Module	Size (Bytes)
\$0000 – \$0017	CORE (Ports A, B, E, Modes, Inits, Test)	24
\$0018 – \$0019	Reserved	2
\$001A – \$001B	Device ID register (PARTID)	2
\$001C – \$001F	CORE (MEMSIZ, IRQ, HPRI0)	4
\$0020 – \$0027	Reserved	8
\$0028 – \$002F	CORE (Background Debug Mode)	8
\$0030 – \$0033	CORE (PPAGE, Port K)	4
\$0034 – \$003F	Clock and Reset Generator (PLL, RTI, COP)	12
\$0040 – \$007F	Enhanced Capture Timer 16-bit 8 channels	64
\$0080 – \$009F	Analog to Digital Converter 10-bit 8 channels (ATD0)	32
\$00A0 – \$00C7	Pulse Width Modulator 8-bit 8 channels (PWM)	40
\$00C8 – \$00CF	Serial Communications Interface (SCI0)	8
\$00D0 – \$00D7	Serial Communications Interface (SCI1)	8
\$00D8 – \$00DF	Serial Peripheral Interface (SPI0)	8
\$00E0 – \$00E7	Inter IC Bus	8
\$00E8 – \$00EF	Byte Level Data Link Controller (BDLC)	8
\$00F0 – \$00F7	Serial Peripheral Interface (SPI1)	8
\$00F8 – \$00FF	Reserved	8
\$0100 – \$010F	Flash Control Register	16
\$0110 – \$011B	EEPROM Control Register	12
\$011C – \$011F	Reserved	4
\$0120 – \$013F	Analog to Digital Converter 10-bit 8 channels (ATD1)	32
\$0140 – \$017F	Motorola Scalable CAN (CAN0)	64
\$0180 – \$01BF	Motorola Scalable CAN (CAN1)	64
\$01C0 – \$01FF	Reserved	64
\$0200 – \$023F	Reserved	64
\$0240 – \$027F	Port Integration Module (PIM)	64
\$0280 – \$02BF	Motorola Scalable CAN (CAN4)	64
\$02C0 – \$02FF	Reserved	64
\$0300 – \$035F	Byteflight (BF)	96
\$0360 – \$03FF	Reserved	160
\$0000 – \$07FF	EEPROM array	2048
\$0000 – \$1FFF	RAM array	8192
\$4000 – \$7FFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at start	16384
\$8000 – \$BFFF	Flash EEPROM Page Window	16384

\$0034 - \$003F

CRG (Clock and Reset Generator)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0034	SYNR	Read:	0	0	SYN5	SYN4	SYN3	SYN2	SYN1	SYN0
		Write:								
\$0035	REFDV	Read:	0	0	0	0	REFDV3	REFDV2	REFDV1	REFDV0
		Write:								
\$0036	CTFLG TEST ONLY	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0037	CRGFLG	Read:	RTIF	PORF	0	LOCKIF	LOCK	TRACK	SCMIF	SCM
		Write:								
\$0038	CRGINT	Read:	RTIE	0	0	LOCKIE	0	0	SCMIE	0
		Write:								
\$0039	CLKSEL	Read:	PLLSEL	PSTP	SYSWAI	ROAWAI	PLLWAI	CWAI	RTIWAI	COPWAI
		Write:								
\$003A	PLLCTL	Read:	CME	PLLON	AUTO	ACQ	0	PRE	PCE	SCME
		Write:								
\$003B	RTICTL	Read:	0	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		Write:								
\$003C	COPCTL	Read:	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		Write:								
\$003D	FORBYP TEST ONLY	Read:	0	0	0	0	0	0	0	0
		Write:								
\$003E	CTCTL TEST ONLY	Read:	0	0	0	0	0	0	0	0
		Write:								
\$003F	ARMCOP	Read:	0	0	0	0	0	0	0	0
		Write:	Bit 7	6	5	4	3	2	1	Bit 0

\$0040 - \$007F

ECT (Enhanced Capture Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0040	TIOS	Read:	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
		Write:								
\$0041	CFORC	Read:	0	0	0	0	0	0	0	0
		Write:	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
\$0042	OC7M	Read:	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
		Write:								
\$0043	OC7D	Read:	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
		Write:								
\$0044	TCNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
\$0045	TCNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0046	TSCR1	Read:	TEN	TSWAI	TSFRZ	TFFCA	0	0	0	0
		Write:								
\$0047	TTOV	Read:	TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0
		Write:								
\$0048	TCTL1	Read:	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
		Write:								
\$0049	TCTL2	Read:	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
		Write:								

\$00D0 - \$00D7

SCI1 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$00D5	SCI1SR2	Read:	0	0	0	0	0	BRK13	TXDIR	RAF
		Write:								
\$00D6	SCI1DRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
\$00D7	SCI1DRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

\$00D8 - \$00DF

SPI0 (Serial Peripheral Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$00D8	SPI0CR1	Read:	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		Write:								
\$00D9	SPI0CR2	Read:	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		Write:								
\$00DA	SPI0BR	Read:	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		Write:								
\$00DB	SPI0SR	Read:	SPIF	0	SPTEF	MODF	0	0	0	0
		Write:								
\$00DC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$00DD	SPI0DR	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
\$00DE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$00DF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

\$00E0 - \$00E7

IIC (Inter IC Bus)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$00E0	IBAD	Read:	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
		Write:								
\$00E1	IBFD	Read:	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
		Write:								
\$00E2	IBCR	Read:	IBEN	IBIE	MS/SL	TX/RX	TXAK	0	0	IBSWAI
		Write:						RSTA		
\$00E3	IBSR	Read:	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
		Write:								
\$00E4	IBDR	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
\$00E5	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$00E6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$00E7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

\$0240 - \$027F

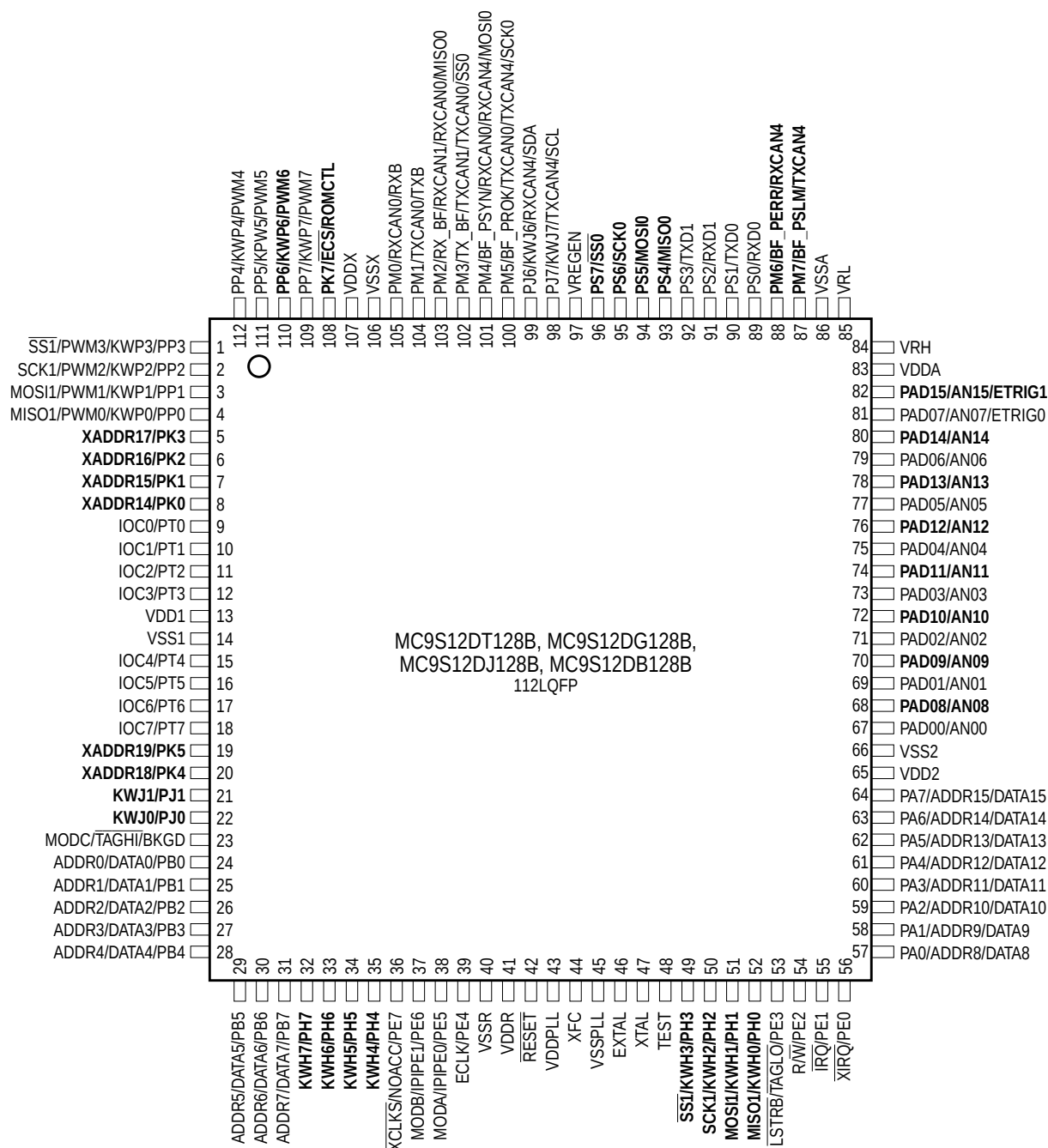
PIM (Port Integration Module)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0240	PTT	Read:	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
		Write:								
\$0241	PTIT	Read:	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
		Write:								
\$0242	DDRT	Read:	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
		Write:								
\$0243	RDRT	Read:	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
		Write:								
\$0244	PERT	Read:	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
		Write:								
\$0245	PPST	Read:	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
		Write:								
\$0246	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0247	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0248	PTS	Read:	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
		Write:								
\$0249	PTIS	Read:	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
		Write:								
\$024A	DDRS	Read:	DDRS7	DDRS6	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
		Write:								
\$024B	RDRS	Read:	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
		Write:								
\$024C	PERS	Read:	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
		Write:								
\$024D	PPSS	Read:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
		Write:								
\$024E	WOMS	Read:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
		Write:								
\$024F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0250	PTM	Read:	PTM7	PTM6	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
		Write:								
\$0251	PTIM	Read:	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
		Write:								
\$0252	DDRM	Read:	DDRM7	DDRM6	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
		Write:								
\$0253	RDRM	Read:	RDRM7	RDRM6	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
		Write:								
\$0254	PERM	Read:	PERM7	PERM6	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
		Write:								
\$0255	PPSM	Read:	PPSM7	PPSM6	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
		Write:								
\$0256	WOMM	Read:	WOMM7	WOMM6	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
		Write:								
\$0257	MODRR	Read:	0	0	MODRR5	MODRR4	MODRR3	MODRR2	MODRR1	MODRR0
		Write:								
\$0258	PTP	Read:	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
		Write:								

\$0300 - \$035F

Byteflight

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0315	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0316	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0317	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0318	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0319	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
\$031A	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
\$031B	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
\$031C	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
\$031D	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
\$031E	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
\$031F	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0320	BFTIDENT	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0321	BFTLEN	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0322 - \$032D	BFTDATA0-BFTDATA11	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$032E - \$032F	Unimplemented	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0330	BFRIDENT	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0331	BFRLEN	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0332 - \$033D	BFRDATA0-BFRDATA11	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$033E - \$033F	Unimplemented	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0340	BFFIDENT	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0341	BFFLEN	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0342 - \$034D	BFFDATA0-BFFDATA11	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$034E - \$034F	Unimplemented	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0350 - \$035F	BFBUFCTL0 - BFBUFCTL15	Read:	IFLG	IENA	LOCK	ABTAK	ABTRQ	0	0	CFG
		Write:								



Signals shown in **Bold** are not available on the 80 Pin Package

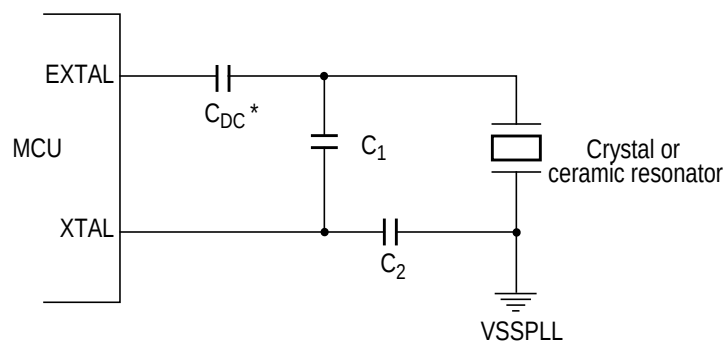
Figure 2-1 Pin assignments 112 LQFP for MC9S12DT128B, MC9S12DG128B, MC9S12DJ128B, MC9S12DB128B

2.2 Signal Properties Summary

Table 2-1 summarizes the pin functionality. Signals shown in **bold** are not available in the 80 pin package.

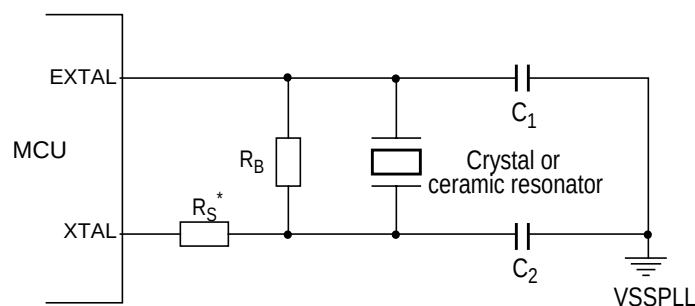
Table 2-1 Signal Properties

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Pin Name Function 5	Powered by	Internal Pull Resistor		Description
						CTRL	Reset State	
EXTAL	—	—	—	—	VDDPLL	NA	NA	Oscillator Pins
XTAL	—	—	—	—	VDDPLL	NA	NA	
RESET	—	—	—	—	VDDR	None	None	External Reset
TEST	—	—	—	—	N.A.	None	None	Test Input
VREGEN	—	—	—	—	VDDX	NA	NA	Voltage Regulator Enable Input
XFC	—	—	—	—	VDDPLL	NA	NA	PLL Loop Filter
BKGD	$\overline{\text{TAGHI}}$	MODC	—	—	VDDR	Always Up	Up	Background Debug, Tag High, Mode Input
PAD[15]	AN1[7]	ETRIG1	—	—	VDDA	None	None	Port AD Input, Analog Inputs, External Trigger Input (ATD1)
PAD[14:8]	AN1[6:0]	—	—	—	VDDA	None	None	Port AD Input, Analog Inputs (ATD1)
PAD[7]	AN0[7]	ETRIG0	—	—	VDDA	None	None	Port AD Input, Analog Inputs, External Trigger Input (ATD0)
PAD[6:0]	AN0[6:0]	—	—	—	VDDA	None	None	Port AD Input, Analog Inputs (ATD0)
PA[7:0]	ADDR[15:8]/ DATA[15:8]	—	—	—	VDDR	PUCR/ PUPAE	Disabled	Port A I/O, Multiplexed Address/Data
PB[7:0]	ADDR[7:0]/ DATA[7:0]	—	—	—	VDDR	PUCR/ PUPBE	Disabled	Port B I/O, Multiplexed Address/Data
PE7	NOACC	$\overline{\text{XCLKS}}$	—	—	VDDR	PUCR/ PUPEE	Up	Port E I/O, Access, Clock Select
PE6	IPIPE1	MODB	—	—	VDDR	While $\overline{\text{RESET}}$ pin low: Down		Port E I/O, Pipe Status, Mode Input
PE5	IPIPE0	MODA	—	—	VDDR			Port E I/O, Pipe Status, Mode Input
PE4	ECLK	—	—	—	VDDR	PUCR/ PUPEE	Up	Port E I/O, Bus Clock Output
PE3	$\overline{\text{LSTRB}}$	$\overline{\text{TAGLO}}$	—	—	VDDR	PUCR/ PUPEE	Up	Port E I/O, Byte Strobe, Tag Low
PE2	R/W	—	—	—	VDDR	PUCR/ PUPEE	Up	Port E I/O, R/W in expanded modes



* Due to the nature of a translated ground Colpitts oscillator a DC voltage bias is applied to the crystal
Please contact the crystal manufacturer for crystal DC bias conditions and recommended capacitor value C_{DC} .

Figure 2-4 Colpitts Oscillator Connections (PE7=1)



* R_S can be zero (shorted) when used with higher frequency crystals. Refer to manufacturer's data.

Figure 2-5 Pierce Oscillator Connections (PE7=0)

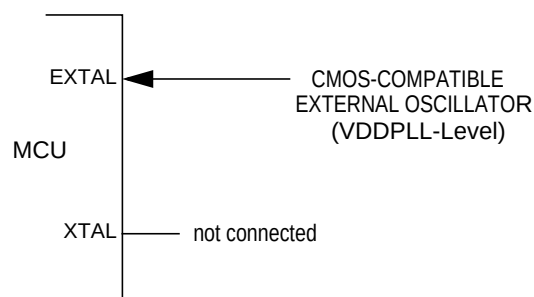


Figure 2-6 External Clock Connections (PE7=0)

2.4.4 VDDA, VSSA — Power Supply Pins for ATD and VREG

VDDA, VSSA are the power supply and ground input pins for the voltage regulator and the analog to digital converter. It also provides the reference for the internal voltage regulator. This allows the supply voltage to the ATD and the reference voltage to be bypassed independently.

2.4.5 VRH, VRL — ATD Reference Voltage Input Pins

VRH and VRL are the reference voltage input pins for the analog to digital converter.

2.4.6 VDDPLL, VSSPLL — Power Supply Pins for PLL

Provides operating voltage and ground for the Oscillator and the Phased-Locked Loop. This allows the supply voltage to the Oscillator and PLL to be bypassed independently. This 2.5V voltage is generated by the internal voltage regulator.

NOTE: No load allowed except for bypass capacitors.

2.4.7 VREGEN — On Chip Voltage Regulator Enable

Enables the internal 5V to 2.5V voltage regulator. If this pin is tied low, VDD1,2 and VDDPLL must be supplied externally.

Table A-5 Thermal Package Characteristics¹

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP112, single sided PCB ²	θ_{JA}	—	—	54	°C/W
2	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes ³	θ_{JA}	—	—	41	°C/W
3	T	Junction to Board LQFP112	θ_{JB}	—	—	31	°C/W
4	T	Junction to Case LQFP112	θ_{JC}	—	—	11	°C/W
5	T	Junction to Package Top LQFP112	Ψ_{JT}	—	—	2	°C/W
6	T	Thermal Resistance QFP 80, single sided PCB	θ_{JA}	—	—	51	°C/W
7	T	Thermal Resistance QFP 80, double sided PCB with 2 internal planes	θ_{JA}	—	—	41	°C/W
8	T	Junction to Board QFP80	θ_{JB}	—	—	27	°C/W
9	T	Junction to Case QFP80	θ_{JC}	—	—	14	°C/W
10	T	Junction to Package Top QFP80	Ψ_{JT}	—	—	3	°C/W

NOTES:

1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-3
3. PC Board according to EIA/JEDEC Standard 51-7

A.1.9 I/O Characteristics

This section describes the characteristics of all 5V I/O pins. All parameters are not always applicable, e.g. not all pins feature pull up/down resistances.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.1.10.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 25MHz bus frequency using a 4MHz oscillator in Colpitts mode. Production testing is performed using a square wave signal at the EXTAL input.

A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be

A.3.1.3 Sector Erase

Erasing a 512 byte Flash sector or a 4 byte EEPROM sector takes:

$$t_{\text{era}} \approx 4000 \cdot \frac{1}{f_{\text{NVMOP}}}$$

The setup times can be ignored for this operation.

A.3.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{\text{mass}} \approx 20000 \cdot \frac{1}{f_{\text{NVMOP}}}$$

The setup times can be ignored for this operation.

A.3.1.5 Blank Check

The time it takes to perform a blank check on the Flash or EEPROM is dependant on the location of the first non-blank word starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{\text{check}} \approx \text{location} \cdot t_{\text{cyc}} + 10 \cdot t_{\text{cyc}}$$

Table A-11 NVM Timing Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	D	External Oscillator Clock	f_{NVMOSC}	0.5		50 ¹	MHz
2	D	Bus frequency for Programming or Erase Operations	f_{NVMBUS}	1			MHz
3	D	Operating Frequency	f_{NVMOP}	150		200	kHz
4	P	Single Word Programming Time	t_{swpgm}	46 ²		74.5 ³	μs
5	D	Flash Burst Programming consecutive word ⁴	t_{bwpgm}	20.4 ²		31 ³	μs
6	D	Flash Burst Programming Time for 32 Words ⁴	t_{brpgm}	678.4 ²		1035.5 ³	μs
7	P	Sector Erase Time	t_{era}	20 ⁵		26.7 ³	ms
8	P	Mass Erase Time	t_{mass}	100 ⁵		133 ³	ms
9	D	Blank Check Time Flash per block	t_{check}	11 ⁶		32778 ⁷	t_{cyc}
10	D	Blank Check Time EEPROM per block	t_{check}	11 ⁶		2058 ⁷	t_{cyc}

NOTES:

1. Restrictions for oscillator in crystal mode apply!
2. Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus} .
3. Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f_{bus} . Refer to formulae in Sections **A.3.1.1** - **A.3.1.5** for guidance.

Table A-20 Expanded Bus Timing Characteristics

Conditions are shown in Table A-4 unless otherwise noted, C _{LOAD} = 50pF							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Frequency of operation (E-clock)	f _o	0		25.0	MHz
2	P	Cycle time	t _{cyc}	40			ns
3	D	Pulse width, E low	PW _{EL}	19			ns
4	D	Pulse width, E high ¹	PW _{EH}	19			ns
5	D	Address delay time	t _{AD}			8	ns
6	D	Address valid time to E rise (PW _{EL} –t _{AD})	t _{AV}	11			ns
7	D	Muxed address hold time	t _{MAH}	2			ns
8	D	Address hold to data valid	t _{AHDS}	7			ns
9	D	Data hold to address	t _{DHA}	2			ns
10	D	Read data setup time	t _{DSR}	13			ns
11	D	Read data hold time	t _{DHR}	0			ns
12	D	Write data delay time	t _{DDW}			7	ns
13	D	Write data hold time	t _{DHW}	2			ns
14	D	Write data setup time ⁽¹⁾ (PW _{EH} –t _{DDW})	t _{DSW}	12			ns
15	D	Address access time ⁽¹⁾ (t _{cyc} –t _{AD} –t _{DSR})	t _{ACCA}	19			ns
16	D	E high access time ⁽¹⁾ (PW _{EH} –t _{DSR})	t _{ACCE}	6			ns
17	D	Non-multiplexed address delay time	t _{NAD}			6	ns
18	D	Non-muxed address valid to E rise (PW _{EL} –t _{NAD})	t _{NAV}	15			ns
19	D	Non-multiplexed address hold time	t _{NAH}	2			ns
20	D	Chip select delay time	t _{CSD}			16	ns
21	D	Chip select access time ⁽¹⁾ (t _{cyc} –t _{CSD} –t _{DSR})	t _{ACCS}	11			ns
22	D	Chip select hold time	t _{CSH}	2			ns
23	D	Chip select negated time	t _{CSN}	8			ns
24	D	Read/write delay time	t _{RWD}			7	ns
25	D	Read/write valid time to E rise (PW _{EL} –t _{RWD})	t _{RWV}	14			ns
26	D	Read/write hold time	t _{RWH}	2			ns
27	D	Low strobe delay time	t _{LSD}			7	ns
28	D	Low strobe valid time to E rise (PW _{EL} –t _{LSD})	t _{LSV}	14			ns
29	D	Low strobe hold time	t _{LSH}	2			ns
30	D	NOACC strobe delay time	t _{NOD}			7	ns
31	D	NOACC valid time to E rise (PW _{EL} –t _{NOD})	t _{NOV}	14			ns

Appendix B Package Information

B.1 General

This section provides the physical dimensions of the MC9S12DT128B packages.

