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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12dg128bcpv

Section 1 Introduction

1.1 Overview

The MC9S12DT128B microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), 128K bytes of Flash EEPROM, 8K bytes of RAM, 2K bytes of EEPROM, two asynchronous serial communications interfaces (SCI), two serial peripheral interfaces (SPI), an 8-channel IC/OC enhanced capture timer, two 8-channel, 10-bit analog-to-digital converters (ADC), an 8-channel pulse-width modulator (PWM), a digital Byte Data Link Controller (BDLC), 29 discrete digital I/O channels (Port A, Port B, Port K and Port E), 20 discrete digital I/O lines with interrupt and wakeup capability, three CAN 2.0 A, B software compatible modules (MSCAN12), a Byteflight module and an Inter-IC Bus. The MC9S12DT128B has full 16-bit data paths throughout. However, the external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements.

1.2 Features

- HCS12 Core
  - 16-bit HCS12 CPU
    - i. Upward compatible with M68HC11 instruction set
    - ii. Interrupt stacking and programmer's model identical to M68HC11
    - iii. 20-bit ALU
    - iv. Instruction queue
    - v. Enhanced indexed addressing
  - MEBI (Multiplexed External Bus Interface)
  - MMC (Module Mapping Control)
  - INT (Interrupt control)
  - BKP (Breakpoints)
  - BDM (Background Debug Mode)
- CRG (Clock and Reset Generator)
  - Choice of low current Colpitts oscillator or standard Pierce Oscillator
  - PLL
  - COP watchdog
  - real time interrupt
  - clock monitor
- 8-bit and 4-bit ports with interrupt functionality

1.5 Device Memory Map

Table 1-1 and **Figure 1-2** show the device memory map of the MC9S12DT128B after reset. Note that after reset the EEPROM ($0000 – $07FF) is hidden by the register space ($0000 - $03FF) and the RAM ($0000 - $1FFF). The bottom 1K Bytes of RAM ($0000 - $03FF) are hidden by the register space.

Table 1-1 Device Memory Map

Address	Module	Size (Bytes)
$0000 – $0017	CORE (Ports A, B, E, Modes, Inits, Test)	24
$0018 – $0019	Reserved	2
$001A – $001B	Device ID register (PARTID)	2
$001C – $001F	CORE (MEMSIZ, IRQ, HPRIO)	4
$0020 – $0027	Reserved	8
$0028 – $002F	CORE (Background Debug Mode)	8
$0030 – $0033	CORE (PPAGE, Port K)	4
$0034 – $003F	Clock and Reset Generator (PLL, RTI, COP)	12
$0040 – $007F	Enhanced Capture Timer 16-bit 8 channels	64
$0080 – $009F	Analog to Digital Converter 10-bit 8 channels (ATD0)	32
$00A0 – $00C7	Pulse Width Modulator 8-bit 8 channels (PWM)	40
$00C8 – $00CF	Serial Communications Interface (SCI0)	8
$00D0 – $00D7	Serial Communications Interface (SCI1)	8
$00D8 – $00DF	Serial Peripheral Interface (SPI0)	8
$00E0 – $00E7	Inter IC Bus	8
$00E8 – $00EF	Byte Level Data Link Controller (BDLC)	8
$00F0 – $00F7	Serial Peripheral Interface (SPI1)	8
$00F8 – $00FF	Reserved	8
$0100 – $010F	Flash Control Register	16
$0110 – $011B	EEPROM Control Register	12
$011C – $011F	Reserved	4
$0120 – $013F	Analog to Digital Converter 10-bit 8 channels (ATD1)	32
$0140 – $017F	Motorola Scalable CAN (CAN0)	64
$0180 – $01BF	Motorola Scalable CAN (CAN1)	64
$01C0 – $01FF	Reserved	64
$0200 – $023F	Reserved	64
$0240 – $027F	Port Integration Module (PIM)	64
$0280 – $02BF	Motorola Scalable CAN (CAN4)	64
$02C0 – $02FF	Reserved	64
$0300 – $035F	Byteflight (BF)	96
$0360 – $03FF	Reserved	160
$0000 – $07FF	EEPROM array	2048
$0000 – $1FFF	RAM array	8192
$4000 – $7FFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at start	16384
$8000 – $BFFF	Flash EEPROM Page Window	16384

$0040 - $007F ECT (Enhanced Capture Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$007C	TC2H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$007D	TC2H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$007E	TC3H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$007F	TC3H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0080 - $009F ATD0 (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0080	ATD0CTL0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0081	ATD0CTL1	Read:	0	0	0	0	0	0	0	0
		Write:								
$0082	ATD0CTL2	Read:	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIG	ASCIE	ASCIF
		Write:								
$0083	ATD0CTL3	Read:	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		Write:								
$0084	ATD0CTL4	Read:	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		Write:								
$0085	ATD0CTL5	Read:	DJM	DSGN	SCAN	MULT	0	CC	CB	CA
		Write:								
$0086	ATD0STAT0	Read:	SCF	0	ETORF	FIFOR	0	CC2	CC1	CC0
		Write:								
$0087	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0088	ATD0TEST0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0089	ATD0TEST1	Read:	0	0	0	0	0	0	0	SC
		Write:								
$008A	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$008B	ATD0STAT1	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		Write:								
$008C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$008D	ATD0DIEN	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$008E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$008F	PORTAD0	Read:	Bit7	6	5	4	3	2	1	BIT 0
		Write:								
$0090	ATD0DR0H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0091	ATD0DR0L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

$00D0 - $00D7 SCI1 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D5	SCI1SR2	Read:	0	0	0	0	0	BRK13	TXDIR	RAF
		Write:								
$00D6	SCI1DRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
$00D7	SCI1DRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

$00D8 - $00DF SPI0 (Serial Peripheral Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D8	SPI0CR1	Read:	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		Write:								
$00D9	SPI0CR2	Read:	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		Write:								
$00DA	SPI0BR	Read:	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		Write:								
$00DB	SPI0SR	Read:	SPIF	0	SPTEF	MODF	0	0	0	0
		Write:								
$00DC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00DD	SPI0DR	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00DE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00DF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00E0 - $00E7 IIC (Inter IC Bus)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E0	IBAD	Read:	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
		Write:								
$00E1	IBFD	Read:	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
		Write:								
$00E2	IBCR	Read:	IBEN	IBIE	MS/$\overline{SL}$	TX/$\overline{RX}$	TXAK	0	0	IBSWAI
		Write:						RSTA		
$00E3	IBSR	Read:	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
		Write:								
$00E4	IBDR	Read:	D7	D6	D5	D4	D3	D2	D1	D 0
		Write:								
$00E5	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0120 - $013F   ATD1 (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0130	ATD1DR0H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0131	ATD1DR0L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0132	ATD1DR1H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0133	ATD1DR1L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0134	ATD1DR2H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0135	ATD1DR2L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0136	ATD1DR3H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0137	ATD1DR3L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0138	ATD1DR4H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0139	ATD1DR4L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$013A	ATD1DR5H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$013B	ATD1DR5L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$013C	ATD1DR6H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$013D	ATD1DR6L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$013E	ATD1DR7H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$013F	ATD1DR7L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

$0140 - $017F   CAN0 (Motorola Scalable CAN - MSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0140	CAN0CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:								
$0141	CAN0CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		Write:								
$0142	CAN0BTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:								
$0143	CAN0BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:								
$0144	CAN0RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:								
$0145	CAN0RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:								

$0140 - $017F CAN0 (Motorola Scalable CAN - MSCAN)

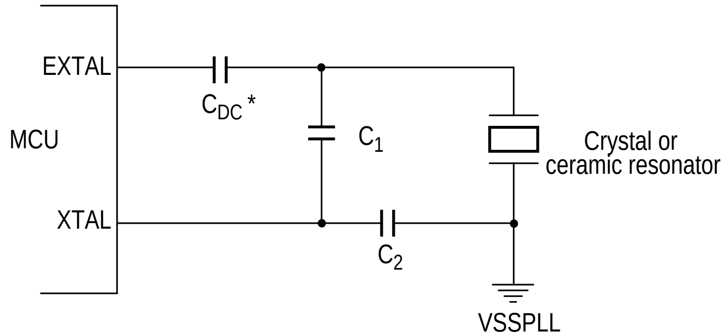
Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0146	CAN0TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:								
$0147	CAN0TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:								
$0148	CAN0TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:								
$0149	CAN0TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
$014A	CAN0TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:								
$014B	CAN0IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:								
$014C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$014D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$014E	CAN0RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								
$014F	CAN0TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
$0150 - $0153	CAN0IDAR0 - CAN0IDAR3	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0154 - $0157	CAN0IDMR0 - CAN0IDMR3	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0158 - $015B	CAN0IDAR4 - CAN0IDAR7	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$015C - $015F	CAN0IDMR4 - CAN0IDMR7	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0160 - $016F	CAN0RXFG	Read:	FOREGROUND RECEIVE BUFFER see **Table 1-2**							
		Write:								
$0170 - $017F	CAN0TXFG	Read: Write:	FOREGROUND TRANSMIT BUFFER see **Table 1-2**							

Table 1-2 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Extended ID	Read:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
$xxx0	Standard ID	Read:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
	CANxRIDR0	Write:								
	Extended ID	Read:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
$xxx1	Standard ID	Read:	ID2	ID1	ID0	RTR	IDE=0			
	CANxRIDR1	Write:								
	Extended ID	Read:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
$xxx2	Standard ID	Read:								
	CANxRIDR2	Write:								
	Extended ID	Read:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
$xxx3	Standard ID	Read:								
	CANxRIDR3	Write:								
$xxx4- $xxxB	CANxRDSR0 - CANxRDSR7	Read:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Write:								

$0300 - $035F **Byteflight**

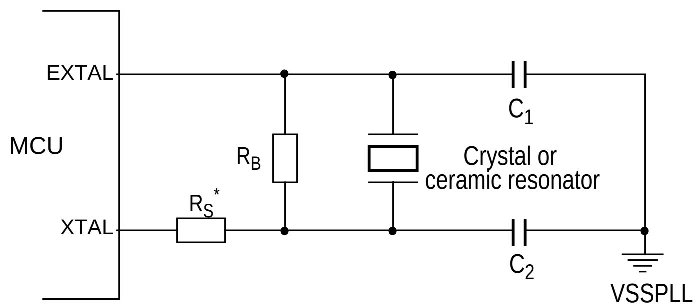
Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0315	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0316	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0317	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0318	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0319	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$031A	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$031B	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$031C	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$031D	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$031E	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$031F	Reserved for Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0320	BFTIDENT	Read: / Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0321	BFTLEN	Read: / Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0322 - $032D	BFTDATA0-BFTDATA11	Read: / Write:	Bit 7	6	5	4	3	2	1	Bit 0
$032E - $032F	Unimplemented	Read: / Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0330	BFRIDENT	Read: / Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0331	BFRLEN	Read: / Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0332 - $033D	BFRDATA0-BFRDATA11	Read: / Write:	Bit 7	6	5	4	3	2	1	Bit 0
$033E- $033F	Unimplemented	Read: / Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0340	BFFIDENT	Read: / Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0341	BFFLEN	Read: / Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0342 - $034D	BFFDATA0-BFFDATA11	Read: / Write:	Bit 7	6	5	4	3	2	1	Bit 0
$034E - $034F	Unimplemented	Read: / Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0350 - $035F	BFBUFCTL0 - BFBUFCTL15	Read:	IFLG	IENA	LOCK	ABTAK	ABTRQ	0	0	CFG
		Write:								



* Due to the nature of a translated ground Colpitts oscillator a DC voltage bias is applied to the crystal

Please contact the crystal manufacturer for crystal DC bias conditions and recommended capacitor value C_{DC}.

Figure 2-4 Colpitts Oscillator Connections (PE7=1)



* Rs can be zero (shorted) when used with higher frequency crystals. Refer to manufacturer's data.

Figure 2-5 Pierce Oscillator Connections (PE7=0)

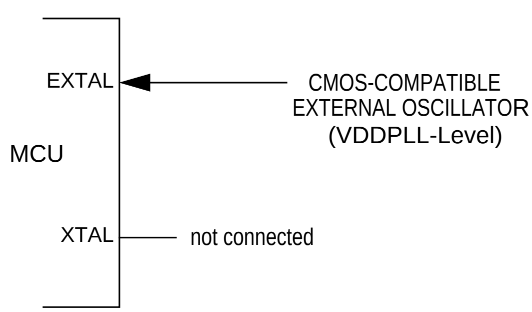


Figure 2-6 External Clock Connections (PE7=0)

Section 3 System Clock Description

3.1 Overview

The Clock and Reset Generator provides the internal clock signals for the core and all peripheral modules. **Figure 3-1** shows the clock connections from the CRG to all modules.

Consult the CRG Block User Guide for details on clock generation.

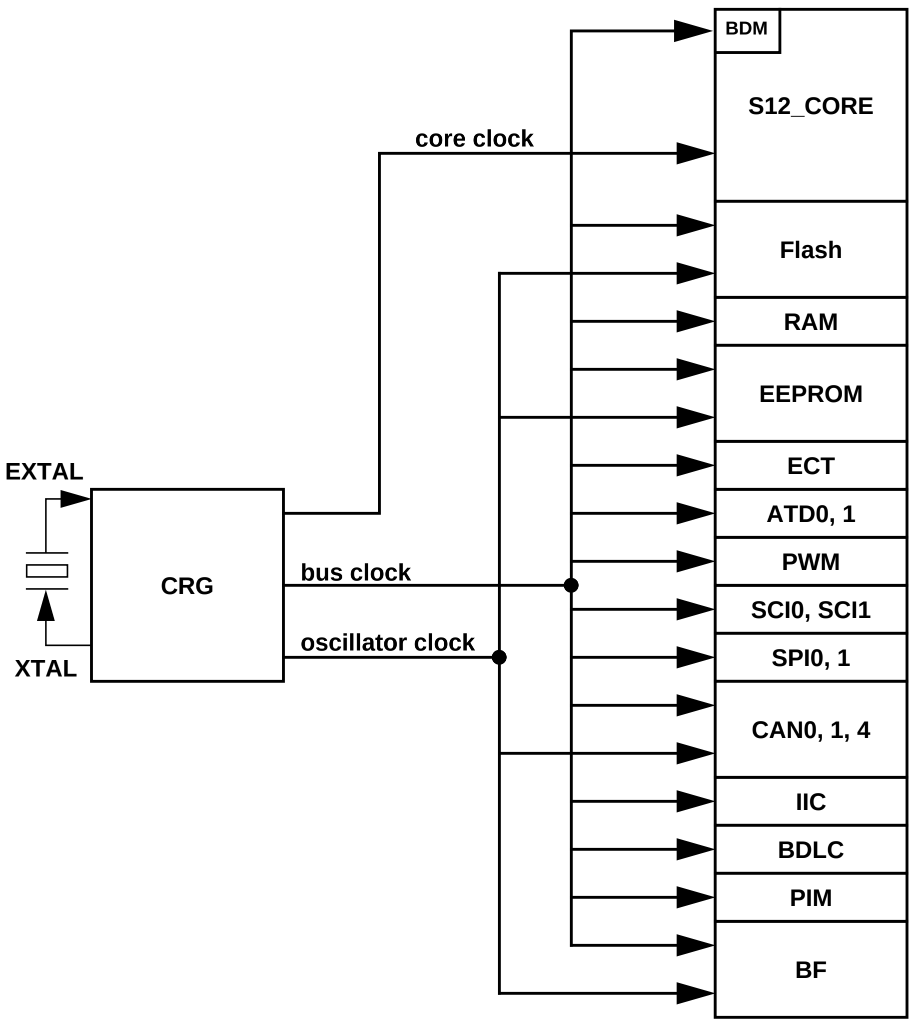


Figure 3-1 Clock Connections

Section 4 Modes of Operation

4.1 Overview

Eight possible modes determine the operating configuration of the MC9S12DT128B. Each mode has an associated default memory map and external bus configuration controlled by a further pin.

Three low power modes exist for the device.

4.2 Chip Configuration Summary

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset (**Table 4-1**). The MODC, MODB, and MODA bits in the MODE register show the current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal. The ROMCTL signal allows the setting of the ROMON bit in the MISC register thus controlling whether the internal Flash is visible in the memory map. ROMON = 1 mean the Flash is visible in the memory map. The state of the ROMCTL pin is latched into the ROMON bit in the MISC register on the rising edge of the reset signal.

Table 4-1 Mode Selection

BKGD = MODC	PE6 = MODB	PE5 = MODA	PK7 = ROMCTL	ROMON Bit	Mode Description
0	0	0	X	1	Special Single Chip, BDM allowed and ACTIVE. BDM is allowed in all other modes but a serial command is required to make BDM active.
0	0	1	X	0	Emulation Expanded Narrow, BDM allowed
0	1	0	X	0	Special Test (Expanded Wide), BDM allowed
0	1	1	X	0	Emulation Expanded Wide, BDM allowed
1	0	0	X	1	Normal Single Chip, BDM allowed
1	0	1	0	0	Normal Expanded Narrow, BDM allowed
			1	1	
1	1	0	X	1	Special Peripheral; BDM allowed but bus operations would cause bus conflicts (must not be used)
1	1	1	0	0	Normal Expanded Wide, BDM allowed
			1	1	

For further explanation on the modes refer to the Core User Guide.

Table 4-2 Clock Selection Based on PE7

PE7 = $\overline{XCLKS}$	Description
1	Colpitts Oscillator selected
0	Pierce Oscillator/external clock selected

Section 6 HCS12 Core Block Description

Consult the HCS12 Core User Guide for information about the HCS12 core modules, i.e. central processing unit (CPU), interrupt module (INT), module mapping control module (MMC), multiplexed external bus interface (MEBI), breakpoint module (BKP) and background debug mode module (BDM).

6.1 Device-specific information

When the BDM section of S12 Core User Guide refers to *alternate clock* this is equivalent to *oscillator clock*.

Section 7 Clock and Reset Generator (CRG) Block Description

Consult the CRG Block User Guide for information about the Clock and Reset Generator module.

7.1 Device-specific information

7.1.1 $\overline{\text{XCLKS}}$

The $\overline{\text{XCLKS}}$ input signal is active low (see **2.3.12 PE7 / NOACC / XCLKS — Port E I/O Pin 7**).

Section 8 Enhanced Capture Timer (ECT) Block Description

Consult the ECT_16B8C Block User Guide for information about the Enhanced Capture Timer module.When the ECT_16B8C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 9 Analog to Digital Converter (ATD) Block Description

There are two Analog to Digital Converters (ATD1 and ATD0) implemented on the MC9S12DT128B. Consult the ATD_10B8C Block User Guide for information about each Analog to Digital Converter module. When the ATD_10B8C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 10 Inter-IC Bus (IIC) Block Description

Consult the IIC Block User Guide for information about the Inter-IC Bus module.

Section 11 Serial Communications Interface (SCI) Block Description

There are two Serial Communications Interfaces (SCI1 and SCI0) implemented on theMC9S12DT128B device. Consult the SCI Block User Guide for information about each Serial Communications Interface module.

Section 12 Serial Peripheral Interface (SPI) Block Description

There are two Serial Peripheral Interfaces (SPI1 and SPI0) implemented on MC9S12DT128B. Consult the SPI Block User Guide for information about each Serial Peripheral Interface module.

Section 13 J1850 (BDLC) Block Description

Consult the BDLC Block User Guide for information about the J1850 module.

Section 14 Byteflight (BF) Block Description

Consult the BF Block User Guide for information about the 10 Mbps Byteflight module.

Section 15 Pulse Width Modulator (PWM) Block Description

Consult the PWM_8B8C Block User Guide for information about the Pulse Width Modulator module. When the PWM_8B8C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 16 Flash EEPROM 128K Block Description

Consult the FTS128K Block User Guide for information about the flash module.

Section 17 EEPROM 2K Block Description

Consult the EETS2K Block User Guide for information about the EEPROM module.

Section 18 RAM Block Description

This module supports single-cycle misaligned word accesses without wait states.

Section 19 MSCAN Block Description

There are three MSCAN modules (CAN4, CAN1 and CAN0) implemented on the MC9S12DT128B. Consult the MSCAN Block User Guide for information about the Motorola Scalable CAN Module.

Section 20 Port Integration Module (PIM) Block Description

Consult the PIM_9DTB128 Block User Guide for information about the Port Integration Module.

Section 21 Voltage Regulator (VREG) Block Description

Consult the VREG Block User Guide for information about the dual output linear voltage regulator.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-2 ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ohm
	Storage Capacitance	C	100	pF
	Number of Pulse per pin positive negative	–	– 3 3	
Machine	Series Resistance	R1	0	Ohm
	Storage Capacitance	C	200	pF
	Number of Pulse per pin positive negative	–	– 3 3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table A-3 ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	C	Human Body Model (HBM)	V_{HBM}	2000	–	V
2	C	Machine Model (MM)	V_{MM}	200	–	V
3	C	Charge Device Model (CDM)	V_{CDM}	500	–	V
4	C	Latch-up Current at 125°C positive negative	I_{LAT}	 +100 –100	–	mA
5	C	Latch-up Current at 27°C positive negative	I_{LAT}	 +200 –200	–	mA

A.1.7 Operating Conditions

This chapter describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

NOTE: *Please refer to the temperature rating of the device (C, V, M) with regards to the ambient temperature T_A and the junction temperature T_J. For power dissipation*

A.3 NVM, Flash and EEPROM

NOTE: *Unless otherwise noted the abbreviation NVM (Non Volatile Memory) is used for both Flash and EEPROM.*

A.3.1 NVM timing

The time base for all NVM program or erase operations is derived from the oscillator. A minimum oscillator frequency f_{NVMOSC} is required for performing program or erase operations. The NVM modules do not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency a full program or erase transition is not assured.

The Flash and EEPROM program and erase operations are timed using a clock derived from the oscillator using the FCLKDIV and ECLKDIV registers respectively. The frequency of this clock must be set within the limits specified as f_{NVMOP}.

The minimum program and erase times shown in **Table A-11** are calculated for maximum f_{NVMOP} and maximum f_{bus}. The maximum times are calculated for minimum f_{NVMOP} and a f_{bus} of 2MHz.

A.3.1.1 Single Word Programming

The programming time for single word programming is dependant on the bus frequency as a well as on the frequency f_{NVMOP} and can be calculated according to the following formula.

$$t_{swpgm} = 9 \cdot \frac{1}{f_{NVMOP}} + 25 \cdot \frac{1}{f_{bus}}$$

A.3.1.2 Burst Programming

This applies only to the Flash where up to 32 words in a row can be programmed consecutively using burst programming by keeping the command pipeline filled. The time to program a consecutive word can be calculated as:

$$t_{bwpgm} = 4 \cdot \frac{1}{f_{NVMOP}} + 9 \cdot \frac{1}{f_{bus}}$$

The time to program a whole row is:

$$t_{brpgm} = t_{swpgm} + 31 \cdot t_{bwpgm}$$

Burst programming is more than 2 times faster than single word programming.

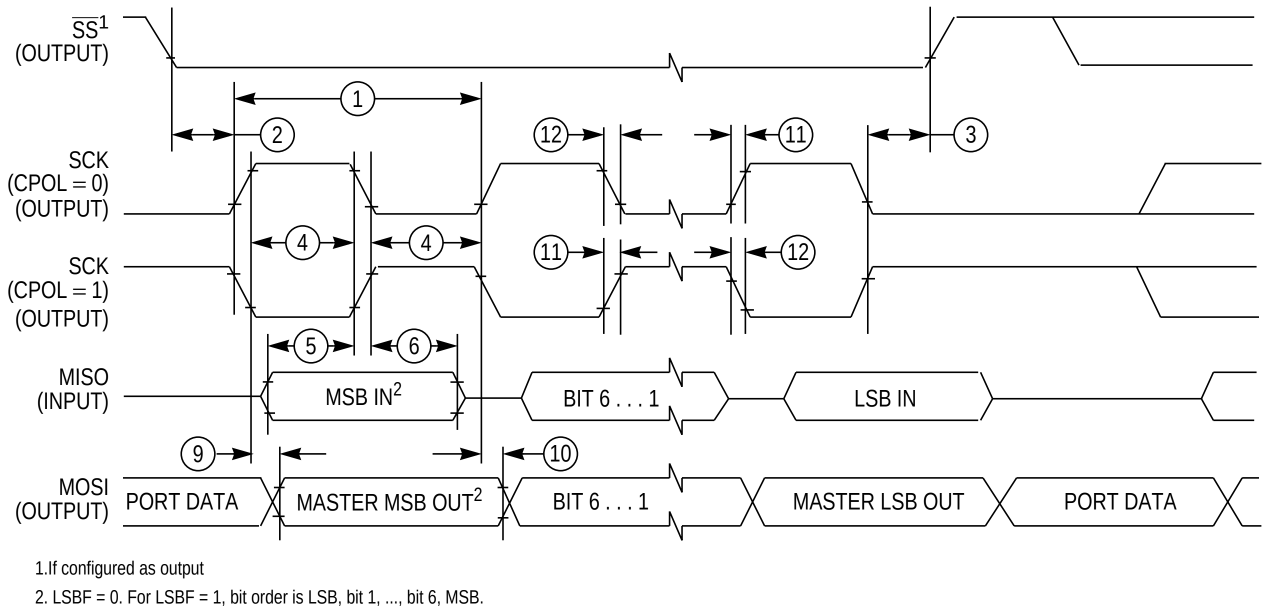


Figure A-6 SPI Master Timing (CPHA =1)

Table A-18 SPI Master Mode Timing Characteristics[1]

Conditions are shown in **Table A-4** unless otherwise noted, C_{LOAD} = 200pF on all outputs							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Operating Frequency	f_{op}	DC		1/4	f_{bus}
1	P	SCK Period t_{sck} = 1./f_{op}	t_{sck}	4		2048	t_{bus}
2	D	Enable Lead Time	t_{lead}	1/2		—	t_{sck}
3	D	Enable Lag Time	t_{lag}	1/2			t_{sck}
4	D	Clock (SCK) High or Low Time	t_{wsck}	t_{bus} – 30		1024 t_{bus}	ns
5	D	Data Setup Time (Inputs)	t_{su}	25			ns
6	D	Data Hold Time (Inputs)	t_{hi}	0			ns
9	D	Data Valid (after SCK Edge)	t_v			25	ns
10	D	Data Hold Time (Outputs)	t_{ho}	0			ns
11	D	Rise Time Inputs and Outputs	t_r			25	ns
12	D	Fall Time Inputs and Outputs	t_f			25	ns

NOTES:
1. The numbers 7, 8 in the column labeled "Num" are missing. This has been done on purpose to be consistent between the Master and the Slave timing shown in **Table A-19**.