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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I ² C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12dj128bcfu

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- Do not write or read BDLC registers (after reset: address range \$00E8 - \$00EF), if using a derivative without BDLC (see **Table 0-1**).
- Do not write or read IIC registers (after reset: address range \$00E0 - \$00E7), if using a derivative without IIC (see **Table 0-1**).
- Do not write or read Byteflight registers (after reset: address range \$0300 - \$035F), if using a derivative without Byteflight registers (see **Table 0-1**).
- **Interrupts**
 - Fill the four CAN1 interrupt vectors (\$FFA8 - \$FFAF) according to your coding policies for unused interrupts, if using a derivative without CAN1 (see **Table 0-1**).
 - Fill the BDLC interrupt vector (\$FFC2, \$FFC3) according to your coding policies for unused interrupts, if using a derivative without BDLC (see **Table 0-1**).
 - Fill the IIC interrupt vector (\$FFC0, \$FFC1) according to your coding policies for unused interrupts, if using a derivative without IIC (see **Table 0-1**).
 - Fill the four Byteflight interrupt vectors (\$FFA0 - \$FFA7) according to your coding policies for unused interrupts, if using a derivative without Byteflight (see **Table 0-1**).
- **Ports**
 - The CAN1 pin functionality (TXCAN1, RXCAN1) is not available on port PM3 and PM2, if using a derivative without CAN1 (see **Table 0-1**).
 - The BDLC pin functionality (TXB, RXB) is not available on port PM1 and PM0, if using a derivative without BDLC (see **Table 0-1**).
 - The IIC pin functionality (SCL, SCA) is not available on port PJ7 and PJ6, if using a derivative without IIC (see **Table 0-1**).
 - The Byteflight pin functionality (BF_PSLM, BF_PERR, BF_PROK, BF_PSYN, TX_BF, RX_BF) is not available on port PM7, PM6, PM5, PM4, PM3 and PM2, if using a derivative without Byteflight (see **Table 0-1**).
- **Pins not available in 80 pin QFP package**
 - **Port H**
In order to avoid floating nodes the ports should be either configured as outputs by setting the data direction register (DDRH at Base+\$0262) to \$FF, or enabling the pull resistors by writing a \$FF to the pull enable register (PERH at Base+\$0264).
 - **Port J[1:0]**
Port J pull-up resistors are enabled out of reset on all four pins (7:6 and 1:0). Therefore care must be taken not to disable the pull enables on PJ[1:0] by clearing the bits PERJ1 and PERJ0 at Base+\$026C.
 - **Port K**
Port K pull-up resistors are enabled out of reset, i.e. Bit 7 = PUKE = 1 in the register PUCR at Base+\$000C. Therefore care must be taken not to clear this bit.

\$0015 - \$0016**INT map 1 of 2 (Core User Guide)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0015	ITCR	Read:	0	0	0	WRINT	ADR3	ADR2	ADR1	ADR0
		Write:								
\$0016	ITEST	Read:	INTE	INTC	INTA	INT8	INT6	INT4	INT2	INT0
		Write:								

\$0017 - \$0017**MMC map 2 of 4 (Core User Guide)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0017	MTST1 Test Only	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

\$0018 - \$001B**Miscellaneous Peripherals (Device User Guide, Table 1-3)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0018	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0019	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$001A	PARTIDH	Read:	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
		Write:								
\$001B	PARTIDL	Read:	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		Write:								

\$001C - \$001D**MMC map 3 of 4 (Core and Device User Guide, Table 1-4)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$001C	MEMSIZ0	Read:	reg_sw0	0	eep_sw1	eep_sw0	0	ram_sw2	ram_sw1	ram_sw0
		Write:								
\$001D	MEMSIZ1	Read:	rom_sw1	rom_sw0	0	0	0	0	pag_sw1	pag_sw0
		Write:								

\$001E - \$001E**MEBI map 2 of 3 (Core User Guide)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$001E	INTCR	Read:	IRQE	IRQEN	0	0	0	0	0	0
		Write:								

\$001F - \$001F**INT map 2 of 2 (Core User Guide)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$001F	HPRIO	Read:	PSEL7	PSEL6	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0
		Write:								

\$0020 - \$0027**Reserved**

Address Name
 \$0020 - Reserved
 \$0027

Read:
 Write:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	0

\$0028 - \$002F**BKP (Core User Guide)**

Address Name
 \$0028 BKPCT0

Read:
 Write:

\$0029 BKPCT1

Read:
 Write:

\$002A BKP0X

Read:
 Write:

\$002B BKP0H

Read:
 Write:

\$002C BKP0L

Read:
 Write:

\$002D BKP1X

Read:
 Write:

\$002E BKP1H

Read:
 Write:

\$002F BKP1L

Read:
 Write:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BKEN	BKFULL	BKBDM	BKTAG	0	0	0	0
BK0MBH	BK0MBL	BK1MBH	BK1MBL	BK0RWE	BK0RW	BK1RWE	BK1RW
0	0	BK0V5	BK0V4	BK0V3	BK0V2	BK0V1	BK0V0
Bit 15	14	13	12	11	10	9	Bit 8
Bit 7	6	5	4	3	2	1	Bit 0
0	0	BK1V5	BK1V4	BK1V3	BK1V2	BK1V1	BK1V0
Bit 15	14	13	12	11	10	9	Bit 8
Bit 7	6	5	4	3	2	1	Bit 0

\$0030 - \$0031**MMC map 4 of 4 (Core User Guide)**

Address Name
 \$0030 PPAGE
 \$0031 Reserved

Read:
 Write:

Read:
 Write:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	PIX5	PIX4	PIX3	PIX2	PIX1	PIX0
0	0	0	0	0	0	0	0

\$0032 - \$0033**MEBI map 3 of 3 (Core User Guide)**

Address Name
 \$0032 PORTK
 \$0033 DDRK

Read:
 Write:

Read:
 Write:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0

\$0120 - \$013F

ATD1 (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0130	ATD1DR0H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$0131	ATD1DR0L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
\$0132	ATD1DR1H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$0133	ATD1DR1L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
\$0134	ATD1DR2H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$0135	ATD1DR2L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
\$0136	ATD1DR3H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$0137	ATD1DR3L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
\$0138	ATD1DR4H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$0139	ATD1DR4L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
\$013A	ATD1DR5H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$013B	ATD1DR5L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
\$013C	ATD1DR6H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$013D	ATD1DR6L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
\$013E	ATD1DR7H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$013F	ATD1DR7L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

\$0140 - \$017F

CAN0 (Motorola Scalable CAN - MSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0140	CAN0CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:								
\$0141	CAN0CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		Write:								
\$0142	CAN0BTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:								
\$0143	CAN0BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:								
\$0144	CAN0RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:								
\$0145	CAN0RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:								

Table 1-2 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$xxxC	CANRxDLR	Read:					DLC3	DLC2	DLC1	DLC0
		Write:								
\$xxxD	Reserved	Read:								
		Write:								
\$xxxE	CANxRTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
\$xxxF	CANxRTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								
\$xx10	Extended ID CANxTIDR0	Read:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
		Write:								
	Standard ID	Read:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
		Write:								
\$xx11	Extended ID CANxTIDR1	Read:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
		Write:								
	Standard ID	Read:	ID2	ID1	ID0	RTR	IDE=0			
		Write:								
\$xx12	Extended ID CANxTIDR2	Read:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
		Write:								
	Standard ID	Read:								
		Write:								
\$xx13	Extended ID CANxTIDR3	Read:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
		Write:								
	Standard ID	Read:								
		Write:								
\$xx14- \$xx1B	CANxTDSR0 - CANxTDSR7	Read:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Write:								
\$xx1C	CANxTDLR	Read:					DLC3	DLC2	DLC1	DLC0
		Write:								
\$xx1D	CONxTTBPR	Read:	PRI07	PRI06	PRI05	PRI04	PRI03	PRI02	PRI01	PRI00
		Write:								
\$xx1E	CANxTTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
\$xx1F	CANxTTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								

\$0180 - \$01BF

CAN1 (Motorola Scalable CAN - MSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0180	CAN1CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:								
\$0181	CAN1CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		Write:								
\$0182	CAN1BTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:								
\$0183	CAN1BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:								
\$0184	CAN1RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIIF	RXF
		Write:								

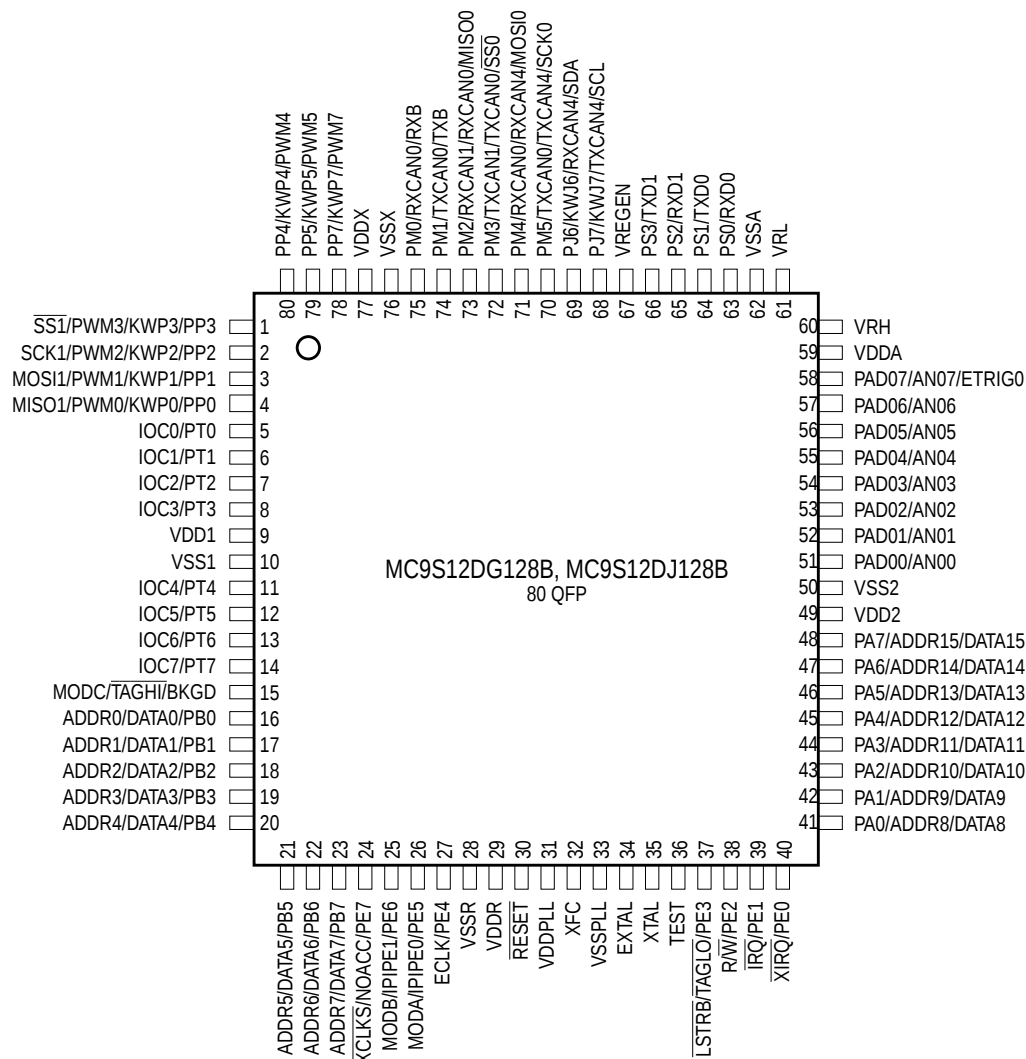


Figure 2-2 Pin Assignments in 80 QFP for MC9S12DG128B, MC9S12DJ128B Bondout

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Pin Name Function 5	Powered by	Internal Pull Resistor		Description
						CTRL	Reset State	
PE1	$\overline{\text{IRQ}}$	—	—	—	VDDR	Always Up	Up	Port E Input, Maskable Interrupt
PE0	$\overline{\text{XIRQ}}$	—	—	—	VDDR	Always Up	Up	Port E Input, Non Maskable Interrupt
PH7	KWH7	---	—	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt
PH6	KWH6	---	—	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt
PH5	KWH5	---	—	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt
PH4	KWH4	---	—	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt
PH3	KWH3	$\overline{\text{SS1}}$	—	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, $\overline{\text{SS}}$ of SPI1
PH2	KWH2	SCK1	—	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, SCK of SPI1
PH1	KWH1	MOSI1	—	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, MOSI of SPI1
PH0	KWH0	MISO1	—	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, MISO of SPI1
PJ7	KWJ7	TXCAN4	SCL	—	VDDX	PERJ/ PPSJ	Up	Port J I/O, Interrupt, TX of CAN4, SCL of IIC
PJ6	KWJ6	RXCAN4	SDA	—	VDDX	PERJ/ PPSJ	Up	Port J I/O, Interrupt, RX of CAN4, SDA of IIC
PJ[1:0]	KWJ[1:0]	—	—	—	VDDX	PERJ/ PPSJ	Up	Port J I/O, Interrupts
PK7	$\overline{\text{ECS}}$	ROMCTL	—	—	VDDX	PUCR/ PUPKE	Up	Port K I/O, Emulation Chip Select, ROM Control
PK[5:0]	XADDR[19: 14]	—	—	—	VDDX	PUCR/ PUPKE	Up	Port K I/O, Extended Addresses
PM7	BF_PSLM	TXCAN4	—	—	VDDX	PERM/ PPSM	Disabled	Port M I/O, BF slot mismatch pulse, TX of CAN4
PM6	BF_PERR	RXCAN4	—	—	VDDX	PERM/ PPSM	Disabled	Port M I/O, BF illegal pulse/message format error pulse, RX of CAN4
PM5	BF_PROK	TXCAN0	TXCAN4	SCK0	VDDX	PERM/ PPSM	Disabled	Port M I/O, BF reception ok pulse, TX of CAN0, CAN4, SCK of SPI0
PM4	BF_PSYN	RXCAN0	RXCAN4	MOSI0	VDDX	PERM/ PPSM	Disabled	Port M I/O, BF sync pulse (Rx/Tx) OK pulse o/p, RX of CAN0, CAN4, MOSI of SPI0

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Pin Name Function 5	Powered by	Internal Pull Resistor		Description
						CTRL	Reset State	
PM3	TX_BF	TXCAN1	TXCAN0	$\overline{SS}0$	VDDX	PERM/ PPSM	Disabled	Port M I/O, TX of BF, CAN1, CAN0, $\overline{SS}$ of SPI0
PM2	RX_BF	RXCAN1	RXCAN0	MISO0	VDDX	PERM/ PPSM	Disabled	Port M I/O, RX of BF, CAN1, CAN0, MISO of SPI0
PM1	TXCAN0	TXB	—	—	VDDX	PERM/ PPSM	Disabled	Port M I/O, TX of CAN0, RX of BDLC
PM0	RXCAN0	RXB	—	—	VDDX	PERM/ PPSM	Disabled	Port M I/O, RX of CAN0, RX of BDLC
PP7	KWP7	PWM7	—	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 7 of PWM
PP6	KWP6	PWM6	—	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 6 of PWM
PP5	KWP5	PWM5	—	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 5 of PWM
PP4	KWP4	PWM4	—	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 4 of PWM
PP3	KWP3	PWM3	$\overline{SS}1$	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 3 of PWM, $\overline{SS}$ of SPI1
PP2	KWP2	PWM2	SCK1	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 2 of PWM, SCK of SPI1
PP1	KWP1	PWM1	MOSI1	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 1 of PWM, MOSI of SPI1
PP0	KWP0	PWM0	MISO1	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 0 of PWM, MISO2 of SPI1
PS7	$\overline{SS}0$	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, $\overline{SS}$ of SPI0
PS6	SCK0	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, SCK of SPI0
PS5	MOSI0	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, MOSI of SPI0
PS4	MISO0	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, MISO of SPI0
PS3	TXD1	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, TXD of SCI1
PS2	RXD1	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, RXD of SCI1
PS1	TXD0	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, TXD of SCI0
PS0	RXD0	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, RXD of SCI0
PT[7:0]	IOC[7:0]	—	—	—	VDDX	PERT/ PPST	Disabled	Port T I/O, Timer channels

Mnemonic	Pin Number	Nominal Voltage	Description
	112-pin QFP		
VDDR	41	5.0V	External power and ground, supply to pin drivers and internal voltage regulator.
VSSR	40	0V	
VDDX	107	5.0V	External power and ground, supply to pin drivers.
VSSX	106	0V	
VDDA	83	5.0V	Operating voltage and ground for the analog-to-digital converters and the reference for the internal voltage regulator, allows the supply voltage to the A/D to be bypassed independently.
VSSA	86	0V	
VRL	85	0V	Reference voltages for the analog-to-digital converter.
VRH	84	5.0V	
VDDPLL	43	2.5V	Provides operating voltage and ground for the Phased-Locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator.
VSSPLL	45	0V	
VREGEN	97	5V	Internal Voltage Regulator enable/disable

NOTE: All VSS pins must be connected together in the application.

2.4.1 VDDX,VSSX — Power & Ground Pins for I/O Drivers

External power and ground for I/O drivers. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.2 VDDR, VSSR — Power & Ground Pins for I/O Drivers & for Internal Voltage Regulator

External power and ground for I/O drivers and input to the internal voltage regulator. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.3 VDD1, VDD2, VSS1, VSS2 — Core Power Pins

Power is supplied to the MCU through VDD and VSS. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VREGEN is tied to ground.

NOTE: No load allowed except for bypass capacitors.

Consult the IIC Block User Guide for information about the Inter-IC Bus module.

Section 11 Serial Communications Interface (SCI) Block Description

There are two Serial Communications Interfaces (SCI1 and SCI0) implemented on the MC9S12DT128B device. Consult the SCI Block User Guide for information about each Serial Communications Interface module.

Section 12 Serial Peripheral Interface (SPI) Block Description

There are two Serial Peripheral Interfaces (SPI1 and SPI0) implemented on MC9S12DT128B. Consult the SPI Block User Guide for information about each Serial Peripheral Interface module.

Section 13 J1850 (BDLC) Block Description

Consult the BDLC Block User Guide for information about the J1850 module.

Section 14 Byteflight (BF) Block Description

Consult the BF Block User Guide for information about the 10 Mbps Byteflight module.

Section 15 Pulse Width Modulator (PWM) Block Description

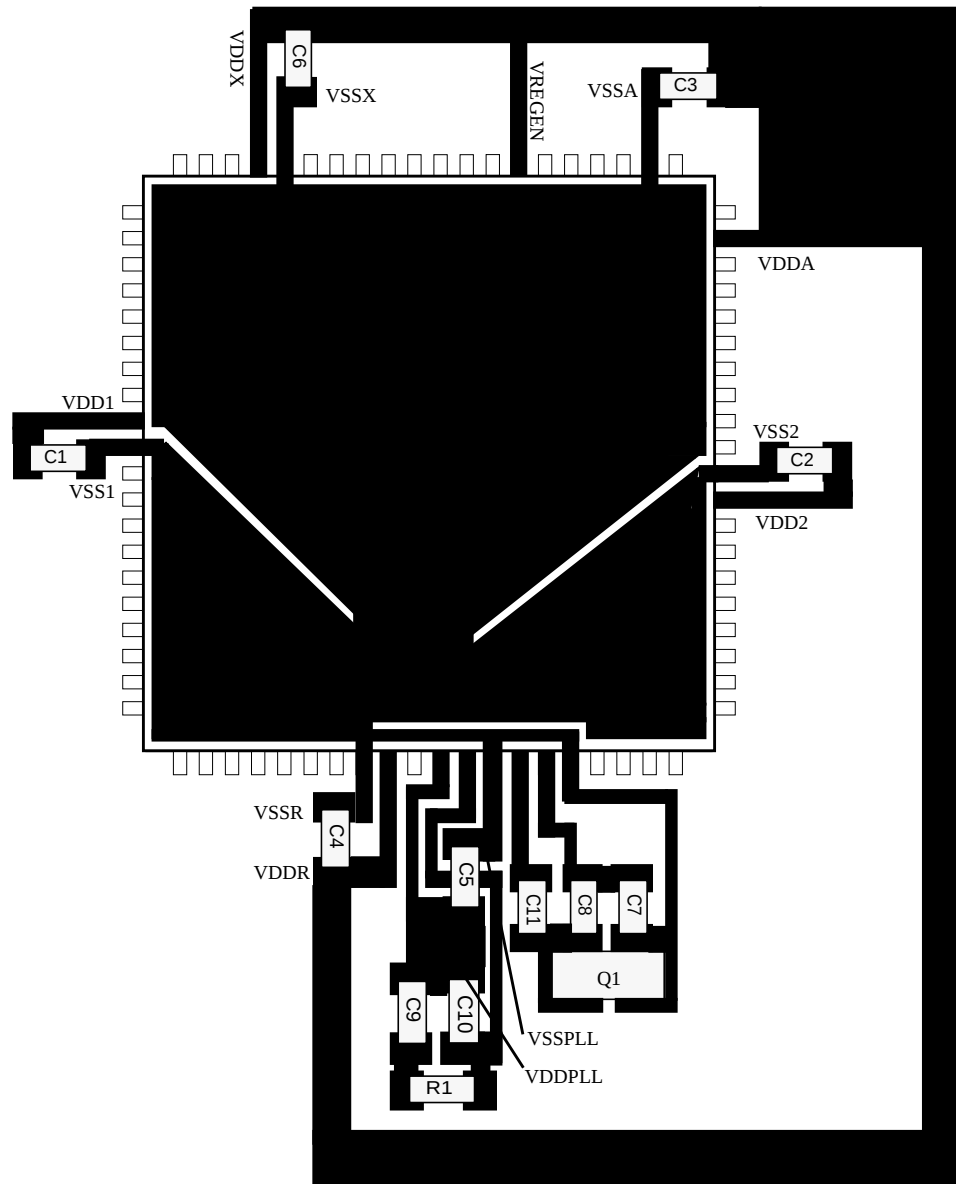
Consult the PWM_8B8C Block User Guide for information about the Pulse Width Modulator module. When the PWM_8B8C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 16 Flash EEPROM 128K Block Description

Consult the FTS128K Block User Guide for information about the flash module.

Section 17 EEPROM 2K Block Description

Figure 22-2 Recommended PCB Layout for 80QFP Colpitts Oscillator



A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-2 ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ohm
	Storage Capacitance	C	100	pF
	Number of Pulse per pin positive negative	— 3 3	— 3 3	
Machine	Series Resistance	R1	0	Ohm
	Storage Capacitance	C	200	pF
	Number of Pulse per pin positive negative	— 3 3	— 3 3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table A-3 ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	C	Human Body Model (HBM)	V_{HBM}	2000	—	V
2	C	Machine Model (MM)	V_{MM}	200	—	V
3	C	Charge Device Model (CDM)	V_{CDM}	500	—	V
4	C	Latch-up Current at 125°C positive negative	I_{LAT}	+100 –100	—	mA
5	C	Latch-up Current at 27°C positive negative	I_{LAT}	+200 –200	—	mA

A.1.7 Operating Conditions

This chapter describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

NOTE: Please refer to the temperature rating of the device (C, V, M) with regards to the ambient temperature T_A and the junction temperature T_J . For power dissipation

given. A very good estimate is to take the single chip currents and add the currents due to the external loads.

Table A-7 Supply Current Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Run supply currents Single Chip, Internal regulator enabled	I_{DD5}			55	mA
2	P P	Wait Supply current All modules enabled, PLL on only RTI enabled ¹	I_{DDW}			30 5	mA
3	C P C C P C P C P	Pseudo Stop Current (RTI and COP disabled) ^{1, 2} -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C	I_{DDPS}		370 400 450 550 600 650 800 850 1200	500 1600 2100 5000	μA
4	C C C C C C C C	Pseudo Stop Current (RTI and COP enabled) ^{1, 2} -40°C 27°C 70°C 85°C 105°C 125°C 140°C	I_{DDPS}		570 600 650 750 850 1200 1500		μA
5	C P C C P C P C P	Stop Current ² -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C	I_{DDS}		12 25 100 130 160 200 350 400 600	100 1200 1700 5000	μA

NOTES:

1. PLL off, Oscillator in Colpitts Mode

2. At those low power dissipation levels $T_J = T_A$ can be assumed

A.3 NVM, Flash and EEPROM

NOTE: Unless otherwise noted the abbreviation NVM (Non Volatile Memory) is used for both Flash and EEPROM.

A.3.1 NVM timing

The time base for all NVM program or erase operations is derived from the oscillator. A minimum oscillator frequency f_{NVMOSC} is required for performing program or erase operations. The NVM modules do not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency a full program or erase transition is not assured.

The Flash and EEPROM program and erase operations are timed using a clock derived from the oscillator using the FCLKDIV and ECLKDIV registers respectively. The frequency of this clock must be set within the limits specified as f_{NVMOP} .

The minimum program and erase times shown in **Table A-11** are calculated for maximum f_{NVMOP} and maximum f_{bus} . The maximum times are calculated for minimum f_{NVMOP} and a f_{bus} of 2MHz.

A.3.1.1 Single Word Programming

The programming time for single word programming is dependant on the bus frequency as a well as on the frequency f_{NVMOP} and can be calculated according to the following formula.

$$t_{\text{swpgm}} = 9 \cdot \frac{1}{f_{\text{NVMOP}}} + 25 \cdot \frac{1}{f_{\text{bus}}}$$

A.3.1.2 Burst Programming

This applies only to the Flash where up to 32 words in a row can be programmed consecutively using burst programming by keeping the command pipeline filled. The time to program a consecutive word can be calculated as:

$$t_{\text{bwpgm}} = 4 \cdot \frac{1}{f_{\text{NVMOP}}} + 9 \cdot \frac{1}{f_{\text{bus}}}$$

The time to program a whole row is:

$$t_{\text{brpgm}} = t_{\text{swpgm}} + 31 \cdot t_{\text{bwpgm}}$$

Burst programming is more than 2 times faster than single word programming.

A.5 Reset, Oscillator and PLL

This section summarizes the electrical characteristics of the various startup scenarios for Oscillator and Phase-Locked-Loop (PLL).

A.5.1 Startup

Table A-14 summarizes several startup characteristics explained in this section. Detailed description of the startup behavior can be found in the Clock and Reset Generator (CRG) Block User Guide.

Table A-14 Startup Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	POR release level	V_{PORR}			2.07	V
2	T	POR assert level	V_{PORA}	0.97			V
3	D	Reset input pulse width, minimum input time	PW_{RSTL}	2			t_{osc}
4	D	Startup from Reset	n_{RST}	192		196	n_{osc}
5	D	Interrupt pulse width, $\overline{IRQ}$ edge-sensitive mode	PW_{IRQ}	20			ns
6	D	Wait recovery startup time	t_{WRS}			14	t_{cyc}

A.5.1.1 POR

The release level V_{PORR} and the assert level V_{PORA} are derived from the V_{DD} Supply. They are also valid if the device is powered externally. After releasing the POR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc} .

A.5.1.2 SRAM Data Retention

Provided an appropriate external reset signal is applied to the MCU, preventing the CPU from executing code when VDD5 is out of specification limits, the SRAM contents integrity is guaranteed if after the reset the PORF bit in the CRG Flags Register has not been set.

A.5.1.3 External Reset

When external reset is asserted for a time greater than PW_{RSTL} the CRG module generates an internal reset, and the CPU starts fetching the reset vector without doing a clock quality check, if there was an oscillation before reset.

A.5.1.4 Stop Recovery

Out of STOP the controller can be woken up by an external interrupt. A clock quality check as after POR is performed before releasing the clocks to the system.

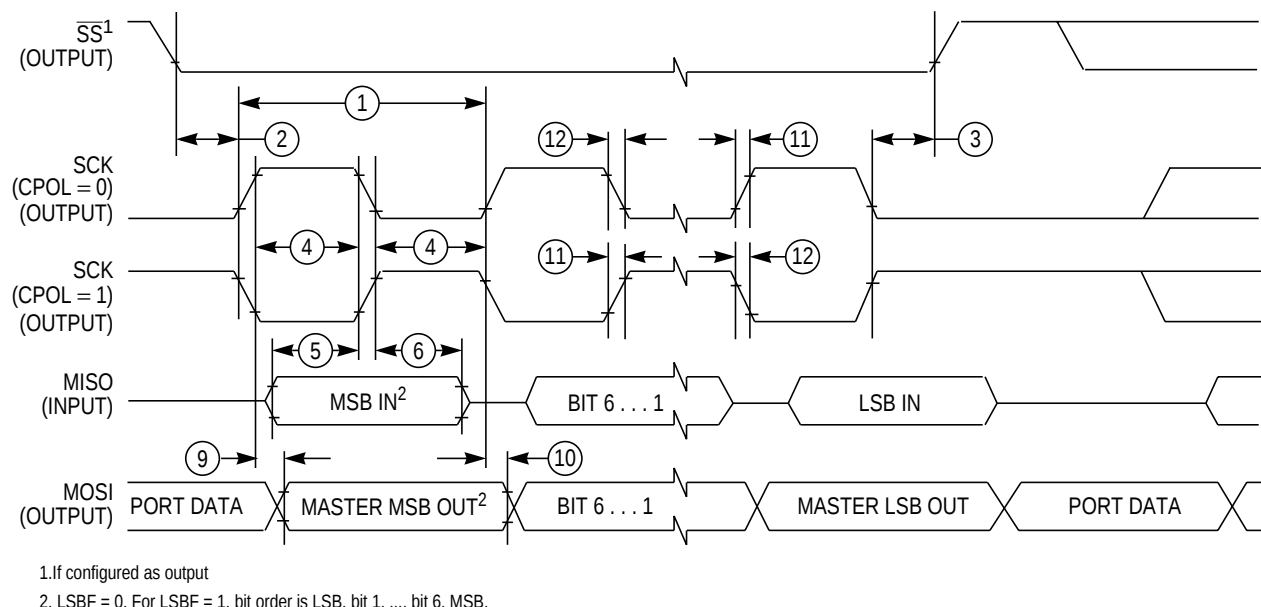


Figure A-6 SPI Master Timing (CPHA =1)

Table A-18 SPI Master Mode Timing Characteristics¹

Conditions are shown in Table A-4 unless otherwise noted, $C_{LOAD} = 200pF$ on all outputs							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Operating Frequency	f_{op}	DC		1/4	f_{bus}
1	P	SCK Period $t_{sck} = 1./f_{op}$	t_{sck}	4		2048	t_{bus}
2	D	Enable Lead Time	t_{lead}	1/2		—	t_{sck}
3	D	Enable Lag Time	t_{lag}	1/2			t_{sck}
4	D	Clock (SCK) High or Low Time	t_{wsck}	$t_{bus} - 30$		$1024 t_{bus}$	ns
5	D	Data Setup Time (Inputs)	t_{su}	25			ns
6	D	Data Hold Time (Inputs)	t_{hi}	0			ns
9	D	Data Valid (after SCK Edge)	t_v			25	ns
10	D	Data Hold Time (Outputs)	t_{ho}	0			ns
11	D	Rise Time Inputs and Outputs	t_r			25	ns
12	D	Fall Time Inputs and Outputs	t_f			25	ns

NOTES:

- The numbers 7, 8 in the column labeled "Num" are missing. This has been done on purpose to be consistent between the Master and the Slave timing shown in **Table A-19**.

Table A-20 Expanded Bus Timing Characteristics

Conditions are shown in Table A-4 unless otherwise noted, C _{LOAD} = 50pF							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Frequency of operation (E-clock)	f _o	0		25.0	MHz
2	P	Cycle time	t _{cyc}	40			ns
3	D	Pulse width, E low	PW _{EL}	19			ns
4	D	Pulse width, E high ¹	PW _{EH}	19			ns
5	D	Address delay time	t _{AD}			8	ns
6	D	Address valid time to E rise (PW _{EL} –t _{AD})	t _{AV}	11			ns
7	D	Muxed address hold time	t _{MAH}	2			ns
8	D	Address hold to data valid	t _{AHDS}	7			ns
9	D	Data hold to address	t _{DHA}	2			ns
10	D	Read data setup time	t _{DSR}	13			ns
11	D	Read data hold time	t _{DHR}	0			ns
12	D	Write data delay time	t _{DDW}			7	ns
13	D	Write data hold time	t _{DHW}	2			ns
14	D	Write data setup time ⁽¹⁾ (PW _{EH} –t _{DDW})	t _{DSW}	12			ns
15	D	Address access time ⁽¹⁾ (t _{cyc} –t _{AD} –t _{DSR})	t _{ACCA}	19			ns
16	D	E high access time ⁽¹⁾ (PW _{EH} –t _{DSR})	t _{ACCE}	6			ns
17	D	Non-multiplexed address delay time	t _{NAD}			6	ns
18	D	Non-muxed address valid to E rise (PW _{EL} –t _{NAD})	t _{NAV}	15			ns
19	D	Non-multiplexed address hold time	t _{NAH}	2			ns
20	D	Chip select delay time	t _{CSD}			16	ns
21	D	Chip select access time ⁽¹⁾ (t _{cyc} –t _{CSD} –t _{DSR})	t _{ACCS}	11			ns
22	D	Chip select hold time	t _{CSH}	2			ns
23	D	Chip select negated time	t _{CSN}	8			ns
24	D	Read/write delay time	t _{RWD}			7	ns
25	D	Read/write valid time to E rise (PW _{EL} –t _{RWD})	t _{RWV}	14			ns
26	D	Read/write hold time	t _{RWH}	2			ns
27	D	Low strobe delay time	t _{LSD}			7	ns
28	D	Low strobe valid time to E rise (PW _{EL} –t _{LSD})	t _{LSV}	14			ns
29	D	Low strobe hold time	t _{LSH}	2			ns
30	D	NOACC strobe delay time	t _{NOD}			7	ns
31	D	NOACC valid time to E rise (PW _{EL} –t _{NOD})	t _{NOV}	14			ns