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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | HCS12 |
| Core Size | 16-Bit |
| Speed | 25MHz |
| Connectivity | CANbus, I²C, SCI, SPI |
| Peripherals | PWM, WDT |
| Number of I/O | 91 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.35V ~ 5.25V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 112-LQFP |
| Supplier Device Package | 112-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12dt128cpv |

# Section 1 Introduction

## 1.1 Overview

The MC9S12DT128B microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), 128K bytes of Flash EEPROM, 8K bytes of RAM, 2K bytes of EEPROM, two asynchronous serial communications interfaces (SCI), two serial peripheral interfaces (SPI), an 8-channel IC/OC enhanced capture timer, two 8-channel, 10-bit analog-to-digital converters (ADC), an 8-channel pulse-width modulator (PWM), a digital Byte Data Link Controller (BDLC), 29 discrete digital I/O channels (Port A, Port B, Port K and Port E), 20 discrete digital I/O lines with interrupt and wakeup capability, three CAN 2.0 A, B software compatible modules (MSCAN12), a Byteflight module and an Inter-IC Bus. The MC9S12DT128B has full 16-bit data paths throughout. However, the external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements.

## 1.2 Features

- HCS12 Core
  - 16-bit HCS12 CPU
    i. Upward compatible with M68HC11 instruction set
    ii. Interrupt stacking and programmer’s model identical to M68HC11
    iii. 20-bit ALU
    iv. Instruction queue
    v. Enhanced indexed addressing
  - MEBI (Multiplexed External Bus Interface)
  - MMC (Module Mapping Control)
  - INT (Interrupt control)
  - BKP (Breakpoints)
  - BDM (Background Debug Mode)
- CRG (Clock and Reset Generator)
  - Choice of low current Colpitts oscillator or standard Pierce Oscillator
  - PLL
  - COP watchdog
  - real time interrupt
  - clock monitor
- 8-bit and 4-bit ports with interrupt functionality

## $00E8 - $00EF BDLC (Byte Level Data Link Controller J1850)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $00E8 | DLCBCR1 | Read: | IMSG | CLKS | 0 | 0 | 0 | 0 | IE | WCM |
| | | Write: | | | | | | | | |
| $00E9 | DLCBSVR | Read: | 0 | 0 | I3 | I2 | I1 | I0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $00EA | DLCBCR2 | Read: | SMRST | DLOOP | RX4XE | NBFS | TEOD | TSIFR | TMIFR1 | TMIFR0 |
| | | Write: | | | | | | | | |
| $00EB | DLCBDR | Read: | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | Write: | | | | | | | | |
| $00EC | DLCBARD | Read: | 0 | RXPOL | 0 | 0 | BO3 | BO2 | BO1 | BO0 |
| | | Write: | | | | | | | | |
| $00ED | DLCBRSR | Read: | 0 | 0 | R5 | R4 | R3 | R2 | R1 | R0 |
| | | Write: | | | | | | | | |
| $00EE | DLCSCR | Read: | 0 | 0 | 0 | BDLCE | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $00EF | DLCBSTAT | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IDLE |
| | | Write: | | | | | | | | |

## $00F0 - $00F7 SPI1 (Serial Peripheral Interface)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $00F0 | SPI1CR1 | Read: | SPIE | SPE | SPTIE | MSTR | CPOL | CPHA | SSOE | LSBFE |
| | | Write: | | | | | | | | |
| $00F1 | SPI1CR2 | Read: | 0 | 0 | 0 | MODFEN | BIDIROE | 0 | SPISWAI | SPC0 |
| | | Write: | | | | | | | | |
| $00F2 | SPI1BR | Read: | 0 | SPPR2 | SPPR1 | SPPR0 | 0 | SPR2 | SPR1 | SPR0 |
| | | Write: | | | | | | | | |
| $00F3 | SPI1SR | Read: | SPIF | 0 | SPTEF | MODF | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $00F4 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $00F5 | SPI1DR | Read: | Bit7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit0 |
| | | Write: | | | | | | | | |
| $00F6 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $00F7 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

## $00F8 - $00FF Reserved

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $00F8 - $00FF | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

## $0110 - $011B EEPROM Control Register (eets2k)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $0119 | EADDRLO | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| $011A | EDATAHI | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| $011B | EDATALO | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |

## $011C - $011F Reserved for RAM Control Register

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $011C - $011F | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

## $0120 - $013F ATD1 (Analog to Digital Converter 10 Bit 8 Channel)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $0120 | ATD1CTL0 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $0121 | ATD1CTL1 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $0122 | ATD1CTL2 | Read: | ADPU | AFFC | AWAI | ETRIGLE | ETRIGP | ETRIG | ASCIE | ASCIF |
| | | Write: | | | | | | | | |
| $0123 | ATD1CTL3 | Read: | 0 | S8C | S4C | S2C | S1C | FIFO | FRZ1 | FRZ0 |
| | | Write: | | | | | | | | |
| $0124 | ATD1CTL4 | Read: | SRES8 | SMP1 | SMP0 | PRS4 | PRS3 | PRS2 | PRS1 | PRS0 |
| | | Write: | | | | | | | | |
| $0125 | ATD1CTL5 | Read: | DJM | DSGN | SCAN | MULT | 0 | CC | CB | CA |
| | | Write: | | | | | | | | |
| $0126 | ATD1STAT0 | Read: | SCF | 0 | ETORF | FIFOR | 0 | CC2 | CC1 | CC0 |
| | | Write: | | | | | | | | |
| $0127 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $0128 | ATD1TEST0 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $0129 | ATD1TEST1 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SC |
| | | Write: | | | | | | | | |
| $012A | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $012B | ATD1STAT1 | Read: | CCF7 | CCF6 | CCF5 | CCF4 | CCF3 | CCF2 | CCF1 | CCF0 |
| | | Write: | | | | | | | | |
| $012C | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $012D | ATD1DIEN | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| $012E | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $012F | PORTAD1 | Read: | Bit7 | 6 | 5 | 4 | 3 | 2 | 1 | BIT 0 |
| | | Write: | | | | | | | | |

## $0180 - $01BF CAN1 (Motorola Scalable CAN - MSCAN)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $0185 | CAN1RIER | Read: | WUPIE | CSCIE | RSTATE1 | RSTATE0 | TSTATE1 | TSTATE0 | OVRIE | RXFIE |
| | | Write: | | | | | | | | |
| $0186 | CAN1TFLG | Read: | 0 | 0 | 0 | 0 | 0 | TXE2 | TXE1 | TXE0 |
| | | Write: | | | | | | | | |
| $0187 | CAN1TIER | Read: | 0 | 0 | 0 | 0 | 0 | TXEIE2 | TXEIE1 | TXEIE0 |
| | | Write: | | | | | | | | |
| $0188 | CAN1TARQ | Read: | 0 | 0 | 0 | 0 | 0 | ABTRQ2 | ABTRQ1 | ABTRQ0 |
| | | Write: | | | | | | | | |
| $0189 | CAN1TAAK | Read: | 0 | 0 | 0 | 0 | 0 | ABTAK2 | ABTAK1 | ABTAK0 |
| | | Write: | | | | | | | | |
| $018A | CAN1TBSEL | Read: | 0 | 0 | 0 | 0 | 0 | TX2 | TX1 | TX0 |
| | | Write: | | | | | | | | |
| $018B | CAN1IDAC | Read: | 0 | 0 | IDAM1 | IDAM0 | 0 | IDHIT2 | IDHIT1 | IDHIT0 |
| | | Write: | | | | | | | | |
| $018C | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $018D | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $018E | CAN1RXERR | Read: | RXERR7 | RXERR6 | RXERR5 | RXERR4 | RXERR3 | RXERR2 | RXERR1 | RXERR0 |
| | | Write: | | | | | | | | |
| $018F | CAN1TXERR | Read: | TXERR7 | TXERR6 | TXERR5 | TXERR4 | TXERR3 | TXERR2 | TXERR1 | TXERR0 |
| | | Write: | | | | | | | | |
| $0190 - $0193 | CAN1IDAR0 - CAN1IDAR3 | Read: | AC7 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |
| | | Write: | | | | | | | | |
| $0194 - $0197 | CAN1IDMR0 - CAN1IDMR3 | Read: | AM7 | AM6 | AM5 | AM4 | AM3 | AM2 | AM1 | AM0 |
| | | Write: | | | | | | | | |
| $0198 - $019B | CAN1IDAR4 - CAN1IDAR7 | Read: | AC7 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |
| | | Write: | | | | | | | | |
| $019C - $019F | CAN1IDMR4 - CAN1IDMR7 | Read: | AM7 | AM6 | AM5 | AM4 | AM3 | AM2 | AM1 | AM0 |
| | | Write: | | | | | | | | |
| $01A0 - $01AF | CAN0RXFG | Read: | FOREGROUND RECEIVE BUFFER see **Table 1-2** | | | | | | | |
| | | Write: | | | | | | | | |
| $01B0 - $01BF | CAN0TXFG | Read: | FOREGROUND TRANSMIT BUFFER see **Table 1-2** | | | | | | | |
| | | Write: | | | | | | | | |

## $01C0 - $01FF Reserved

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $01C0 - $01FF | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

## $0200 - $023F Reserved

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $020C - $023F | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

## $0240 - $027F PIM (Port Integration Module)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $0259 | PTIP | Read: | PTIP7 | PTIP6 | PTIP5 | PTIP4 | PTIP3 | PTIP2 | PTIP1 | PTIP0 |
| | | Write: | | | | | | | | |
| $025A | DDRP | Read: | DDRP7 | DDRP7 | DDRP5 | DDRP4 | DDRP3 | DDRP2 | DDRP1 | DDRP0 |
| | | Write: | | | | | | | | |
| $025B | RDRP | Read: | RDRP7 | RDRP6 | RDRP5 | RDRP4 | RDRP3 | RDRP2 | RDRP1 | RDRP0 |
| | | Write: | | | | | | | | |
| $025C | PERP | Read: | PERP7 | PERP6 | PERP5 | PERP4 | PERP3 | PERP2 | PERP1 | PERP0 |
| | | Write: | | | | | | | | |
| $025D | PPSP | Read: | PPSP7 | PPSP6 | PPSP5 | PPSP4 | PPSP3 | PPSP2 | PPSP1 | PPSS0 |
| | | Write: | | | | | | | | |
| $025E | PIEP | Read: | PIEP7 | PIEP6 | PIEP5 | PIEP4 | PIEP3 | PIEP2 | PIEP1 | PIEP0 |
| | | Write: | | | | | | | | |
| $025F | PIFP | Read: | PIFP7 | PIFP6 | PIFP5 | PIFP4 | PIFP3 | PIFP2 | PIFP1 | PIFP0 |
| | | Write: | | | | | | | | |
| $0260 | PTH | Read: | PTH7 | PTH6 | PTH5 | PTH4 | PTH3 | PTH2 | PTH1 | PTH0 |
| | | Write: | | | | | | | | |
| $0261 | PTIH | Read: | PTIH7 | PTIH6 | PTIH5 | PTIH4 | PTIH3 | PTIH2 | PTIH1 | PTIH0 |
| | | Write: | | | | | | | | |
| $0262 | DDRH | Read: | DDRH7 | DDRH7 | DDRH5 | DDRH4 | DDRH3 | DDRH2 | DDRH1 | DDRH0 |
| | | Write: | | | | | | | | |
| $0263 | RDRH | Read: | RDRH7 | RDRH6 | RDRH5 | RDRH4 | RDRH3 | RDRH2 | RDRH1 | RDRH0 |
| | | Write: | | | | | | | | |
| $0264 | PERH | Read: | PERH7 | PERH6 | PERH5 | PERH4 | PERH3 | PERH2 | PERH1 | PERH0 |
| | | Write: | | | | | | | | |
| $0265 | PPSH | Read: | PPSH7 | PPSH6 | PPSH5 | PPSH4 | PPSH3 | PPSH2 | PPSH1 | PPSH0 |
| | | Write: | | | | | | | | |
| $0266 | PIEH | Read: | PIEH7 | PIEH6 | PIEH5 | PIEH4 | PIEH3 | PIEH2 | PIEH1 | PIEH0 |
| | | Write: | | | | | | | | |
| $0267 | PIFH | Read: | PIFH7 | PIFH6 | PIFH5 | PIFH4 | PIFH3 | PIFH2 | PIFH1 | PIFH0 |
| | | Write: | | | | | | | | |
| $0268 | PTJ | Read: | PTJ7 | PTJ6 | 0 | 0 | 0 | 0 | PTJ1 | PTJ0 |
| | | Write: | | | | | | | | |
| $0269 | PTIJ | Read: | PTIJ7 | PTIJ6 | 0 | 0 | 0 | 0 | PTIJ1 | PTIJ0 |
| | | Write: | | | | | | | | |
| $026A | DDRJ | Read: | DDRJ7 | DDRJ7 | 0 | 0 | 0 | 0 | DDRJ1 | DDRJ0 |
| | | Write: | | | | | | | | |
| $026B | RDRJ | Read: | RDRJ7 | RDRJ6 | 0 | 0 | 0 | 0 | RDRJ1 | RDRJ0 |
| | | Write: | | | | | | | | |
| $026C | PERJ | Read: | PERJ7 | PERJ6 | 0 | 0 | 0 | 0 | PERJ1 | PERJ0 |
| | | Write: | | | | | | | | |
| $026D | PPSJ | Read: | PPSJ7 | PPSJ6 | 0 | 0 | 0 | 0 | PPSJ1 | PPSJ0 |
| | | Write: | | | | | | | | |
| $026E | PIEJ | Read: | PIEJ7 | PIEJ6 | 0 | 0 | 0 | 0 | PIEJ1 | PIEJ0 |
| | | Write: | | | | | | | | |
| $026F | PIFJ | Read: | PIFJ7 | PIFJ6 | 0 | 0 | 0 | 0 | PIFJ1 | PIFJ0 |
| | | Write: | | | | | | | | |
| $0270 - $027F | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

## $0280 - $02BF CAN4 (Motorola Scalable CAN - MSCAN)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $0280 | CAN4CTL0 | Read: | RXFRM | RXACT | CSWAI | SYNCH | TIME | WUPE | SLPRQ | INITRQ |
| | | Write: | | | | | | | | |
| $0281 | CAN4CTL1 | Read: | CANE | CLKSRC | LOOPB | LISTEN | 0 | WUPM | SLPAK | INITAK |
| | | Write: | | | | | | | | |
| $0282 | CAN4BTR0 | Read: | SJW1 | SJW0 | BRP5 | BRP4 | BRP3 | BRP2 | BRP1 | BRP0 |
| | | Write: | | | | | | | | |
| $0283 | CAN4BTR1 | Read: | SAMP | TSEG22 | TSEG21 | TSEG20 | TSEG13 | TSEG12 | TSEG11 | TSEG10 |
| | | Write: | | | | | | | | |
| $0284 | CAN4RFLG | Read: | WUPIF | CSCIF | RSTAT1 | RSTAT0 | TSTAT1 | TSTAT0 | OVRIF | RXF |
| | | Write: | | | | | | | | |
| $0285 | CAN4RIER | Read: | WUPIE | CSCIE | RSTATE1 | RSTATE0 | TSTATE1 | TSTATE0 | OVRIE | RXFIE |
| | | Write: | | | | | | | | |
| $0286 | CAN4TFLG | Read: | 0 | 0 | 0 | 0 | 0 | TXE2 | TXE1 | TXE0 |
| | | Write: | | | | | | | | |
| $0287 | CAN4TIER | Read: | 0 | 0 | 0 | 0 | 0 | TXEIE2 | TXEIE1 | TXEIE0 |
| | | Write: | | | | | | | | |
| $0288 | CAN4TARQ | Read: | 0 | 0 | 0 | 0 | 0 | ABTRQ2 | ABTRQ1 | ABTRQ0 |
| | | Write: | | | | | | | | |
| $0289 | CAN4TAAK | Read: | 0 | 0 | 0 | 0 | 0 | ABTAK2 | ABTAK1 | ABTAK0 |
| | | Write: | | | | | | | | |
| $028A | CAN4TBSEL | Read: | 0 | 0 | 0 | 0 | 0 | TX2 | TX1 | TX0 |
| | | Write: | | | | | | | | |
| $028B | CAN4IDAC | Read: | 0 | 0 | IDAM1 | IDAM0 | 0 | IDHIT2 | IDHIT1 | IDHIT0 |
| | | Write: | | | | | | | | |
| $028C | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $028D | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $028E | CAN4RXERR | Read: | RXERR7 | RXERR6 | RXERR5 | RXERR4 | RXERR3 | RXERR2 | RXERR1 | RXERR0 |
| | | Write: | | | | | | | | |
| $028F | CAN4TXERR | Read: | TXERR7 | TXERR6 | TXERR5 | TXERR4 | TXERR3 | TXERR2 | TXERR1 | TXERR0 |
| | | Write: | | | | | | | | |
| $0290 - $0293 | CAN0IDAR0 - CAN0IDAR3 | Read: | AC7 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |
| | | Write: | | | | | | | | |
| $0294 - $0297 | CAN0IDMR0 - CAN0IDMR3 | Read: | AM7 | AM6 | AM5 | AM4 | AM3 | AM2 | AM1 | AM0 |
| | | Write: | | | | | | | | |
| $0298 - $029B | CAN0IDAR4 - CAN0IDAR7 | Read: | AC7 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |
| | | Write: | | | | | | | | |
| $029C - $029F | CAN0IDMR4 - CAN0IDMR7 | Read: | AM7 | AM6 | AM5 | AM4 | AM3 | AM2 | AM1 | AM0 |
| $02A0 - $02AF | CAN4RXFG | Read: | FOREGROUND RECEIVE BUFFER see **Table 1-2** | | | | | | | |
| | | Write: | | | | | | | | |
| $02B0 - $02BF | CAN4TXFG | Read: | FOREGROUND TRANSMIT BUFFER see **Table 1-2** | | | | | | | |
| | | Write: | | | | | | | | |

### 2.3.6 PAD[15] / AN1[7] / ETRIG1 — Port AD Input Pin [15]

PAD15 is a general purpose input pin and analog input of the analog to digital converter ATD1. It can act as an external trigger input for the ATD1.

### 2.3.7 PAD[14:8] / AN1[6:0] — Port AD Input Pins [14:8]

PAD14 - PAD8 are general purpose input pins and analog inputs of the analog to digital converter ATD1.

### 2.3.8 PAD[7] / AN0[7] / ETRIG0 — Port AD Input Pin [7]

PAD7 is a general purpose input pin and analog input of the analog to digital converter ATD0. It can act as an external trigger input for the ATD0.

### 2.3.9 PAD[6:0] / AN0[6:0] — Port AD Input Pins [6:0]

PAD6 - PAD8 are general purpose input pins and analog inputs of the analog to digital converter ATD0.

### 2.3.10 PA[7:0] / ADDR[15:8] / DATA[15:8] — Port A I/O Pins

PA7-PA0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

### 2.3.11 PB[7:0] / ADDR[7:0] / DATA[7:0] — Port B I/O Pins

PB7-PB0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

### 2.3.12 PE7 / NOACC / $\overline{\text{XCLKS}}$ — Port E I/O Pin 7

PE7 is a general purpose input or output pin. During MCU expanded modes of operation, the NOACC signal, when enabled, is used to indicate that the current bus cycle is an unused or “free” cycle. This signal will assert when the CPU is not using the bus.
The $\overline{\text{XCLKS}}$ is an input signal which controls whether a crystal in combination with the internal Colpitts (low power) oscillator is used or whether Pierce oscillator/external clock circuitry is used. The state of this pin is latched at the rising edge of $\overline{\text{RESET}}$. If the input is a logic low the EXTAL pin is configured for an external clock drive. If input is a logic high an oscillator circuit is configured on EXTAL and XTAL. Since this pin is an input with a pull-up device during reset, if the pin is left floating, the default configuration is an oscillator circuit on EXTAL and XTAL.

### 2.3.13 PE6 / MODB / IPIPE1 — Port E I/O Pin 6

PE6 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODB bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE1. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low.

### 2.3.14 PE5 / MODA / IPIPE0 — Port E I/O Pin 5

PE5 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODA bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE0. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low.

### 2.3.15 PE4 / ECLK — Port E I/O Pin 4

PE4 is a general purpose input or output pin. It can be configured to drive the internal bus clock ECLK. ECLK can be used as a timing reference.

### 2.3.16 PE3 / $\overline{\text{LSTRB}}$ / $\overline{\text{TAGLO}}$ — Port E I/O Pin 3

PE3 is a general purpose input or output pin. In MCU expanded modes of operation, $\overline{\text{LSTRB}}$ can be used for the low-byte strobe function to indicate the type of bus access and when instruction tagging is on, $\overline{\text{TAGLO}}$ is used to tag the low half of the instruction word being read into the instruction queue.

### 2.3.17 PE2 / R/$\overline{\text{W}}$ — Port E I/O Pin 2

PE2 is a general purpose input or output pin. In MCU expanded modes of operations, this pin drives the read/write output signal for the external bus. It indicates the direction of data on the external bus.

### 2.3.18 PE1 / $\overline{\text{IRQ}}$ — Port E Input Pin 1

PE1 is a general purpose input pin and the maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

### 2.3.19 PE0 / $\overline{\text{XIRQ}}$ — Port E Input Pin 0

PE0 is a general purpose input pin and the non-maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

### 2.3.20 PH7 / KWH7 — Port H I/O Pin 7

PH7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

### 2.3.36 PM4 / BF_PSYN / RXCAN0 / RXCAN4/ MOSI0 — Port M I/O Pin 4

PM4 is a general purpose input or output pin. It can be configured as the correct synchronisation pulse reception/transmission output pulse pin of Byteflight. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controllers 0 or 4 (CAN0 or CAN4). It can be configured as the master output (during master mode) or slave input pin (during slave mode) MOSI for the Serial Peripheral Interface 0 (SPI0).

### 2.3.37 PM3 / TX_BF / TXCAN1 / TXCAN0 / $\overline{SS0}$ — Port M I/O Pin 3

PM3 is a general purpose input or output pin. It can be configured as the transmit pinTX_BF of Byteflight. It can be configured as the transmit pin TXCAN of the Motorola Scalable Controller Area Network controllers 1 or 0 (CAN1 or CAN0). It can be configured as the slave select pin $\overline{SS}$ of the Serial Peripheral Interface 0 (SPI0).

### 2.3.38 PM2 / RX_BF / RXCAN1 / RXCAN0 / MISO0 — Port M I/O Pin 2

PM2 is a general purpose input or output pin. It can be configured as the receive pin RX_BF of Byteflight. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controllers 1 or 0 (CAN1 or CAN0). It can be configured as the master input (during master mode) or slave output pin (during slave mode) MISO for the Serial Peripheral Interface 0 (SPI0).

### 2.3.39 PM1 / TXCAN0 / TXB — Port M I/O Pin 1

PM1 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Motorola Scalable Controller Area Network controller 0 (CAN0). It can be configured as the transmit pin TXB of the BDLC.

### 2.3.40 PM0 / RXCAN0 / RXB — Port M I/O Pin 0

PM0 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controller 0 (CAN0). It can be configured as the receive pin RXB of the BDLC.

### 2.3.41 PP7 / KWP7 / PWM7 — Port P I/O Pin 7

PP7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 7 output.

### 2.3.42 PP6 / KWP6 / PWM6 — Port P I/O Pin 6

PP6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 6 output.

# Section 5 Resets and Interrupts

## 5.1 Overview

Consult the Exception Processing section of the HCS12 Core User Guide for information on resets and interrupts.

## 5.2 Vectors

### 5.2.1 Vector Table

**Table 5-1** lists interrupt sources and vectors in default order of priority.

**Table 5-1 Interrupt Vector Locations**

| Vector Address | Interrupt Source | CCR Mask | Local Enable | HPRIO Value to Elevate |
|---|---|---|---|---|
| $FFFE, $FFFF | Reset | None | None | – |
| $FFFC, $FFFD | Clock Monitor fail reset | None | COPCTL (CME, FCME) | – |
| $FFFA, $FFFB | COP failure reset | None | COP rate select | – |
| $FFF8, $FFF9 | Unimplemented instruction trap | None | None | – |
| $FFF6, $FFF7 | SWI | None | None | – |
| $FFF4, $FFF5 | XIRQ / BF High prio Sync pulse intr | X-Bit | None / BFRIER (XSYNIE) | – |
| $FFF2, $FFF3 | IRQ | I-Bit | INTCR (IRQEN) | $F2 |
| $FFF0, $FFF1 | Real Time Interrupt | I-Bit | CRGINT (RTIE) | $F0 |
| $FFEE, $FFEF | Enhanced Capture Timer channel 0 | I-Bit | TIE (C0I) | $EE |
| $FFEC, $FFED | Enhanced Capture Timer channel 1 | I-Bit | TIE (C1I) | $EC |
| $FFEA, $FFEB | Enhanced Capture Timer channel 2 | I-Bit | TIE (C2I) | $EA |
| $FFE8, $FFE9 | Enhanced Capture Timer channel 3 | I-Bit | TIE (C3I) | $E8 |
| $FFE6, $FFE7 | Enhanced Capture Timer channel 4 | I-Bit | TIE (C4I) | $E6 |
| $FFE4, $FFE5 | Enhanced Capture Timer channel 5 | I-Bit | TIE (C5I) | $E4 |
| $FFE2, $FFE3 | Enhanced Capture Timer channel 6 | I-Bit | TIE (C6I) | $E2 |
| $FFE0, $FFE1 | Enhanced Capture Timer channel 7 | I-Bit | TIE (C7I) | $E0 |
| $FFDE, $FFDF | Enhanced Capture Timer overflow | I-Bit | TSCR2 (TOF) | $DE |
| $FFDC, $FFDD | Pulse accumulator A overflow | I-Bit | PACTL (PAOVI) | $DC |
| $FFDA, $FFDB | Pulse accumulator input edge | I-Bit | PACTL (PAI) | $DA |
| $FFD8, $FFD9 | SPI0 | I-Bit | SPICR1 (SPIE, SPTIE) | $D8 |
| $FFD6, $FFD7 | SCI0 | I-Bit | SCICR2 (TIE, TCIE, RIE, ILIE) | $D6 |
| $FFD4, $FFD5 | SCI1 | I-Bit | SCICR2 (TIE, TCIE, RIE, ILIE) | $D4 |
| $FFD2, $FFD3 | ATD0 | I-Bit | ATDCTL2 (ASCIE) | $D2 |
| $FFD0, $FFD1 | ATD1 | I-Bit | ATDCTL2 (ASCIE) | $D0 |
| $FFCE, $FFCF | Port J | I-Bit | PIEJ (PIEJ7, PIEJ6, PIEJ1, PIEJ0) | $CE |
| $FFCC, $FFCD | Port H | I-Bit | PIEH (PIEH7-0) | $CC |

| | | | | |
|---|---|---|---|---|
| $FFCA, $FFCB | Modulus Down Counter underflow | I-Bit | MCCTL (MCZI) | $CA |
| $FFC8, $FFC9 | Pulse Accumulator B Overflow | I-Bit | PBCTL (PBOVI) | $C8 |
| $FFC6, $FFC7 | CRG PLL lock | I-Bit | PLLCR (LOCKIE) | $C6 |
| $FFC4, $FFC5 | CRG Self Clock Mode | I-Bit | PLLCR (SCMIE) | $C4 |
| $FFC2, $FFC3 | BDLC | I-Bit | DLCBCR1 (IE) | $C2 |
| $FFC0, $FFC1 | IIC Bus | I-Bit | IBCR (IBIE) | $C0 |
| $FFBE, $FFBF | SPI1 | I-Bit | SPICR1 (SPIE, SPTIE) | $BE |
| $FFBC, $FFBD | Reserved | | | |
| $FFBA, $FFBB | EEPROM | I-Bit | ECNFG (CCIE, CBEIE) | $BA |
| $FFB8, $FFB9 | FLASH | I-Bit | FCNFG (CCIE, CBEIE) | $B8 |
| $FFB6, $FFB7 | CAN0 wake-up | I-Bit | CANRIER (WUPIE) | $B6 |
| $FFB4, $FFB5 | CAN0 errors | I-Bit | CANRIER (CSCIE, OVRIE) | $B4 |
| $FFB2, $FFB3 | CAN0 receive | I-Bit | CANRIER (RXFIE) | $B2 |
| $FFB0, $FFB1 | CAN0 transmit | I-Bit | CANTIER (TXEIE[2:0]) | $B0 |
| $FFAE, $FFAF | CAN1 wake-up | I-Bit | CANRIER (WUPIE) | $AE |
| $FFAC, $FFAD | CAN1 errors | I-Bit | CANRIER (CSCIE, OVRIE) | $AC |
| $FFAA, $FFAB | CAN1 receive | I-Bit | CANRIER (RXFIE) | $AA |
| $FFA8, $FFA9 | CAN1 transmit | I-Bit | CANTIER (TXEIE[2:0]) | $A8 |
| $FFA6, $FFA7 | BF Rx FIFO not empty | I-Bit | BFRIER (RCVFIE) | $A6 |
| $FFA4, $FFA5 | BF receive | I-Bit | BFBUFCTL[15:0] (IENA) | $A4 |
| $FFA2, $FFA3 | BF Synchronisation | I-Bit | BFRIER (SYNAIE, SYNNIE) | $A2 |
| $FFA0, $FFA1 | BF general | I-Bit | BFBUFCTL[15:0] (IENA), BFGIER (OVRNIE, ERRIE, SYNEIE, SYNLIE, ILLPIE, LOCKIE, WAKEIE) BFRIER (SLMMIE) | $A0 |
| $FF98, $FF9F | Reserved | | | |
| $FF96, $FF97 | CAN4 wake-up | I-Bit | CANRIER (WUPIE) | $96 |
| $FF94, $FF95 | CAN4 errors | I-Bit | CANRIER (CSCIE, OVRIE) | $94 |
| $FF92, $FF93 | CAN4 receive | I-Bit | CANRIER (RXFIE) | $92 |
| $FF90, $FF91 | CAN4 transmit | I-Bit | CANTIER (TXEIE[2:0]) | $90 |
| $FF8E, $FF8F | Port P Interrupt | I-Bit | PIEP (PIEP7-0) | $8E |
| $FF8C, $FF8D | PWM Emergency Shutdown | I-Bit | PWMSDN (PWMIE) | $8C |
| $FF80 to $FF8B | Reserved | | | |

## 5.3 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module Block User Guides for register reset states.

### 5.3.1 I/O pins

Refer to the HCS12 Core User Guides for mode dependent pin configuration of port A, B, E and K out of reset.

Refer to the PIM Block User Guide for reset configurations of all peripheral module ports.

***NOTE:*** *In the following context VDD5 is used for either VDDA, VDDR and VDDX; VSS5 is used for either VSSA, VSSR and VSSX unless otherwise noted.*
*IDD5 denotes the sum of the currents flowing into the VDDA, VDDX and VDDR pins.*
*VDD is used for VDD1, VDD2 and VDDPLL, VSS is used for VSS1, VSS2 and VSSPLL.*
*IDD is used for the sum of the currents flowing into VDD1 and VDD2.*

## A.1.3 Pins

There are four groups of functional pins.

### A.1.3.1 5V I/O pins

Those I/O pins have a nominal level of 5V. This class of pins is comprised of all port I/O pins, the analog inputs, BKGD pin and the RESET inputs.The internal structure of all those pins is identical, however some of the functionality may be disabled. E.g. for the analog inputs the output drivers, pull-up and pull-down resistors are disabled permanently.

### A.1.3.2 Analog Reference

This class is made up by the two VRH and VRL pins.

### A.1.3.3 Oscillator

The pins XFC, EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

### A.1.3.4 TEST

This pin is used for production testing only.

### A.1.3.5 VREGEN

This pin is used to enable the on chip voltage regulator.

## A.1.4 Current Injection

Power supply must maintain regulation within operating $V_{DD5}$ or $V_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD5}$) is greater than $I_{DD5}$, the injection current may flow out of VDD5 and could result in external power supply going out of regulation. Insure external VDD5 load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power; e.g. if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table A-2 ESD and Latch-up Test Conditions**

| Model | Description | Symbol | Value | Unit |
|---|---|---|---|---|
| Human Body | Series Resistance | R1 | 1500 | Ohm |
| | Storage Capacitance | C | 100 | pF |
| | Number of Pulse per pin<br>positive<br>negative | – | –<br>3<br>3 | |
| Machine | Series Resistance | R1 | 0 | Ohm |
| | Storage Capacitance | C | 200 | pF |
| | Number of Pulse per pin<br>positive<br>negative | – | –<br>3<br>3 | |
| Latch-up | Minimum input voltage limit | | –2.5 | V |
| | Maximum input voltage limit | | 7.5 | V |

**Table A-3 ESD and Latch-Up Protection Characteristics**

| Num | C | Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | C | Human Body Model (HBM) | $V_{HBM}$ | 2000 | – | V |
| 2 | C | Machine Model (MM) | $V_{MM}$ | 200 | – | V |
| 3 | C | Charge Device Model (CDM) | $V_{CDM}$ | 500 | – | V |
| 4 | C | Latch-up Current at 125°C<br>positive<br>negative | $I_{LAT}$ | +100<br>–100 | – | mA |
| 5 | C | Latch-up Current at 27°C<br>positive<br>negative | $I_{LAT}$ | +200<br>–200 | – | mA |

## A.1.7 Operating Conditions

This chapter describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

***NOTE:*** *Please refer to the temperature rating of the device (C, V, M) with regards to the ambient temperature $T_A$ and the junction temperature $T_J$. For power dissipation*

## A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

### A.1.10.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 25MHz bus frequency using a 4MHz oscillator in Colpitts mode. Production testing is performed using a square wave signal at the EXTAL input.

### A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be

## A.6 MSCAN

### Table A-17 MSCAN Wake-up Pulse Characteristics

| Conditions are shown in **Table A-4** unless otherwise noted | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Num** | **C** | **Rating** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
| 1 | P | MSCAN Wake-up dominant pulse filtered | $t_{WUP}$ | | | 2 | µs |
| 2 | P | MSCAN Wake-up dominant pulse pass | $t_{WUP}$ | 5 | | | µs |

## Table A-19 SPI Slave Mode Timing Characteristics

| Conditions are shown in **Table A-4** unless otherwise noted, CLOAD = 200pF on all outputs | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Num** | **C** | **Rating** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
| 1 | P | Operating Frequency | $f_{op}$ | DC | | 1/4 | $f_{bus}$ |
| 1 | P | SCK Period $t_{sck} = 1./f_{op}$ | $t_{sck}$ | 4 | | 2048 | $t_{bus}$ |
| 2 | D | Enable Lead Time | $t_{lead}$ | 1 | | | $t_{cyc}$ |
| 3 | D | Enable Lag Time | $t_{lag}$ | 1 | | | $t_{cyc}$ |
| 4 | D | Clock (SCK) High or Low Time | $t_{wsck}$ | $t_{cyc} – 30$ | | | ns |
| 5 | D | Data Setup Time (Inputs) | $t_{su}$ | 25 | | | ns |
| 6 | D | Data Hold Time (Inputs) | $t_{hi}$ | 25 | | | ns |
| 7 | D | Slave Access Time | $t_a$ | | | 1 | $t_{cyc}$ |
| 8 | D | Slave MISO Disable Time | $t_{dis}$ | | | 1 | $t_{cyc}$ |
| 9 | D | Data Valid (after SCK Edge) | $t_v$ | | | 25 | ns |
| 10 | D | Data Hold Time (Outputs) | $t_{ho}$ | 0 | | | ns |
| 11 | D | Rise Time Inputs and Outputs | $t_r$ | | | 25 | ns |
| 12 | D | Fall Time Inputs and Outputs | $t_f$ | | | 25 | ns |

# A.8 External Bus Timing

A timing diagram of the external multiplexed-bus is illustrated in **Figure A-9** with the actual timing values shown on table **Table A-20**. All major bus signals are included in the diagram. While both a data write and data read cycle are shown, only one or the other would occur on a particular bus cycle.

## A.8.1 General Muxed Bus Timing

The expanded bus timings are highly dependent on the load conditions. The timing parameters shown assume a balanced load across all outputs.

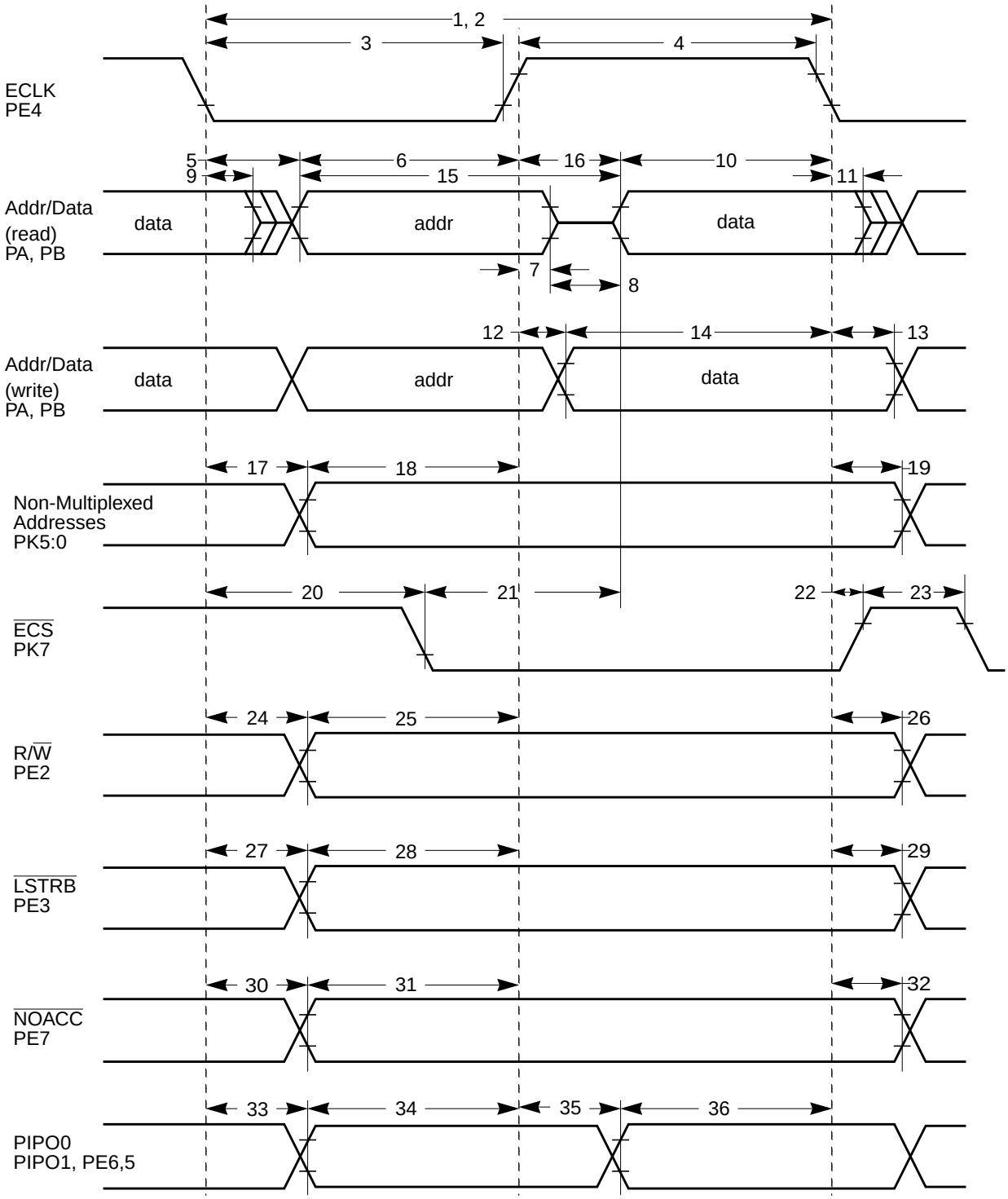
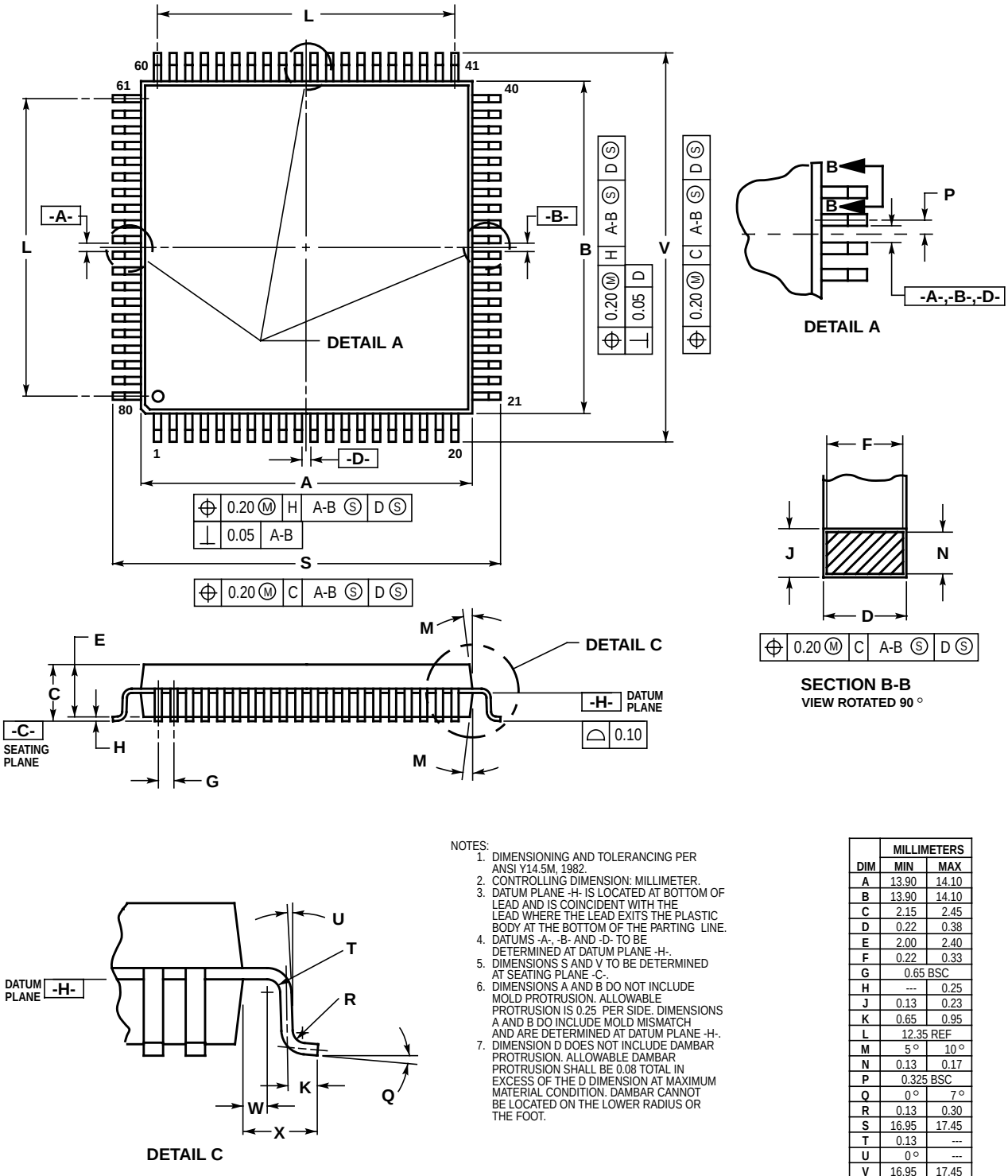



**Figure A-9 General External Bus Timing**

## Table A-20 Expanded Bus Timing Characteristics

| Conditions are shown in **Table A-4** unless otherwise noted, $C_{LOAD}$ = 50pF | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Num** | **C** | **Rating** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
| 1 | P | Frequency of operation (E-clock) | $f_o$ | 0 | | 25.0 | MHz |
| 2 | P | Cycle time | $t_{cyc}$ | 40 | | | ns |
| 3 | D | Pulse width, E low | $PW_{EL}$ | 19 | | | ns |
| 4 | D | Pulse width, E high[1] | $PW_{EH}$ | 19 | | | ns |
| 5 | D | Address delay time | $t_{AD}$ | | | 8 | ns |
| 6 | D | Address valid time to E rise ($PW_{EL}$–$t_{AD}$) | $t_{AV}$ | 11 | | | ns |
| 7 | D | Muxed address hold time | $t_{MAH}$ | 2 | | | ns |
| 8 | D | Address hold to data valid | $t_{AHDS}$ | 7 | | | ns |
| 9 | D | Data hold to address | $t_{DHA}$ | 2 | | | ns |
| 10 | D | Read data setup time | $t_{DSR}$ | 13 | | | ns |
| 11 | D | Read data hold time | $t_{DHR}$ | 0 | | | ns |
| 12 | D | Write data delay time | $t_{DDW}$ | | | 7 | ns |
| 13 | D | Write data hold time | $t_{DHW}$ | 2 | | | ns |
| 14 | D | Write data setup time(1) ($PW_{EH}$–$t_{DDW}$) | $t_{DSW}$ | 12 | | | ns |
| 15 | D | Address access time(1) ($t_{cyc}$–$t_{AD}$–$t_{DSR}$) | $t_{ACCA}$ | 19 | | | ns |
| 16 | D | E high access time(1) ($PW_{EH}$–$t_{DSR}$) | $t_{ACCE}$ | 6 | | | ns |
| 17 | D | Non-multiplexed address delay time | $t_{NAD}$ | | | 6 | ns |
| 18 | D | Non-muxed address valid to E rise ($PW_{EL}$–$t_{NAD}$) | $t_{NAV}$ | 15 | | | ns |
| 19 | D | Non-multiplexed address hold time | $t_{NAH}$ | 2 | | | ns |
| 20 | D | Chip select delay time | $t_{CSD}$ | | | 16 | ns |
| 21 | D | Chip select access time(1) ($t_{cyc}$–$t_{CSD}$–$t_{DSR}$) | $t_{ACCS}$ | 11 | | | ns |
| 22 | D | Chip select hold time | $t_{CSH}$ | 2 | | | ns |
| 23 | D | Chip select negated time | $t_{CSN}$ | 8 | | | ns |
| 24 | D | Read/write delay time | $t_{RWD}$ | | | 7 | ns |
| 25 | D | Read/write valid time to E rise ($PW_{EL}$–$t_{RWD}$) | $t_{RWV}$ | 14 | | | ns |
| 26 | D | Read/write hold time | $t_{RWH}$ | 2 | | | ns |
| 27 | D | Low strobe delay time | $t_{LSD}$ | | | 7 | ns |
| 28 | D | Low strobe valid time to E rise ($PW_{EL}$–$t_{LSD}$) | $t_{LSV}$ | 14 | | | ns |
| 29 | D | Low strobe hold time | $t_{LSH}$ | 2 | | | ns |
| 30 | D | NOACC strobe delay time | $t_{NOD}$ | | | 7 | ns |
| 31 | D | NOACC valid time to E rise ($PW_{EL}$–$t_{NOD}$) | $t_{NOV}$ | 14 | | | ns |

## B.3 80-pin QFP package




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 13.90 | 14.10 |
| B | 13.90 | 14.10 |
| C | 2.15 | 2.45 |
| D | 0.22 | 0.38 |
| E | 2.00 | 2.40 |
| F | 0.22 | 0.33 |
| G | 0.65 BSC | |
| H | --- | 0.25 |
| J | 0.13 | 0.23 |
| K | 0.65 | 0.95 |
| L | 12.35 REF | |
| M | 5° | 10° |
| N | 0.13 | 0.17 |
| P | 0.325 BSC | |
| Q | 0° | 7° |
| R | 0.13 | 0.30 |
| S | 16.95 | 17.45 |
| T | 0.13 | --- |
| U | 0° | --- |
| V | 16.95 | 17.45 |
| W | 0.35 | 0.45 |
| X | 1.6 REF | |

**Figure 1 80-pin QFP Mechanical Dimensions (case no. 841B)**