What is "**Embedded - Microcontrollers**"?

"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gp304t-i-pt

3.4   CPU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en530331

3.4.1   KEY RESOURCES

- **Section 2. "CPU"** (DS70204)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

REGISTER 3-1: **SR: CPU STATUS REGISTER (CONTINUED)**

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits[2]

111 = CPU Interrupt Priority Level is 7 (15), user interrupts disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

bit 4 **RA:** REPEAT Loop Active bit

1 = REPEAT loop in progress
0 = REPEAT loop not in progress

bit 3 **N:** MCU ALU Negative bit

1 = Result was negative
0 = Result was non-negative (zero or positive)

bit 2 **OV:** MCU ALU Overflow bit

This bit is used for signed arithmetic (2's complement). It indicates an overflow of a magnitude that causes the sign bit to change state.
1 = Overflow occurred for signed arithmetic (in this arithmetic operation)
0 = No overflow occurred

bit 1 **Z:** MCU ALU Zero bit

1 = An operation that affects the Z bit has set it at some time in the past
0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)

bit 0 **C:** MCU ALU Carry/Borrow bit

1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: This bit can be read or cleared (not set).

2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level (IPL). The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.

3: The IPL<2:0> Status bits are read only when NSTDIS = 1 (INTCON1<15>).

TABLE 4-20: SYSTEM CONTROL REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	—	—	—	—	CM	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	xxxx[1]
OSCCON	0742	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	IOLOCK	LOCK	—	CF	—	LPOSCEN	OSWEN	0300[2]
CLKDIV	0744	ROI	DOZE<2:0>			DOZEN	FRCDIV<2:0>			PLLPOST<1:0>		—	PLLPRE<4:0>						3040
PLLFBD	0746	—	—	—	—	—	—	—	PLLDIV<8:0>										0030
OSCTUN	0748	—	—	—	—	—	—	—	—	—	—	TUN<5:0>							0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: RCON register Reset values dependent on type of Reset.
    2: OSCCON register Reset values dependent on the FOSC Configuration bits and by type of Reset.

TABLE 4-21: NVM REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0760	WR	WREN	WRERR	—	—	—	—	—	—	ERASE	—	—	NVMOP<3:0>					0000[1]
NVMKEY	0766	—	—	—	—	—	—	—	—	NVMKEY<7:0>									0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: Reset value shown is for POR only. Value on other Reset states is dependent on the state of memory write or erase operations at the time of Reset.

TABLE 4-22: PMD REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	—	—	T3MD	T2MD	T1MD	—	—	—	I2C1MD	—	U1MD	—	SPI1MD	—	—	AD1MD	0000
PMD2	0772	IC8MD	IC7MD	—	—	—	—	IC2MD	IC1MD	—	—	—	—	—	—	OC2MD	OC1MD	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4.1 SOFTWARE STACK

In addition to its use as a working register, the W15 register in the dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 devices is also used as a software Stack Pointer. The Stack Pointer always points to the first available free word and grows from lower to higher addresses. It pre-decrements for stack pops and post-increments for stack pushes, as shown in Figure 4-4. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, ensuring that the MSB is always clear.

> **Note:** A PC push during exception processing concatenates the SRL register to the MSB of the PC prior to the push.

The Stack Pointer Limit register (SPLIM) associated with the Stack Pointer sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '0' because all stack operations must be word-aligned.

When an EA is generated using W15 as a source or destination pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal and a push operation is performed, a stack error trap will not occur. The stack error trap will occur on a subsequent push operation. For example, to cause a stack error trap when the stack grows beyond address 0x1000 in RAM, initialize the SPLIM with the value 0x0FFE.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0x0800. This prevents the stack from interfering with the Special Function Register (SFR) space.

A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.

FIGURE 4-4: CALL STACK FRAME
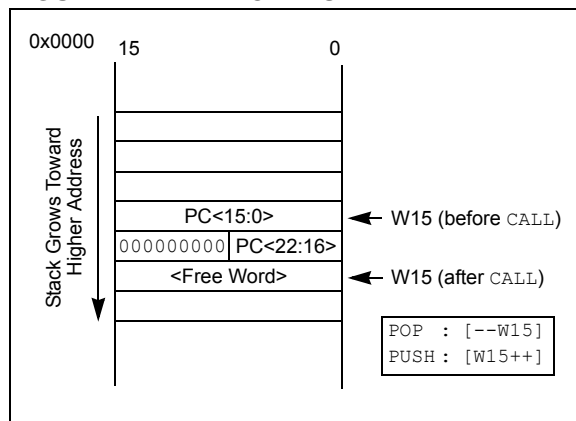
4.4.2 DATA RAM PROTECTION FEATURE

The dsPIC33F product family supports Data RAM protection features that enable segments of RAM to be protected when used in conjunction with Boot and Secure Code Segment Security. BSRAM (Secure RAM segment for Boot Segment) is accessible only from the Boot Segment Flash code when enabled. SSRAM (Secure RAM segment for RAM) is accessible only from the Secure Segment Flash code when enabled. See Table 4-1 for an overview of the BSRAM and SSRAM SFRs.

4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-23 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire data space.

4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where:

Operand 1 is always a working register (that is, the addressing mode can only be register direct), which is referred to as Wb.

Operand 2 can be a W register, fetched from data memory, or a 5-bit literal.

The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

• Register Direct
• Register Indirect
• Register Indirect Post-Modified
• Register Indirect Pre-Modified
• 5-bit or 10-bit Literal

> **Note:** Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

5.2   RTSP Operation

The dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user application to erase a page of memory, which consists of eight rows (512 instructions) at a time, and to program one row or one word at a time. The 8-row erase pages and single row write rows are edge-aligned from the beginning of program memory, on boundaries of 1536 bytes and 192 bytes, respectively.

The program memory implements holding buffers that can contain 64 instructions of programming data. Prior to the actual programming operation, the write data must be loaded into the buffers sequentially. The instruction words loaded must always be from a group of 64 boundary.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of TBLWT instructions to load the buffers. Programming is performed by setting the control bits in the NVMCON register. A total of 64 TBLWTL and TBLWTH instructions are required to load the instructions.

All of the table write operations are single-word writes (two instruction cycles) because only the buffers are written. A programming cycle is required for programming each row.

5.3   Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

The programming time depends on the FRC accuracy (see Table 22-18) and the value of the FRC Oscillator Tuning register (see Register 8-4). Use the following formula to calculate the minimum and maximum values for the Row Write Time, Page Erase Time, and Word Write Cycle Time parameters (see Table 22-12).

EQUATION 5-1:   PROGRAMMING TIME

$$\frac{T}{7.37\ MHz \times (FRC\ Accuracy)\% \times (FRC\ Tuning)\%}$$

For example, if the device is operating at +125° C, the FRC accuracy will be ±5%. If the TUN<5:0> bits (see Register 8-4) are set to 'b111111, the minimum row write time is equal to Equation 5-2.

EQUATION 5-2:   MINIMUM ROW WRITE TIME

$$T_{RW} = \frac{11064\ Cycles}{7.37\ MHz \times (1 + 0.05) \times (1 - 0.00375)} = 1.435ms$$

The maximum row write time is equal to Equation 5-3.

EQUATION 5-3:   MAXIMUM ROW WRITE TIME

$$T_{RW} = \frac{11064\ Cycles}{7.37\ MHz \times (1 - 0.05) \times (1 - 0.00375)} = 1.586ms$$

Setting the WR bit (NVMCON<15>) starts the operation, and the WR bit is automatically cleared when the operation is finished.

5.4   Flash Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| Note: | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en530331 |

5.4.1   KEY RESOURCES

- **Section 5. "Flash Programming"** (DS70191)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

5.5   Control Registers

The two SFRs that are used to read and write the program Flash memory are:

- **NVMCON: Flash Memory Control Register**
- **NVMKEY: Nonvolatile Memory Key Register**

The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

NVMKEY (Register 5-2) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register. Refer to **Section 5.3 "Programming Operations"** for further details.

6.1 Resets Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

> **Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en530331

6.1.1 KEY RESOURCES

- **Section 8. "Reset"** (DS70192)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

REGISTER 7-8: **IEC0: INTERRUPT ENABLE CONTROL REGISTER 0 (CONTINUED)**

bit 1   **IC1IE:** Input Capture Channel 1 Interrupt Enable bit

1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 0   **INT0IE:** External Interrupt 0 Enable bit

1 = Interrupt request enabled
0 = Interrupt request not enabled

8.2 Oscillator Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

> **Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en530331

8.2.1 KEY RESOURCES

- **Section 7. "Oscillator"** (DS70186)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

REGISTER 8-2:   CLKDIV: CLOCK DIVISOR REGISTER[2] (CONTINUED)

bit 4-0   **PLLPRE<4:0>:** PLL Phase Detector Input Divider bits (also denoted as 'N1', PLL prescaler)

11111 = Input/33

•

•

•

00001 = Input/3

00000 = Input/2 (default)

Note 1: This bit is cleared when the ROI bit is set and an interrupt occurs.

2: This register is reset only on a Power-on Reset (POR).

10.2 Open-Drain Configuration

In addition to the PORT, LAT and TRIS registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than V_{DD} (e.g., 5V) on any desired 5V tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum V_{IH} specification.

See **"Pin Diagrams"** for the available pins and their functionality.

10.3 Configuring Analog Port Pins

The AD1PCFG and TRIS registers control the operation of the analog-to-digital (A/D) port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level (V_{OH} or V_{OL}) will be converted.

The AD1PCFGL register has a default value of 0x0000; therefore, all pins that share ANx functions are analog (not digital) by default.

When the PORT register is read, all pins configured as analog input channels will read as cleared (a low level).

Pins configured as digital inputs will not convert an analog input. Analog levels on any pin that is defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

10.4 I/O Port Write/Read Timing

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP. Examples are shown in Example 10-1 and Example 10-2. This also applies to PORT bit operations, such as BSET PORTB, # RB0, which are single cycle read-modify-write. All PORT bit operations, such as MOV PORTB, W0 or BSET PORTB, # RBx, read the pin and *not* the latch.

10.5 Input Change Notification

The input change notification function of the I/O ports allows the dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature can detect input change-of-states even in Sleep mode, when the clocks are disabled. Depending on the device pin count, up to 31 external signals (CNx pin) can be selected (enabled) for generating an interrupt request on a change-of-state.

Four control registers are associated with the CN module. The CNEN1 and CNEN2 registers contain the interrupt enable control bits for each of the CN input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CN pin also has a weak pull-up connected to it. The pull-ups act as a current source connected to the pin, and eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups are enabled separately using the CNPU1 and CNPU2 registers, which contain the control bits for each of the CN pins. Setting any of the control bits enables the weak pull-ups for the corresponding pins.

> **Note:** Pull-ups on change notification pins should always be disabled when the port pin is configured as a digital output.

EXAMPLE 10-1: PORT WRITE/READ

```
MOV     0xFF00, W0          ;Configure PORTB<15:8> as inputs
MOV     W0, TRISBB          ;and PORTB<7:0> as outputs
NOP                         ;Delay 1 cycle
BTSS    PORTB, #13          ;Next Instruction
```

EXAMPLE 10-2: PORT BIT OPERATIONS

```
Incorrect:
BSET    PORTB, #RB1         ;Set PORTB<RB1> high
BSET    PORTB, #RB6         ;Set PORTB<RB6> high

Correct:
BSET    PORTB, #RB1         ;Set PORTB<RB1> high
NOP
BSET    PORTB, #RB6         ;Set PORTB<RB6> high
NOP

Preferred:
BSET    LATB, LATB1         ;Set PORTB<RB1> high
BSET    LATB, LATB6         ;Set PORTB<RB6> high
```

10.6 Peripheral Pin Select

A major challenge in general-purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low-pin count devices. In an application where more than one peripheral must be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

Peripheral Pin Select configuration enables peripheral set selection and placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, programmers can better tailor the microcontroller to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Programmers can independently map the input and/or output of most digital peripherals to any one of these I/O pins. Peripheral Pin Select is performed in software, and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping, once it has been established.

10.6.1 AVAILABLE PINS

The Peripheral Pin Select feature is used with a range of up to 26 pins. The number of available pins depends on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the designation "RPn" in their full pin designation, where "RP" designates a remappable peripheral and "n" is the remappable pin number.

10.6.2 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of special function registers: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

10.6.2.1 Input Mapping

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. A control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 10-1 through Register 10-9). Each register contains sets of 5-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 5-bit value maps the RPn pin with that value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

Figure 10-2 Illustrates remappable pin selection for U1RX input.

> **Note:** For input mapping only, the Peripheral Pin Select (PPS) functionality does not have priority over the TRISx settings. Therefore, when configuring the RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (i.e., set to '1').

FIGURE 10-2: REMAPPABLE MUX INPUT FOR U1RX
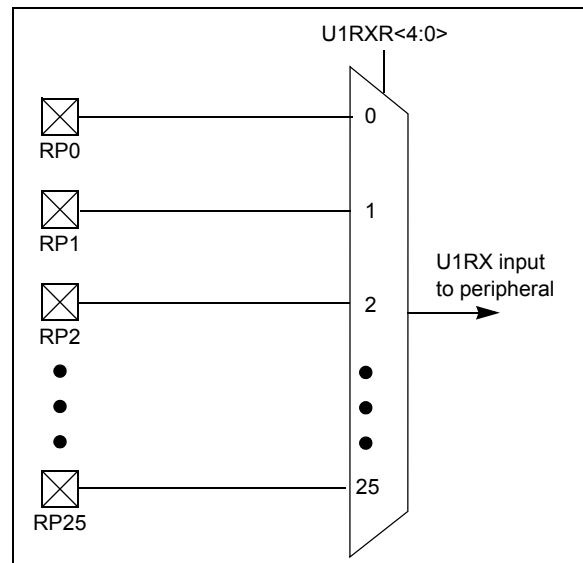
13.1   Input Capture Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en530331

13.1.1   KEY RESOURCES

• **Section 12. "Input Capture"** (DS70198)
• Code Samples
• Application Notes
• Software Libraries
• Webinars
• All related dsPIC33F/PIC24H Family Reference Manuals Sections
• Development Tools

REGISTER 18-2:   AD1CON2: ADC1 CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
VCFG<2:0>			—	—	CSCNA	CHPS<1:0>	
bit 15							bit 8

R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS	—	SMPI<3:0>				BUFM	ALTS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **VCFG<2:0>:** Converter Voltage Reference Configuration bits

	ADREF+	ADREF-
`000`	A$_{VDD}$	A$_{VSS}$
`001`	External V$_{REF}$+	A$_{VSS}$
`010`	A$_{VDD}$	External V$_{REF}$-
`011`	External V$_{REF}$+	External V$_{REF}$-
`1xx`	A$_{VDD}$	A$_{VSS}$

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **CSCNA:** Scan Input Selections for CH0+ during Sample A bit

    `1` = Scan inputs
    `0` = Do not scan inputs

bit 9-8 **CHPS<1:0>:** Select Channels Utilized bits

    When AD12B = `1`, CHPS<1:0> is: U-0, Unimplemented, Read as '0'
    `1x` = Converts CH0, CH1, CH2 and CH3
    `01` = Converts CH0 and CH1
    `00` = Converts CH0

bit 7 **BUFS:** Buffer Fill Status bit (valid only when BUFM = `1`)

    `1` = ADC is currently filling second half of buffer, user application should access data in the first half
    `0` = ADC is currently filling first half of buffer, user application should access data in the second half

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits

    `1111` = Interrupts at the completion of conversion for each 16th sample/convert sequence
    `1110` = Interrupts at the completion of conversion for each 15th sample/convert sequence
    •
    •
    •
    `0001` = Interrupts at the completion of conversion for each 2nd sample/convert sequence
    `0000` = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** Buffer Fill Mode Select bit

    `1` = Starts filling first half of buffer on first interrupt and the second half of buffer on next interrupt
    `0` = Always starts filling buffer from the beginning

bit 0 **ALTS:** Alternate Input Sample Mode Select bit

    `1` = Uses channel input selects for Sample A on first sample and Sample B on next sample
    `0` = Always uses channel input selects for Sample A

19.5 JTAG Interface

dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 devices implement a JTAG interface, which supports boundary scan device testing, as well as in-circuit programming. Detailed information on this interface will be provided in future revisions of the document.

19.6 Code Protection and CodeGuard™ Security

The dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 product families offer the intermediate implementation of CodeGuard™ Security. CodeGuard Security enables multiple parties to securely share resources (memory, interrupts and peripherals) on a single chip. This feature helps protect individual Intellectual Property in collaborative system designs.

When coupled with software encryption libraries, Code-Guard™ Security can be used to securely update Flash even when multiple IPs reside on the single chip.

The code protection features are controlled by the Configuration registers: FBS and FGS. The Secure segment and RAM is not implemented.

Note:	Refer to **Section 23. "CodeGuard™ Security"** (DS70199) in the *"dsPIC33F/PIC24H Family Reference Manual"* for further information on usage, configuration and operation of CodeGuard Security.

TABLE 19-3: CODE FLASH SECURITY SEGMENT SIZES FOR 32 KBYTE DEVICES

CONFIG BITS		
BSS<2:0>=x11 **0K**	VS = 256 IW	0x000000 0x0001FE
	GS = 11008 IW	0x000200 0x0007FE 0x000800 0x001FFE 0x002000 0x003FFE 0x004000 0x0057FE
BSS<2:0>=x10 **256**	VS = 256 IW	0x000000 0x0001FE
	BS = 768 IW	0x000200 0x0007FE 0x000800 0x001FFE 0x002000 0x003FFE 0x004000
	GS = 10240 IW	0x0057FE
BSS<2:0>=x01 **768**	VS = 256 IW	0x000000 0x0001FE
	BS = 3840 IW	0x000200 0x0007FE 0x000800 0x001FFE 0x002000 0x003FFE 0x004000
	GS = 7168 IW	0x0057FE
BSS<2:0>=x00 **1792**	VS = 256 IW	0x000000 0x0001FE
	BS = 7936 IW	0x000200 0x0007FE 0x000800 0x001FFE 0x002000 0x003FFE 0x004000
	GS = 3072 IW	0x0057FE

TABLE 19-4: CODE FLASH SECURITY SEGMENT SIZES FOR 16 KBYTE DEVICES

CONFIG BITS		
BSS<2:0>=x11 **0K**	VS = 256 IW	0x000000 0x0001FE
	GS = 5376 IW	0x000200 0x0007FE 0x000800 0x001FFE 0x002000 0x002BFE
BSS<2:0>=x10 **256**	VS = 256 IW	0x000000 0x0001FE
	BS = 768 IW	0x000200 0x0007FE 0x000800 0x001FFE 0x002000
	GS = 4608 IW	0x002BFE
BSS<2:0>=x01 **768**	VS = 256 IW	0x000000 0x0001FE
	BS = 3840 IW	0x000200 0x0007FE 0x000800 0x001FFE 0x002000
	GS = 1536 IW	0x002BFE
BSS<2:0>=x00 **1792**	VS = 256 IW	0x000000 0x0001FE
	BS = 5376 IW	0x000200 0x0007FE 0x000800 0x001FFE 0x002000 0x002BFE

FIGURE 22-5: **TIMER1, 2 AND 3 EXTERNAL CLOCK TIMING CHARACTERISTICS**

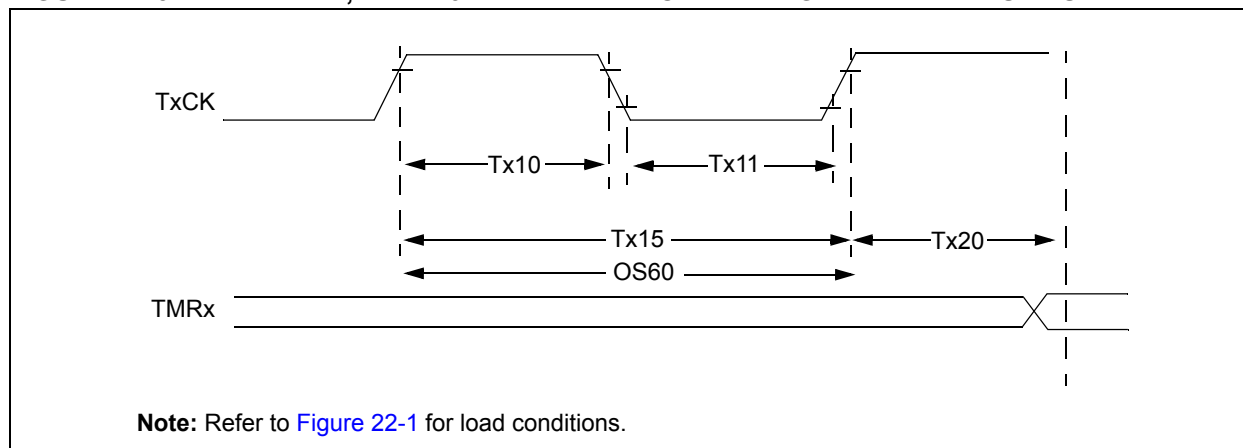Note: Refer to Figure 22-1 for load conditions.

TABLE 22-22: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS[1]

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	Symbol	Characteristic[2]		Min	Typ	Max	Units	Conditions
TA10	T_{TxH}	TxCK High Time	Synchronous, no prescaler	$0.5 T_{CY} + 20$	—	—	ns	Must also meet parameter TA15
			Synchronous, with prescaler	10	—	—	ns	
			Asynchronous	10	—	—	ns	
TA11	T_{TxL}	TxCK Low Time	Synchronous, no prescaler	$0.5 T_{CY} + 20$	—	—	ns	Must also meet parameter TA15
			Synchronous, with prescaler	10	—	—	ns	
			Asynchronous	10	—	—	ns	
TA15	T_{TxP}	TxCK Input Period	Synchronous, no prescaler	$T_{CY} + 40$	—	—	ns	—
			Synchronous, with prescaler	Greater of: 20 ns or $(T_{CY} + 40)/N$	—	—	—	N = prescale value (1, 8, 64, 256)
			Asynchronous	20	—	—	ns	—
OS60	Ft1	SOSC1/T1CK Oscillator Input frequency Range (oscillator enabled by setting bit TCS (T1CON<1>))		DC	—	50	kHz	—
TA20	$T_{CKEXTMRL}$	Delay from External TxCK Clock Edge to Timer Increment		$0.5 T_{CY}$	—	$1.5 T_{CY}$	—	—

Note 1: Timer1 is a Type A.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

FIGURE 22-8: **OC/PWM MODULE TIMING CHARACTERISTICS**
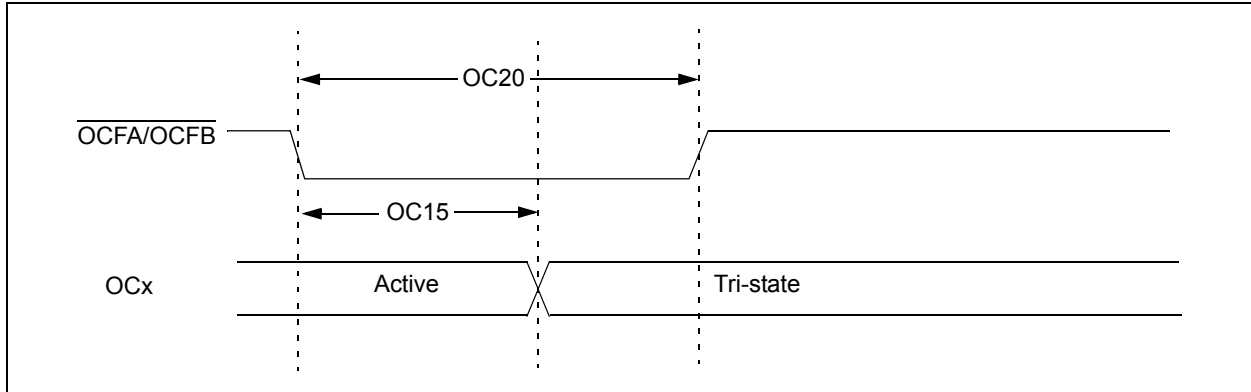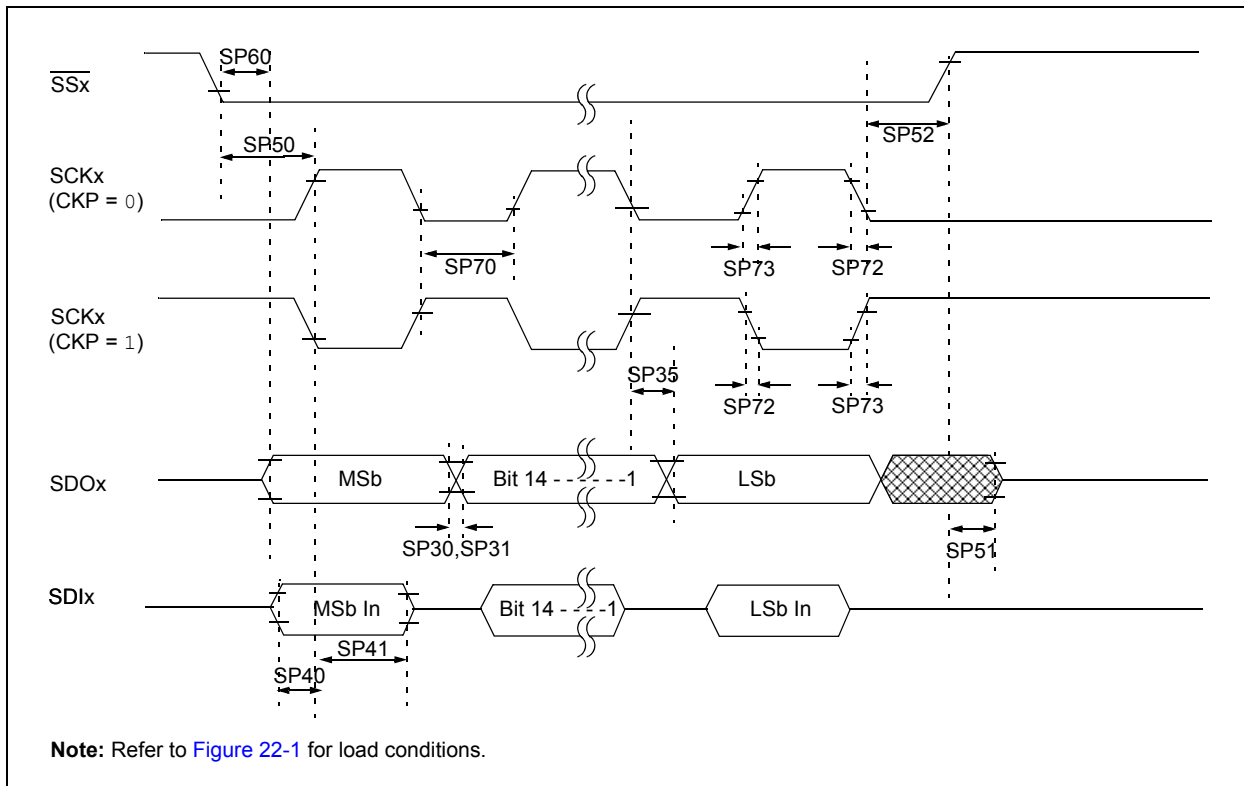

TABLE 22-27: SIMPLE OC/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C $\leq$TA $\leq$+85°C for Industrial -40°C $\leq$TA $\leq$+125°C for Extended				
Param No.	Symbol	Characteristic[1]	Min	Typ	Max	Units	Conditions
OC15	T_{FD}	Fault Input to PWM I/O Change	—	—	T_{CY} + 20	ns	—
OC20	T_{FLT}	Fault Input Pulse-Width	T_{CY} + 20	—	—	ns	—

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 22-13: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

Note: Refer to Figure 22-1 for load conditions.

TABLE 23-10: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+150°C for High Temperature					
Param No.	Symbol	Characteristic[1]	Min	Typ	Max	Units	Conditions
HSP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	10	25	ns	—
HSP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	28	—	—	ns	—
HSP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	35	—	—	ns	—

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 23-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+150°C for High Temperature					
Param No.	Symbol	Characteristic[1]	Min	Typ	Max	Units	Conditions
HSP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	10	25	ns	—
HSP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	35	—	—	ns	—
HSP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	28	—	—	ns	—
HSP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	35	—	—	ns	—

Note 1: These parameters are characterized but not tested in manufacturing.

25.1 Package Marking Information (Continued)

28-Lead QFN-S   Example

```
XXXXXXXX
XXXXXXXX
YYWWNNN
```

```
33FJ32GP
202E/MM (e3)
0730235
```

44-Lead QFN   Example

```
XXXXXXXXXX
XXXXXXXXXX
XXXXXXXXXX
  YYWWNNN
```

```
dsPIC33FJGP
MC204-E/ML (e3)
   0730235
```

44-Lead TQFP   Example

```
MICROCHIP
XXXXXXXXXX
XXXXXXXXXX
XXXXXXXXXX
   YYWWNNN
```

```
MICROCHIP
dsPIC33FJ
32GP204
-E/PT (e3)
   0730235
```
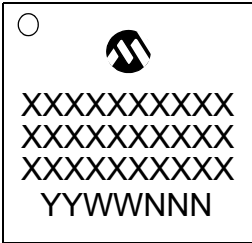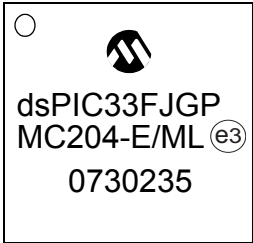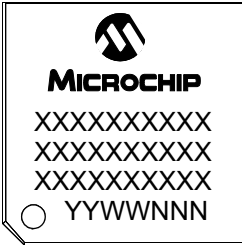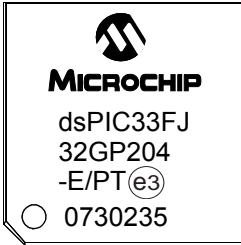
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: If the full Microchip part number cannot be marked on one line, it is carried over to the next line, thus limiting the number of available characters for customer-specific information.

dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

**28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S]
with 0.40 mm Contact Length**
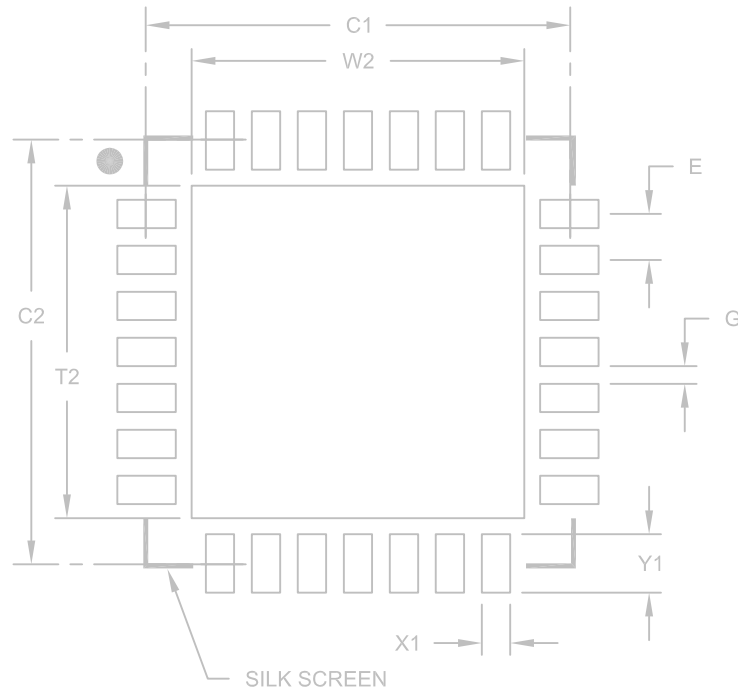
RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.40
Contact Pad Length (X28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A