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Details

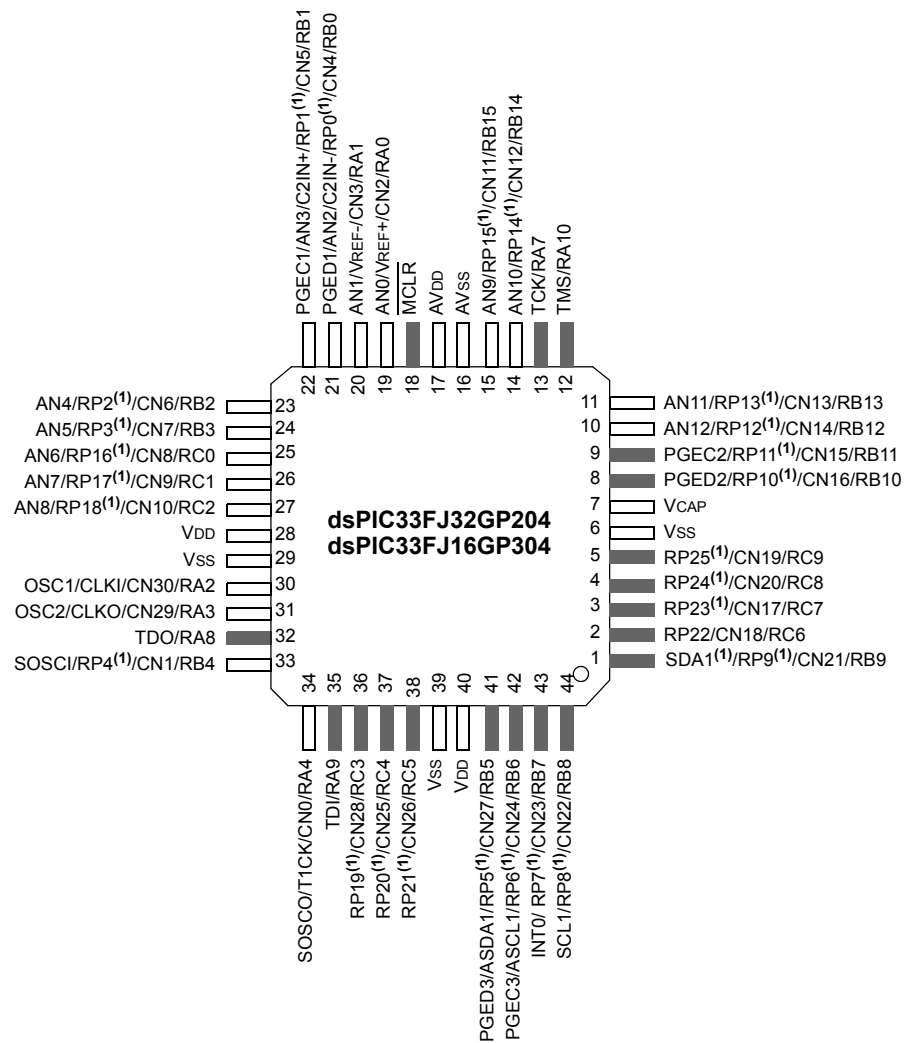
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DCI, DMA, I ² S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj32gp202-e-so

dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

Pin Diagrams (Continued)

44-Pin TQFP

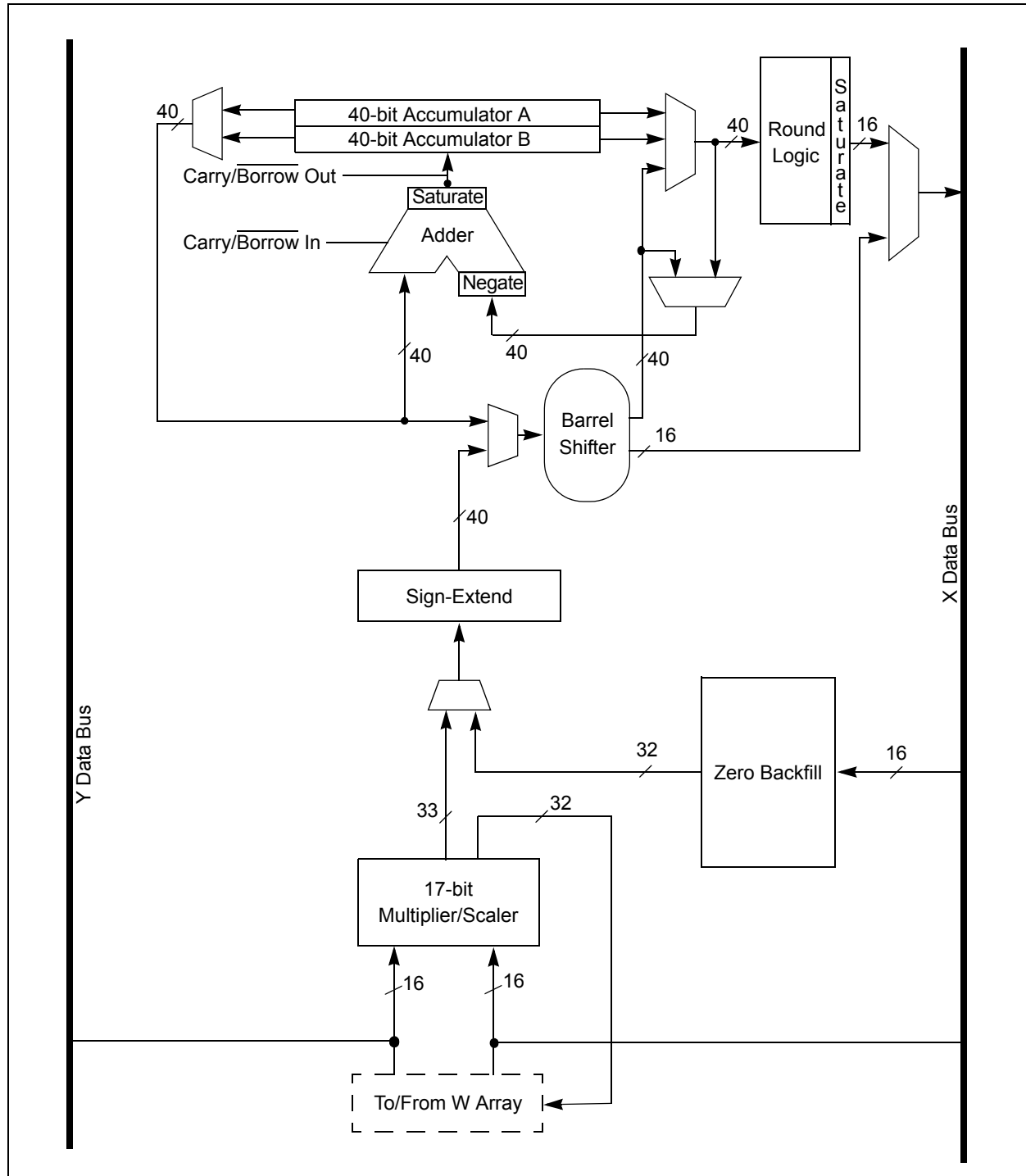
■ = Pins are up to 5V tolerant



Note 1: The RPN pins can be used by any remappable peripheral. See [Table 1](#) for the list of available peripherals.

dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

FIGURE 3-3: DSP ENGINE BLOCK DIAGRAM



dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

FIGURE 4-6: BIT-REVERSED ADDRESS EXAMPLE

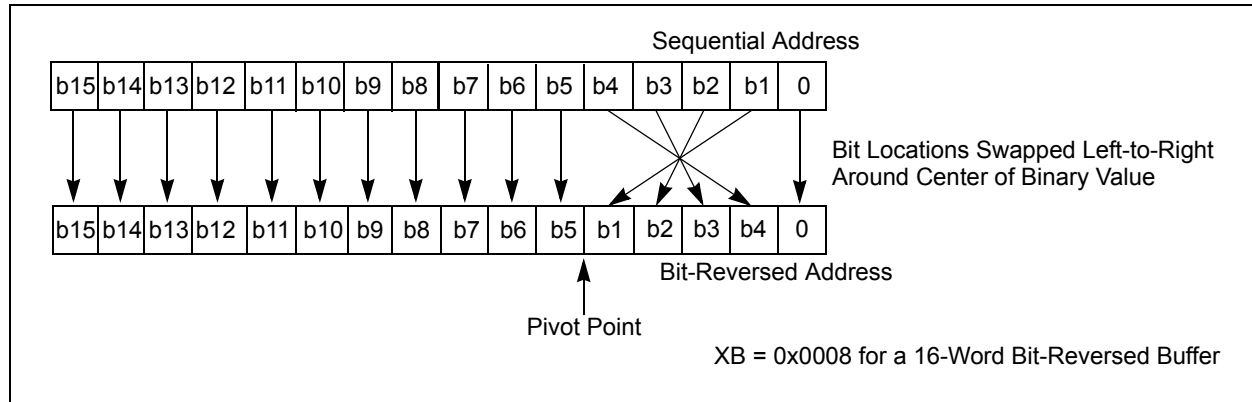


TABLE 4-24: BIT-REVERSED ADDRESS SEQUENCE (16-ENTRY)

Normal Address					Bit-Reversed Address				
A3	A2	A1	A0	Decimal	A3	A2	A1	A0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	8
0	0	1	0	2	0	1	0	0	4
0	0	1	1	3	1	1	0	0	12
0	1	0	0	4	0	0	1	0	2
0	1	0	1	5	1	0	1	0	10
0	1	1	0	6	0	1	1	0	6
0	1	1	1	7	1	1	1	0	14
1	0	0	0	8	0	0	0	1	1
1	0	0	1	9	1	0	0	1	9
1	0	1	0	10	0	1	0	1	5
1	0	1	1	11	1	1	0	1	13
1	1	0	0	12	0	0	1	1	3
1	1	0	1	13	1	0	1	1	11
1	1	1	0	14	0	1	1	1	7
1	1	1	1	15	1	1	1	1	15

dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

4.8.2 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The **TBLRDL** and **TBLWTL** instructions offer a direct method of reading or writing the lower word of any address within the program space without going through data space. The **TBLRDH** and **TBLWTH** instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit wide word address spaces, residing side by side, each with the same address range. **TBLRDL** and **TBLWTL** access the space that contains the least significant data word. **TBLRDH** and **TBLWTH** access the space that contains the upper data byte.

Two table instructions are provided to move byte or word sized (16-bit) data to and from program space. Both function as either byte or word operations.

- **TBLRDL** (Table Read Low): In Word mode, this instruction maps the lower word of the program space location ($P<15:0>$) to a data address ($D<15:0>$).

In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.

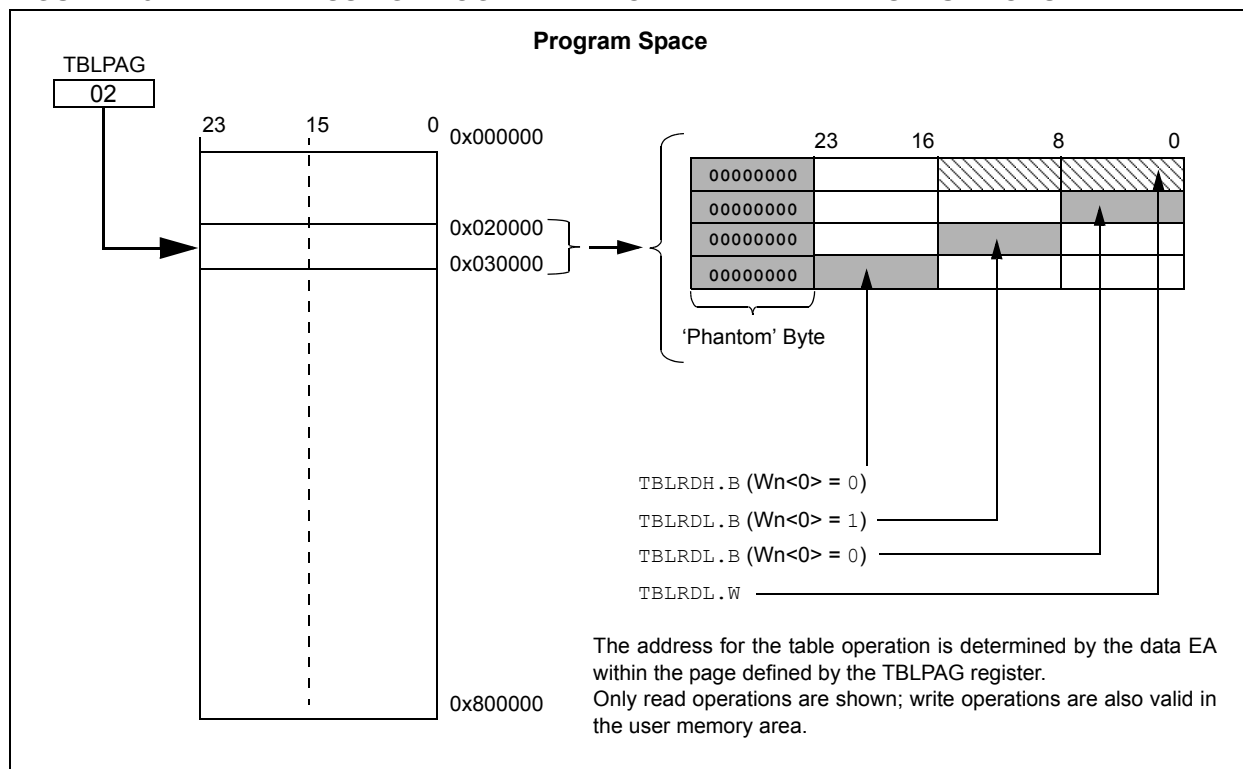
- **TBLRDH** (Table Read High): In Word mode, this instruction maps the entire upper word of a program address ($P<23:16>$) to a data address. Note that $D<15:8>$, the 'phantom byte', will always be '0'.

In Byte mode, this instruction maps the upper or lower byte of the program word to $D<7:0>$ of the data address, as in the **TBLRDL** instruction. Note that the data will always be '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, **TBLWTH** and **TBLWTL**, are used to write individual bytes or words to a program space address. The details of their operation are explained in [Section 5.0 "Flash Program Memory"](#).

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When $TBLPAG<7> = 0$, the table page is located in the user memory space. When $TBLPAG<7> = 1$, the page is located in configuration space.

FIGURE 4-8: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



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REGISTER 5-2: NVMKEY: NONVOLATILE MEMORY KEY REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<7:0>							
bit 7							bit 0

Legend:	SO = Settable Only bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMKEY<7:0>:** Key Register (Write Only) bits

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REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾ (CONTINUED)

bit 2	IDLE: Wake-up from Idle Flag bit 1 = Device was in Idle mode 0 = Device was not in Idle mode
bit 1	BOR: Brown-out Reset Flag bit 1 = A Brown-out Reset has occurred 0 = A Brown-out Reset has not occurred
bit 0	POR: Power-on Reset Flag bit 1 = A Power-on Reset has occurred 0 = A Power-on Reset has not occurred

- Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
- 2:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

7.3 Interrupt Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this [link](#), contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en530331>

7.3.1 KEY RESOURCES

- **Section 6. “Interrupts”** (DS70184)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

7.4 Interrupt Control and Status Registers

dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 devices implement a total of 17 registers for the interrupt controller:

- Interrupt Control Register 1 (INTCON1)
- Interrupt Control Register 2 (INTCON2)
- Interrupt Flag Status Registers (IFSx)
- Interrupt Enable Control Registers (IECx)
- Interrupt Priority Control Registers (IPCx)
- Interrupt Control and Status Register (INTTREG)

7.4.1 INTCON1 AND INTCON2

Global interrupt control functions are controlled from INTCON1 and INTCON2. INTCON1 contains the Interrupt Nesting Disable (NSTDIS) bit as well as the control and status flags for the processor trap sources. The INTCON2 register controls the external interrupt request signal behavior and the use of the Alternate Interrupt Vector Table.

7.4.2 IFSx

The IFS registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

7.4.3 IECx

The IEC registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

7.4.4 IPCx

The IPC registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

7.4.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt priority Level, which are latched into the vector number (VECNUM<6:0>) and Interrupt level bits (ILR<3:0>) in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence that they are listed in [Table 7-1](#). For example, the INT0 (External Interrupt 0) is shown as having vector number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0>, and the INT0IP bits in the first position of IPC0 (IPC0<2:0>).

7.4.6 STATUS REGISTERS

Although they are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality:

- The CPU STATUS register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU Interrupt Priority Level. The user can change the current CPU priority level by writing to the IPL bits.
- The CORCON register contains the IPL3 bit which, together with IPL<2:0>, also indicates the current CPU priority level. IPL3 is a read-only bit, so that trap events cannot be masked by the user software.

All Interrupt bits and registers are described in [Register 7-1](#) through [Register 7-19](#).

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REGISTER 7-1: SR: CPU STATUS REGISTER⁽¹⁾

R-0	R-0	R/C-0	R/C-0	R-0	R/C-0	R-0	R/W-0
OA	OB	SA	SB	OAB	SAB	DA	DC
bit 15						bit 8	

R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2 ⁽²⁾	IPL1 ⁽²⁾	IPL0 ⁽²⁾	RA	N	OV	Z	C
bit 7						bit 0	

Legend:

C = Clear only bit	R = Readable bit	U = Unimplemented bit, read as '0'
S = Set only bit	W = Writable bit	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **IPL<2:0>: CPU Interrupt Priority Level Status bits⁽²⁾**

- 111 = CPU Interrupt Priority Level is 7 (15), user interrupts disabled
- 110 = CPU Interrupt Priority Level is 6 (14)
- 101 = CPU Interrupt Priority Level is 5 (13)
- 100 = CPU Interrupt Priority Level is 4 (12)
- 011 = CPU Interrupt Priority Level is 3 (11)
- 010 = CPU Interrupt Priority Level is 2 (10)
- 001 = CPU Interrupt Priority Level is 1 (9)
- 000 = CPU Interrupt Priority Level is 0 (8)

Note 1: For complete register details, see [Register 3-1](#).

2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.

3: The IPL<2:0> Status bits are read-only when NSTDIS bit (INTCON1<15>) = 1.

REGISTER 7-2: CORCON: CORE CONTROL REGISTER⁽¹⁾

U-0	U-0	U-0	R/W-0	R/W-0	R-0	R-0	R-0
—	—	—	US	EDT	DL<2:0>		
bit 15						bit 8	

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R/W-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3 ⁽²⁾	PSV	RND	IF
bit 7						bit 0	

Legend:

C = Clear only bit	W = Writable bit	-n = Value at POR	'1' = Bit is set
R = Readable bit	'x' = Bit is unknown	U = Unimplemented bit, read as '0'	
'0' = Bit is cleared			

bit 3 **IPL3: CPU Interrupt Priority Level Status bit⁽²⁾**

- 1 = CPU Interrupt Priority Level is greater than 7
- 0 = CPU Interrupt Priority Level is 7 or less

Note 1: For complete register details, see [Register 3-2](#).

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

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10.9 Peripheral Pin Select Registers

The dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 devices implement 17 registers for remappable peripheral configuration:

- Input Remappable Peripheral Registers (9)
- Output Remappable Peripheral Registers (8)

Note: Input and Output Register values can only be changed if OSCCON[IOLOCK] = 0. See [Section 10.6.3.1 “Control Register Lock”](#) for a specific command sequence.

REGISTER 10-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	INT1R<4:0>				
bit 15			bit 8				

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7			bit 0				

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **INT1R<4:0>:** Assign External Interrupt 1 (INTR1) to the corresponding RPn pin

11111 = Input tied to Vss

11001 = Input tied to RP25

•

•

•

00001 = Input tied to RP1

00000 = Input tied to RP0

bit 7-0 **Unimplemented:** Read as '0'

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REGISTER 10-8: RPINR20: PERIPHERAL PIN SELECT INPUT REGISTER 20

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	SCK1R<4:0>				
bit 15							
			bit 8				

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	SDI1R<4:0>				
bit 7							
			bit 0				

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **SCK1R<4:0>:** Assign SPI 1 Clock Input (SCK1IN) to the corresponding RPn pin

11111 = Input tied to Vss

11001 = Input tied to RP25

•
•
•

00001 = Input tied to RP1

00000 = Input tied to RP0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **SDI1R<4:0>:** Assign SPI 1 Data Input (SDI1) to the corresponding RPn pin

11111 = Input tied to Vss

11001 = Input tied to RP25

•
•
•

00001 = Input tied to RP1

00000 = Input tied to RP0

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REGISTER 10-20: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP21R<4:0>				
bit 15							
			bit 8				

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP20R<4:0>				
bit 7							
			bit 0				

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **RP21R<4:0>:** Peripheral Output Function is Assigned to RP21 Output Pin (see [Table 10-2](#) for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP20R<4:0>:** Peripheral Output Function is Assigned to RP20 Output Pin (see [Table 10-2](#) for peripheral function numbers)

REGISTER 10-21: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP23R<4:0>				
bit 15							
			bit 8				

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP22R<4:0>				
bit 7							
			bit 0				

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **RP23R<4:0>:** Peripheral Output Function is Assigned to RP23 Output Pin (see [Table 10-2](#) for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP22R<4:0>:** Peripheral Output Function is Assigned to RP22 Output Pin (see [Table 10-2](#) for peripheral function numbers)

dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

11.0 TIMER1

Note 1: This data sheet summarizes the features of the dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 11. “Timers”** (DS70205) of the *“dsPIC33F/PIC24H Family Reference Manual”*, which is available from the Microchip web site: (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to [Section 4.0 “Memory Organization”](#) in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer, which can serve as the time counter for the real-time clock, or operate as a free-running interval timer/counter. Timer1 can operate in three modes:

- 16-bit Timer
- 16-bit Synchronous Counter
- 16-bit Asynchronous Counter

Timer1 also supports these features:

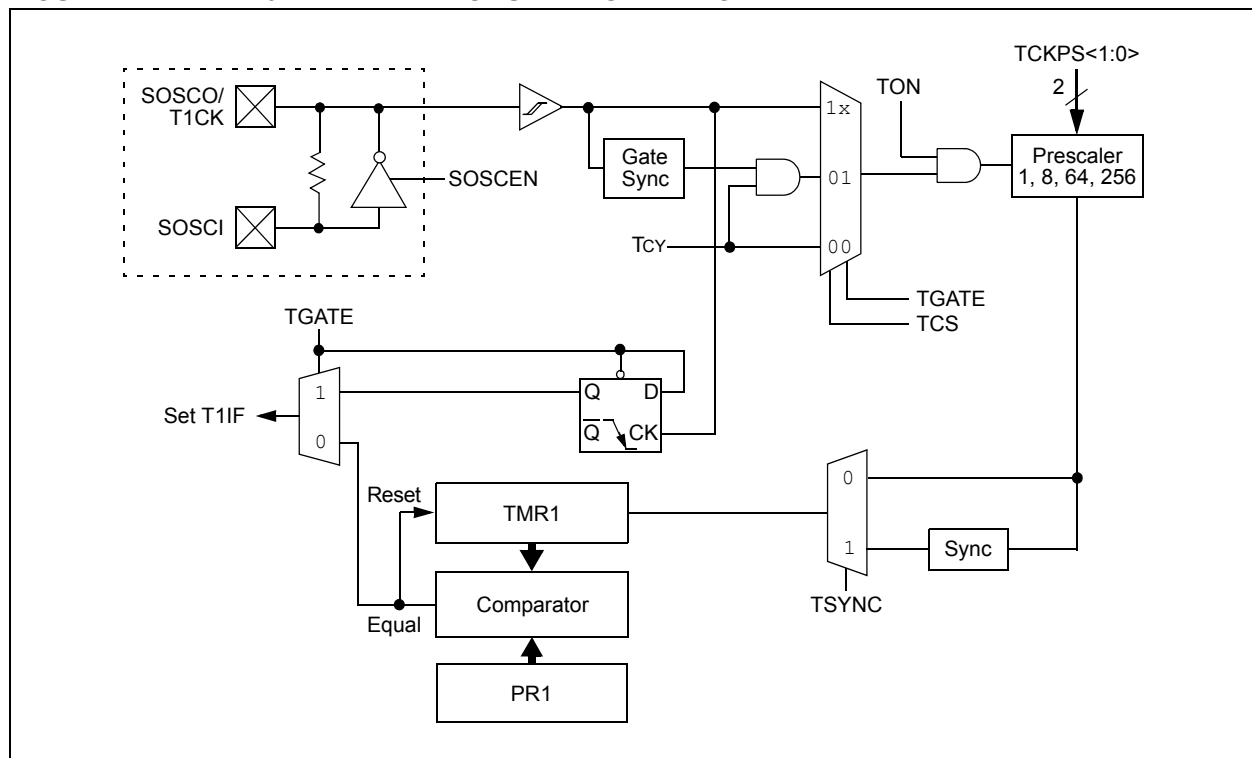
- Timer gate operation
- Selectable prescaler settings
- Timer operation during CPU Idle and Sleep modes
- Interrupt on 16-bit Period register match or falling edge of external gate signal

Figure 11-1 illustrates a block diagram of the 16-bit timer module.

To configure Timer1 for operation:

1. Set the TON bit (= 1) in the T1CON register.
2. Select the timer prescaler ratio using the TCKPS<1:0> bits in the T1CON register.
3. Set the Clock and Gating modes using the TCS and TGATE bits in the T1CON register.
4. Set or clear the TSYNC bit in the T1CON register to select synchronous or asynchronous operation.
5. Load the timer period value into the PR1 register.
6. If interrupts are required, set the interrupt enable bit, T1IE. Use the priority bits, T1IP<2:0>, to set the interrupt priority.

FIGURE 11-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

14.3 Output Compare Register

REGISTER 14-1: OCxCON: OUTPUT COMPARE x CONTROL REGISTER

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	OCSIDL	—	—	—	—	—
bit 15			bit 8				

U-0	U-0	U-0	R-0 HC	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	OCFLT	OCTSEL	OCM<2:0>		
bit 7			bit 0				

Legend:	HC = Cleared in Hardware	HS = Set in Hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **OCSIDL:** Stop Output Compare in Idle Mode Control bit
1 = Output Compare x will halt in CPU Idle mode
0 = Output Compare x will continue to operate in CPU Idle mode
- bit 12-5 **Unimplemented:** Read as '0'
- bit 4 **OCFLT:** PWM Fault Condition Status bit
1 = PWM Fault condition has occurred (cleared in hardware only)
0 = No PWM Fault condition has occurred
(This bit is only used when OCM<2:0> = 111.)
- bit 3 **OCTSEL:** Output Compare Timer Select bit
1 = Timer3 is the clock source for Compare x
0 = Timer2 is the clock source for Compare x
- bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
111 = PWM mode on OCx, Fault pin enabled
110 = PWM mode on OCx, Fault pin disabled
101 = Initialize OCx pin low, generate continuous output pulses on OCx pin
100 = Initialize OCx pin low, generate single output pulse on OCx pin
011 = Compare event toggles OCx pin
010 = Initialize OCx pin high, compare event forces OCx pin low
001 = Initialize OCx pin low, compare event forces OCx pin high
000 = Output compare channel is disabled

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REGISTER 16-1: I2CxCON: I2Cx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-1 HC	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0 HC	R/W-0 HC	R/W-0 HC	R/W-0 HC	R/W-0 HC
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HS = Set in hardware	HC = Cleared in hardware
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **I2CEN:** I2Cx Enable bit
1 = Enables the I2Cx module and configures the SDAx and SCLx pins as serial port pins
0 = Disables the I2Cx module. All I²C pins are controlled by port functions
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **I2CSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters an Idle mode
0 = Continue module operation in Idle mode
- bit 12 **SCLREL:** SCLx Release Control bit (when operating as I²C™ slave)
1 = Release SCLx clock
0 = Hold SCLx clock low (clock stretch)
If STREN = 1:
Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.
If STREN = 0:
Bit is R/S (i.e., software can only write '1' to release clock). Hardware clear at beginning of slave transmission.
- bit 11 **IPMIEN:** Intelligent Peripheral Management Interface (IPMI) Enable bit
1 = IPMI mode is enabled; all addresses Acknowledged
0 = IPMI mode disabled
- bit 10 **A10M:** 10-bit Slave Address bit
1 = I2CxADD is a 10-bit slave address
0 = I2CxADD is a 7-bit slave address
- bit 9 **DISSLW:** Disable Slew Rate Control bit
1 = Slew rate control disabled
0 = Slew rate control enabled
- bit 8 **SMEN:** SMBus Input Levels bit
1 = Enable I/O pin thresholds compliant with SMBus specification
0 = Disable SMBus input thresholds
- bit 7 **GCEN:** General Call Enable bit (when operating as I²C slave)
1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)
0 = General call address disabled
- bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I²C slave)
Used in conjunction with SCLREL bit.
1 = Enable software or receive clock stretching
0 = Disable software or receive clock stretching

dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

17.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note 1: This data sheet summarizes the features of the dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 17. "UART"** (DS70188) of the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available on the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 device family. The UART is a full-duplex asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the UxCTS and UxRTS pins and also includes an IrDA® encoder and decoder.

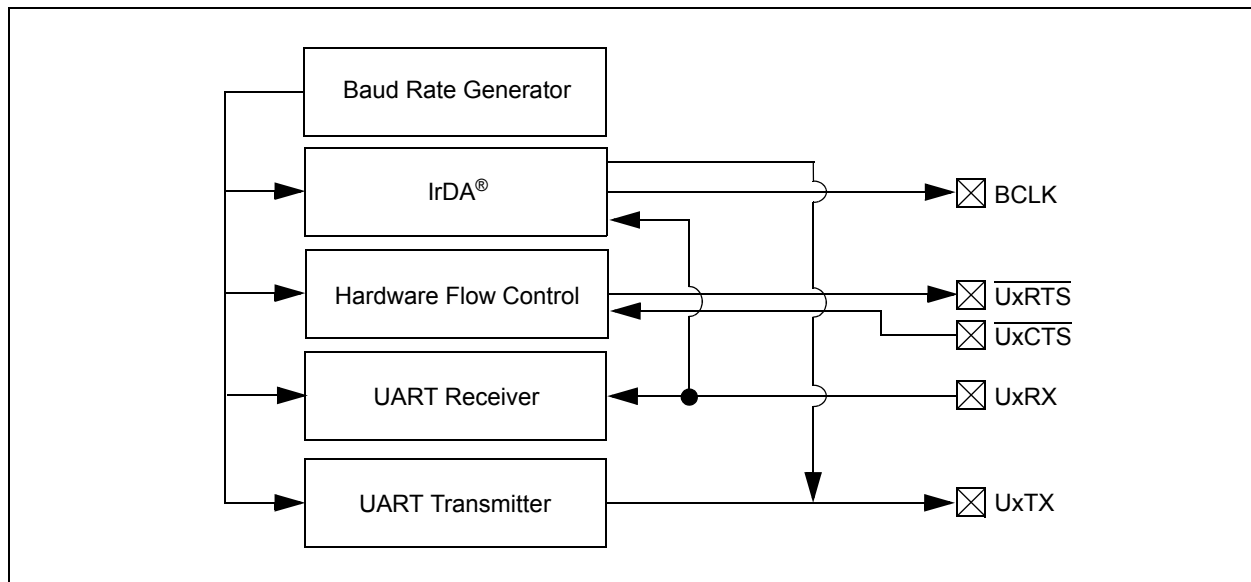
The primary features of the UART module are:

- Full-Duplex, 8-bit or 9-bit Data Transmission through the UxTX and UxRX pins
- Even, odd or no parity options (for 8-bit data)
- One or two stop bits
- Hardware Flow Control Option with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins
- Fully Integrated Baud Rate Generator with 16-bit prescaler
- Baud rates ranging from 10 Mbps to 38 bps at 40 MIPS
- 4-deep first-in-first-out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, framing and buffer overrun error detection
- Support for 9-bit mode with Address Detect (9th bit = 1)
- Transmit and Receive interrupts
- A separate interrupt for all UART error conditions
- Loopback mode for diagnostic support
- Support for Sync and Break characters
- Support for automatic baud rate detection
- IrDA® encoder and decoder logic
- 16x baud clock output for IrDA® support

A simplified block diagram of the UART module is shown in [Figure 17-1](#). The UART module consists of these key hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

FIGURE 17-1: UART SIMPLIFIED BLOCK DIAGRAM



dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

REGISTER 18-4: AD1CHS123: ADC1 INPUT CHANNEL 1, 2, 3 SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	CH123NB<1:0>		CH123SB
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	CH123NA<1:0>		CH123SA
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-9 **CH123NB<1:0>:** Channel 1, 2, 3 Negative Input Select for Sample B bits

dsPIC33FJ32GP202 devices only:

If AD12B = 1:

11 = Reserved

10 = Reserved

01 = Reserved

00 = Reserved

If AD12B = 0:

11 = CH1 negative input is AN9, CH2 negative input is AN10, CH3 negative input is AN11

10 = Reserved

01 = CH1, CH2, CH3 negative input is VREF-

00 = CH1, CH2, CH3 negative input is VREF-

dsPIC33FJ32GP204 and dsPIC33FJ16GP304 devices only:

If AD12B = 1:

11 = Reserved

10 = Reserved

01 = Reserved

00 = Reserved

If AD12B = 0:

11 = CH1 negative input is AN9, CH2 negative input is AN10, CH3 negative input is AN11

10 = CH1 negative input is AN6, CH2 negative input is AN7, CH3 negative input is AN8

01 = CH1, CH2, CH3 negative input is VREF-

00 = CH1, CH2, CH3 negative input is VREF-

bit 8 **CH123SB:** Channel 1, 2, 3 Positive Input Select for Sample B bit

If AD12B = 1:

1 = Reserved

0 = Reserved

If AD12B = 0:

1 = CH1 positive input is AN3, CH2 positive input is AN4, CH3 positive input is AN5

0 = CH1 positive input is AN0, CH2 positive input is AN1, CH3 positive input is AN2

bit 7-3 **Unimplemented:** Read as '0'

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TABLE 20-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
10	BTSC	BTSC $f, \#bit4$	Bit Test f , Skip if Clear	1	1 (2 or 3)	None
		BTSC $Ws, \#bit4$	Bit Test Ws , Skip if Clear	1	1 (2 or 3)	None
11	BTSS	BTSS $f, \#bit4$	Bit Test f , Skip if Set	1	1 (2 or 3)	None
		BTSS $Ws, \#bit4$	Bit Test Ws , Skip if Set	1	1 (2 or 3)	None
12	BTST	BTST $f, \#bit4$	Bit Test f	1	1	Z
		BTST.C $Ws, \#bit4$	Bit Test Ws to C	1	1	C
		BTST.Z $Ws, \#bit4$	Bit Test Ws to Z	1	1	Z
		BTST.C Ws, Wb	Bit Test $Ws < Wb >$ to C	1	1	C
		BTST.Z Ws, Wb	Bit Test $Ws < Wb >$ to Z	1	1	Z
13	BTSTS	BTSTS $f, \#bit4$	Bit Test then Set f	1	1	Z
		BTSTS.C $Ws, \#bit4$	Bit Test Ws to C, then Set	1	1	C
		BTSTS.Z $Ws, \#bit4$	Bit Test Ws to Z, then Set	1	1	Z
14	CALL	CALL $lit23$	Call subroutine	2	2	None
		CALL Wn	Call indirect subroutine	1	2	None
15	CLR	CLR f	$f = 0x0000$	1	1	None
		CLR $WREG$	$WREG = 0x0000$	1	1	None
		CLR Ws	$Ws = 0x0000$	1	1	None
		CLR $Acc, Wx, Wxd, Wy, Wyd, AWB$	Clear Accumulator	1	1	OA,OB,SA,SB
16	CLRWDT	CLRWDT	Clear Watchdog Timer	1	1	WDTO,Sleep
17	COM	COM f	$f = \bar{f}$	1	1	N,Z
		COM $f, WREG$	$WREG = \bar{f}$	1	1	N,Z
		COM Ws, Wd	$Wd = \bar{Ws}$	1	1	N,Z
18	CP	CP f	Compare f with $WREG$	1	1	C,DC,N,OV,Z
		CP $Wb, \#lit5$	Compare Wb with $lit5$	1	1	C,DC,N,OV,Z
		CP Wb, Ws	Compare Wb with Ws ($Wb - Ws$)	1	1	C,DC,N,OV,Z
19	CP0	CP0 f	Compare f with $0x0000$	1	1	C,DC,N,OV,Z
		CP0 Ws	Compare Ws with $0x0000$	1	1	C,DC,N,OV,Z
20	CPB	CPB f	Compare f with $WREG$, with Borrow	1	1	C,DC,N,OV,Z
		CPB $Wb, \#lit5$	Compare Wb with $lit5$, with Borrow	1	1	C,DC,N,OV,Z
		CPB Wb, Ws	Compare Wb with Ws , with Borrow ($Wb - Ws - C$)	1	1	C,DC,N,OV,Z
21	CPSEQ	CPSEQ Wb, Wn	Compare Wb with Wn , skip if =	1	1 (2 or 3)	None
22	CPSGT	CPSGT Wb, Wn	Compare Wb with Wn , skip if >	1	1 (2 or 3)	None
23	CPSLT	CPSLT Wb, Wn	Compare Wb with Wn , skip if <	1	1 (2 or 3)	None
24	CPSNE	CPSNE Wb, Wn	Compare Wb with Wn , skip if \neq	1	1 (2 or 3)	None
25	DAW	DAW Wn	$Wn = \text{decimal adjust } Wn$	1	1	C
26	DEC	DEC f	$f = f - 1$	1	1	C,DC,N,OV,Z
		DEC $f, WREG$	$WREG = f - 1$	1	1	C,DC,N,OV,Z
		DEC Ws, Wd	$Wd = Ws - 1$	1	1	C,DC,N,OV,Z
27	DEC2	DEC2 f	$f = f - 2$	1	1	C,DC,N,OV,Z
		DEC2 $f, WREG$	$WREG = f - 2$	1	1	C,DC,N,OV,Z
		DEC2 Ws, Wd	$Wd = Ws - 2$	1	1	C,DC,N,OV,Z
28	DISI	DISI $\#lit14$	Disable Interrupts for k instruction cycles	1	1	None

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TABLE 22-17: PLL CLOCK TIMING SPECIFICATIONS (VDD = 3.0V TO 3.6V)

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
OS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range ⁽²⁾	0.8	—	8	MHz	ECPLL, XTPLL modes
OS51	FSYS	On-Chip VCO System Frequency ⁽³⁾	100	—	200	MHz	—
OS52	TLOCK	PLL Start-up Time (Lock Time) ⁽³⁾	0.9	1.5	3.1	ms	—
OS53	DCLK	CLKO Stability (Jitter) ⁽³⁾	-3	0.5	3	%	Measured over 100 ms period

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

2: These parameters are characterized by similarity, but are tested in manufacturing at 7.7 MHz input only.

3: These parameters are characterized by similarity, but are not tested in manufacturing. This specification is based on clock cycle by clock cycle measurements. To calculate the effective jitter for individual time bases or communication clocks use this formula:

$$\text{Peripheral Clock Jitter} = \frac{DCLK}{\sqrt{\left(\frac{FOSC}{\text{Peripheral Bit Rate Clock}}\right)}}$$

For example: Fosc = 32 MHz, DCLK = 3%, SPI bit rate clock, (i.e., SCK) is 2 MHz.

$$\text{SPI SCK Jitter} = \left[\frac{DCLK}{\sqrt{\left(\frac{32 \text{ MHz}}{2 \text{ MHz}}\right)}} \right] = \left[\frac{3\%}{\sqrt{16}} \right] = \left[\frac{3\%}{4} \right] = 0.75\%$$

TABLE 22-18: AC CHARACTERISTICS: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for industrial -40°C ≤TA ≤+125°C for Extended					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
	Internal FRC Accuracy @ FRC Frequency = 7.37 MHz ⁽¹⁾						
F20a	FRC	-2	—	+2	%	-40°C ≤TA ≤+85°C	VDD = 3.0-3.6V
F20b	FRC	-5	—	+5	%	-40°C ≤TA ≤+125°C	VDD = 3.0-3.6V

Note 1: Frequency calibrated at 25°C and 3.3V. TUN bits can be used to compensate for temperature drift.

TABLE 22-19: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
	LPRC @ 32.768 kHz ^(1,2)						
F21a	LPRC	-15	±6	+15	%	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$	VDD = 3.0-3.6V
F21b	LPRC	-40	—	+40	%	$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	VDD = 3.0-3.6V

Note 1: Change of LPRC frequency as VDD changes.

2: LPRC impacts the Watchdog Timer Time-out Period (TWDT1). See [Section 19.4 “Watchdog Timer \(WDT\)”](#) for more information.

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FIGURE 22-5: TIMER1, 2 AND 3 EXTERNAL CLOCK TIMING CHARACTERISTICS

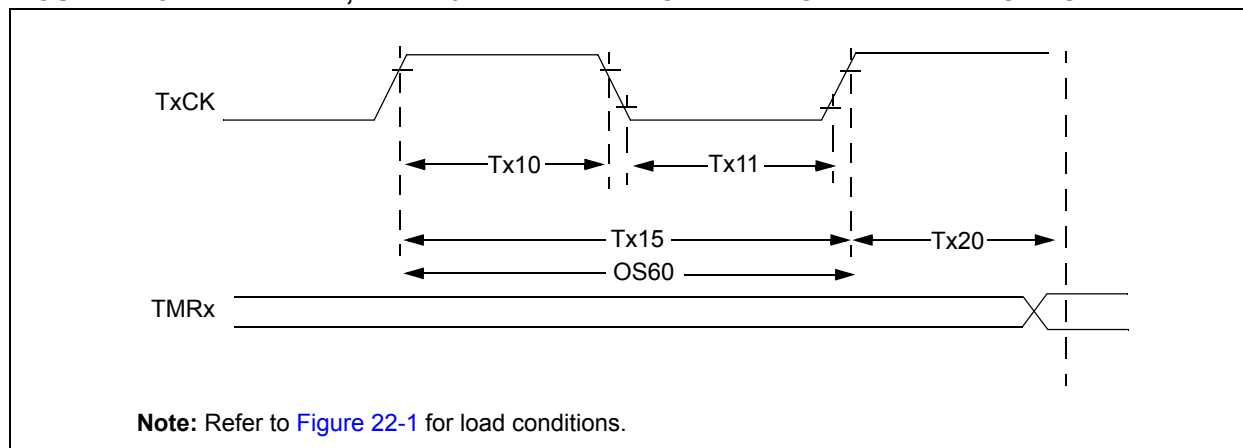


TABLE 22-22: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS⁽¹⁾

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽²⁾		Min	Typ	Max	Units	Conditions
TA10	T _{TXH}	TxCK High Time	Synchronous, no prescaler	0.5 T _{CY} + 20	—	—	ns	Must also meet parameter TA15
			Synchronous, with prescaler	10	—	—	ns	
			Asynchronous	10	—	—	ns	
TA11	T _{TXL}	TxCK Low Time	Synchronous, no prescaler	0.5 T _{CY} + 20	—	—	ns	Must also meet parameter TA15
			Synchronous, with prescaler	10	—	—	ns	
			Asynchronous	10	—	—	ns	
TA15	T _{TXP}	TxCK Input Period	Synchronous, no prescaler	T _{CY} + 40	—	—	ns	—
			Synchronous, with prescaler	Greater of: 20 ns or (T _{CY} + 40)/N	—	—	—	N = prescale value (1, 8, 64, 256)
			Asynchronous	20	—	—	ns	—
OS60	F _{t1}	SOSC1/T1CK Oscillator Input frequency Range (oscillator enabled by setting bit TCS (T1CON<1>))		DC	—	50	kHz	—
TA20	T _{CKEXTMRL}	Delay from External TxCK Clock Edge to Timer Increment		0.5 T _{CY}	—	1.5 T _{CY}	—	—

Note 1: Timer1 is a Type A.

Note 2: These parameters are characterized by similarity, but are not tested in manufacturing.

dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

Revision H (July 2011)

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in the following table.

TABLE A-7: MAJOR SECTION UPDATES

Section Name	Update Description
Section 19.0 “Special Features”	Added Note 3 to the Connections for the On-chip Voltage Regulator diagram (see Figure 19-1).
Section 22.0 “Electrical Characteristics”	Removed Note 3 and parameter DC10 (V _{CORE}) from the DC Temperature and Voltage Specifications (see Table 22-4). Updated the Characteristics definition and Conditions for parameter BO10 in the Electrical Characteristics: BOR (see Table 22-11). Added Note 1 to the Internal Voltage Regulator Specifications (see Table 22-13).

Revision J (June 2012)

This revision includes typographical and formatting changes throughout the data sheet text.

In addition, where applicable, new sections were added to each peripheral chapter that provide information and links to related resources, as well as helpful tips. For examples, see [Section 8.2 “Oscillator Resources”](#) and [Section 18.3 “ADC Helpful Tips”](#).

All other major changes are referenced by their respective section in the following table.

TABLE A-8: MAJOR SECTION UPDATES

Section Name	Update Description
Section 22.0 “Electrical Characteristics”	Added Note 1 to the Operating MIPS vs. Voltage (see Table 22-1). Updated the notes in the following tables: <ul style="list-style-type: none">• Operating Current (I_{DD}) (see Table 22-5)• Idle Current (I_{IDLE}) (see Table 22-6)• Power-Down Current (I_{PD}) (see Table 22-7)• Doze Current (I_{DOZE}) (see Table 22-8) Updated the conditions for Program Memory parameters D136b, D137b, and D138b (T _A = +150°C) (see Table 22-12).
Section 23.0 “High Temperature Electrical Characteristics”	Removed Table 23-8: DC Characteristics: Program Memory.
Section 24.0 “DC and AC Device Characteristics Graphs”	Added new chapter.