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Details

E·XFI

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DCI, DMA, I ² S, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 13x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj32gp204-e-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.4 CPU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access
	the product page using the link above,
	enter this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en530331

3.4.1 KEY RESOURCES

- Section 2. "CPU" (DS70204)
- Code Samples
- Application Notes
- Software Libraries
- · Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

3.6 Arithmetic Logic Unit (ALU)

The dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

The dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit-divisor division.

Refer to the "*dsPIC30F/33F Programmer's Reference Manual*" (DS70157) for information on the SR bits affected by each instruction.

3.6.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier of the DSP engine, the ALU supports unsigned, signed or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- · 8-bit unsigned x 8-bit unsigned

3.6.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. 16-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m+1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.7 DSP Engine

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a barrel shifter and a 40-bit adder/subtracter (with two target accumulators, round and saturation logic).

The dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 is a single-cycle instruction flow architecture; therefore, concurrent operation of the DSP engine with MCU instruction flow is not possible. However, some MCU ALU and DSP engine resources can be used concurrently by the same instruction (e.g., ED, EDAC).

The DSP engine can also perform accumulator-to-accumulator operations that require no additional data. These instructions are ADD, SUB and NEG.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or integer DSP multiply (IF)
- Signed or unsigned DSP multiply (US)
- Conventional or convergent rounding (RND)
- Automatic saturation on/off for AccA (SATA), AccB (SATB) and writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACC-SAT)

A block diagram of the DSP engine is shown in Figure 3-3.

TABLE 3-1: DSP INSTRUCTIONS SUMMARY

Instruction	Algebraic Operation	ACC Write Back
CLR	A = 0	Yes
ED	$A = (x - y)^2$	No
EDAC	$A = A + (x - y)^2$	No
MAC	A = A + (x * y)	Yes
MAC	$A = A + x^2$	No
MOVSAC	No change in A	Yes
MPY	$A = x \bullet y$	No
MPY	$A = x^2$	No
MPY.N	$A = -x \bullet y$	No
MSC	$A = A - x \bullet y$	Yes

4.2 Data Address Space

The dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 CPU has a separate 16-bit wide data memory space. The data space is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory maps is shown in Figure 4-3.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the data space. This arrangement gives a data space address range of 64 Kbytes or 32K words. The lower half of the data memory space (that is, when EA<15> = 0) is used for implemented memory addresses, while the upper half (EA<15> = 1) is reserved for the Program Space Visibility area (see Section 4.8.3 "Reading Data from Program Memory Using Program Space Visibility").

dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 devices implement up to 2 Kbytes of data memory. Should an EA point to a location outside of this area, an all-zero word or byte will be returned.

4.2.1 DATA SPACE WIDTH

The data memory space is organized in byte addressable, 16-bit wide blocks. Data is aligned in data memory and registers as 16-bit words, but all data space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC[®] MCU devices and improve data space memory usage efficiency, the dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 instruction set supports both word and byte operations. As a consequence of byte accessibility, all effective address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] will result in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

Data byte reads will read the complete word that contains the byte, using the LSB of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel byte-wide entities with shared (word) address decode but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address. All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the instruction occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the Least Significant Byte. The Most Significant Byte is not modified.

A sign-extend instruction (SE) is provided to allow users to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a zero-extend (ZE) instruction on the appropriate address.

4.2.3 SFR SPACE

The first 2 Kbytes of the Near Data Space, from 0x0000 to 0x07FF, is primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control, and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'. A complete listing of implemented SFRs, including their addresses, is shown in Table 4-1 through Table 4-22.

Note:	The actual set of peripheral features and											
	interrupts varies by the device. Refer to											
	the corresponding device tables and											
	pinout diagrams for device-specific											
	information.											

4.2.4 NEAR DATA SPACE

The 8 Kbyte area between 0x0000 and 0x1FFF is referred to as the Near Data Space. Locations in this space are directly addressable via a 13-bit absolute address field within all memory direct instructions. Additionally, the whole data space is addressable using MOV instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a working register as an address pointer.

4.4 Special Function Register Maps

TABLE 4-1: CPU CORE REGISTERS MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
WREG0	0000								Working Re	egister 0								0000
WREG1	0002								Working Re	egister 1								0000
WREG2	0004								Working Re	egister 2								0000
WREG3	0006								Working Re	egister 3								0000
WREG4	0008								Working Re	egister 4								0000
WREG5	000A								Working Re	egister 5								0000
WREG6	000C								Working Re	egister 6								0000
WREG7	000E								Working Re	egister 7								0000
WREG8	0010								Working Re	egister 8								0000
WREG9	0012								Working Re	egister 9								0000
WREG10	0014								Working Re	gister 10								0000
WREG11	0016								Working Re	gister 11								0000
WREG12	0018								Working Re	gister 12								0000
WREG13	001A								Working Re	gister 13								0000
WREG14	001C								Working Re	gister 14								0000
WREG15	001E								Working Re	gister 15								0800
SPLIM	0020							Sta	ck Pointer Li	mit Registe	r							XXXX
ACCAL	0022							Accum	ulator A Lov	/ Word Regi	ster							0000
ACCAH	0024							Accum	ulator A Higl	n Word Reg	ister							0000
ACCAU	0026							Accumu	ulator A Uppe	er Word Reg	gister							0000
ACCBL	0028							Accum	ulator B Lov	/ Word Regi	ster							0000
ACCBH	002A							Accum	ulator B Higl	n Word Reg	ister							0000
ACCBU	002C							Accumu	ulator B Uppe	er Word Reg	gister							0000
PCL	002E							Program	n Counter Lo	w Word Re	gister							0000
PCH	0030	_	—	—	—	—	—	—	—			Progra	m Counter	High Byte F	Register			0000
TBLPAG	0032	—	_	—	_	—	—	—	—			Table F	Page Addre	ss Pointer F	Register			0000
PSVPAG	0034	_	—	_		_	—	—	—		Progr	am Memory	/ Visibility P	age Addres	s Pointer R	legister		0000
RCOUNT	0036							Repe	eat Loop Cou	unter Regist	er							XXXX
DCOUNT	0038								DCOUNT	<15:0>								XXXX
DOSTARTL	003A		DOSTARTL<15:1> 0 xxxx										XXXX					
DOSTARTH	003C										00xx							
DOENDL	003E							DO	ENDL<15:1	>							0	XXXX
DOENDH	0040			_	_	—	_			_	_			DOE	NDH			00xx
SR	0042	OA	OB	SA	SB	OAB	SAB	DA	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	С	0000
CORCON	0044	_	_	_	US	EDT		DL<2:0>		SATA	SATB	SATDW	ACCSAT	IPL3	PSV	RND	IF	0020

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Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-11: PERIPHERAL PIN SELECT INPUT REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	0680		_	—			INT1R<4:0>	>		_	—	_	—	—	_			1F00
RPINR1	0682		_	_	_					_	—	_			INT2R<4:0>	>		001F
RPINR3	0686		_	_		T3CKR<4:0>				_	_	_		-	T2CKR<4:0	>		1F1F
RPINR7	068E	_	_	_		IC2R<4:0>				_	_	_	IC1R<4:0>					1F1F
RPINR10	0694	_	_	_			IC8R<4:0>			_	_	_	IC7R<4:0>			1F1F		
RPINR11	0696		_	_	_	_	_	_		_	_	_	OCFAR<4:0>			001F		
RPINR18	06A4		_	_		U1CTSR<4:0>			_	—	_	U1RX <r4:0></r4:0>				1F1F		
RPINR20	06A8		_	—		SCK1R<4:0>				—	—	_	SDI1R<4:0>			1F1F		
RPINR21	06AA	_	_	_	_	_	_	_	_	_	_	_			SS1R<4:0>			001F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-12: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dspic33FJ32GP202

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	06C0	—	_	—		RP1R<4:0>				_	—	_	RP0R<4:0>					0000
RPOR1	06C2	_	_	_		RP3R<4:0>				-	_	_	RP2R<4:0>				0000	
RPOR2	06C4	_	_	_		RP5R<4:0>				_	_	_	RP4R<4:0>				0000	
RPOR3	06C6	_	_	_			RP7R<4:0>			_	_	_		RP6R<4:0>				0000
RPOR4	06C8	_	_	_			RP9R<4:0>			_	_	_			RP8R<4:0>	•		0000
RPOR5	06CA	—	_	_		RP11R<4:0>			_	_	_	RP10R<4:0>				0000		
RPOR6	06CC	_	_	_					_	_	_	RP12R<4:0>				0000		
RPOR7	06CE	_	_	_		RP15R<4:0> — — — RP14R<4:0>						0000						

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.6 Modulo Addressing

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either data or program space (since the data pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into program space) and Y data spaces. Modulo Addressing can operate on any W register pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction, as there are certain restrictions on the buffer start address (for incrementing buffers), or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

4.6.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

Note:	Υ	space	ace Modulo		Addressing			
	calculations		assume	word	sized	data		
	(LS	lear).						

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

4.6.2 W ADDRESS REGISTER SELECTION

The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that will operate with Modulo Addressing:

- If XWM = 15, X RAGU and X WAGU Modulo Addressing is disabled.
- If YWM = 15, Y AGU Modulo Addressing is disabled.

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X data space when XWM is set to any value other than '15' and the XMODEN bit is set at MODCON<15>.

The Y Address Space Pointer W register (YWM) to which Modulo Addressing is to be applied is stored in MODCON<7:4>. Modulo Addressing is enabled for Y data space when YWM is set to any value other than '15' and the YMODEN bit is set at MODCON<14>.

FIGURE 4-5: MODULO ADDRESSING OPERATION EXAMPLE



5.2 RTSP Operation

The dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user application to erase a page of memory, which consists of eight rows (512 instructions) at a time, and to program one row or one word at a time. The 8-row erase pages and single row write rows are edge-aligned from the beginning of program memory, on boundaries of 1536 bytes and 192 bytes, respectively.

The program memory implements holding buffers that can contain 64 instructions of programming data. Prior to the actual programming operation, the write data must be loaded into the buffers sequentially. The instruction words loaded must always be from a group of 64 boundary.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of TBLWT instructions to load the buffers. Programming is performed by setting the control bits in the NVMCON register. A total of 64 TBLWTL and TBLWTH instructions are required to load the instructions.

All of the table write operations are single-word writes (two instruction cycles) because only the buffers are written. A programming cycle is required for programming each row.

5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

The programming time depends on the FRC accuracy (see Table 22-18) and the value of the FRC Oscillator Tuning register (see Register 8-4). Use the following formula to calculate the minimum and maximum values for the Row Write Time, Page Erase Time, and Word Write Cycle Time parameters (see Table 22-12).

EQUATION 5-1: PROGRAMMING TIME



For example, if the device is operating at +125°C, the FRC accuracy will be $\pm 5\%$. If the TUN<5:0> bits (see Register 8-4) are set to `b111111, the minimum row write time is equal to Equation 5-2.

EQUATION 5-2: MINIMUM ROW WRITE TIME

$$T_{RW} = \frac{11064 \ Cycles}{7.37 \ MHz \times (1 + 0.05) \times (1 - 0.00375)} = 1.435 ms$$

The maximum row write time is equal to Equation 5-3.

EQUATION 5-3: MAXIMUM ROW WRITE TIME

$$T_{RW} = \frac{11064 \ Cycles}{7.37 \ MHz \times (1 - 0.05) \times (1 - 0.00375)} = 1.586 ms$$

Setting the WR bit (NVMCON<15>) starts the operation, and the WR bit is automatically cleared when the operation is finished.

5.4 Flash Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en530331

5.4.1 KEY RESOURCES

- Section 5. "Flash Programming" (DS70191)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

5.5 Control Registers

The two SFRs that are used to read and write the program Flash memory are:

NVMCON: Flash Memory Control Register

NVMKEY: Nonvolatile Memory Key Register

The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

NVMKEY (Register 5-2) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register. Refer to **Section 5.3** "**Programming Operations**" for further details.

6.9 Configuration Mismatch Reset

To maintain the integrity of the Peripheral Pin Select control registers, they are constantly monitored with shadow registers in hardware. If an unexpected change in any of the registers occur (such as cell disturbances caused by ESD or other external events), a Configuration Mismatch Reset occurs.

The Configuration Mismatch Flag bit (CM) in the Reset Control register (RCON<9>) is set to indicate the Configuration Mismatch Reset. Refer to **Section 10.0 "I/O Ports"** for more information on the Configuration Mismatch Reset.

Note: The Configuration Mismatch Reset feature and associated Reset flag are not available on all devices.

6.10 Illegal Condition Device Reset

An illegal condition device Reset occurs due to the following sources:

- Illegal Opcode Reset
- Uninitialized W Register Reset
- Security Reset

The Illegal Opcode or Uninitialized W Access Reset Flag bit (IOPUWR) in the Reset Control register (RCON<14>) is set to indicate the illegal condition device Reset.

6.10.1 ILLEGAL OPCODE RESET

A device Reset is generated if the device attempts to execute an illegal opcode value that is fetched from program memory.

The illegal opcode Reset function can prevent the device from executing program memory sections that are used to store constant data. To take advantage of the illegal opcode Reset, use only the lower 16 bits of

each program memory section to store the data values. The upper 8 bits should be programmed with 3Fh, which is an illegal opcode value.

6.10.2 UNINITIALIZED W REGISTER RESET

Any attempts to use the uninitialized W register as an address pointer will Reset the device. The W register array (with the exception of W15) is cleared during all resets and is considered uninitialized until written to.

6.10.3 SECURITY RESET

If a Program Flow Change (PFC) or Vector Flow Change (VFC) targets a restricted location in a protected segment (Boot and Secure Segment), that operation will cause a security Reset.

The PFC occurs when the Program Counter is reloaded as a result of a Call, Jump, Computed Jump, Return, Return from Subroutine, or other form of branch instruction.

The VFC occurs when the Program Counter is reloaded with an Interrupt or Trap vector.

Refer to Section 19.6 "Code Protection and CodeGuard™ Security" for more information on Security Reset.

6.11 Using the RCON Status Bits

The user application can read the Reset Control register (RCON) after any device Reset to determine the cause of the reset.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

Table 6-3 provides a summary of the reset flag bit operation.

Flag Bit	Set by:	Cleared by:
TRAPR (RCON<15>)	Trap conflict event	POR,BOR
IOPWR (RCON<14>)	Illegal opcode or uninitialized W register access or Security Reset	POR,BOR
CM (RCON<9>)	Configuration Mismatch	POR,BOR
EXTR (RCON<7>)	MCLR Reset	POR
SWR (RCON<6>)	RESET instruction	POR,BOR
WDTO (RCON<4>)	WDT time-out	PWRSAV instruction, CLRWDT instruction, POR,BOR
SLEEP (RCON<3>)	PWRSAV #SLEEP instruction	POR,BOR
IDLE (RCON<2>)	PWRSAV #IDLE instruction	POR,BOR
BOR (RCON<1>)	POR, BOR	—
POR (RCON<0>)	POR	—

Note: All Reset flag bits can be set or cleared by user software.

TABLE 6-3: RESET FLAG BIT OPERATION

9.0 POWER-SAVING FEATURES

- **Note 1:** This data sheet summarizes the features of the dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 9. "Watchdog Timer and Power-Saving Modes" (DS70196) of the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power. dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 devices can manage power consumption in four different ways:

- Clock frequency
- Instruction-based Sleep and Idle modes
- · Software-controlled Doze mode
- Selective peripheral control in software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

9.1 Clock Frequency and Clock Switching

dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSC bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in Section 8.0 "Oscillator Configuration".

9.2 Instruction-Based Power-Saving Modes

dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The Assembler syntax of the PWRSAV instruction is shown in Example 9-1.

Note: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to wake-up.

9.2.1 SLEEP MODE

The following occur in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals may continue to operate. This includes items such as the input change notification on the I/O ports, or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device will wake-up from Sleep mode on any of the these events:

- Any interrupt source that is individually enabled
- · Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

EXAMPLE 9-1: PWRSAV INSTRUCTION SYNTAX

PWRSAV #SLEEP_MODE ; Put the device into SLEEP mode
PWRSAV #IDLE_MODE ; Put the device into IDLE mode

10.9 Peripheral Pin Select Registers

The dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 devices implement 17 registers for remappable peripheral configuration:

- Input Remappable Peripheral Registers (9)
- Output Remappable Peripheral Registers (8)

Note:	Input and Output Register values can only
	be changed if OSCCON[IOLOCK] = 0.
	See Section 10.6.3.1 "Control Register
	Lock" for a specific command sequence.

REGISTER 10-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
_	—	—			INT1R<4:0>		
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—		—		—	_
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-13	Unimplemen	ted: Read as ')'				

 bit 12-8
 INT1R<4:0>: Assign External Interrupt 1 (INTR1) to the corresponding RPn pin

 11111 = Input tied to Vss

 11001 = Input tied to RP25

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13.2 Input Capture Registers

REGISTER 13-1: ICxCON: INPUT CAPTURE x CONTROL REGISTER

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	ICSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0
ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>	
bit 7							bit 0

Legend:		HC = Cleared in hardware			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-14	Unimplemented: Read as '0'
bit 13	ICSIDL: Input Capture Module Stop in Idle Control bit
	 1 = Input capture module will halt in CPU Idle mode 0 = Input capture module will continue to operate in CPU Idle mode
bit 12-8	Unimplemented: Read as '0'
bit 7	ICTMR: Input Capture Timer Select bits
	 1 = TMR2 contents are captured on capture event 0 = TMR3 contents are captured on capture event
bit 6-5	ICI<1:0>: Select Number of Captures per Interrupt bits
	 11 = Interrupt on every fourth capture event 10 = Interrupt on every third capture event 01 = Interrupt on every second capture event 00 = Interrupt on every capture event
bit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
	 1 = Input capture overflow occurred 0 = No input capture overflow occurred
bit 3	ICBNE: Input Capture Buffer Empty Status bit (read-only)
	 1 = Input capture buffer is not empty, at least one more capture value can be read 0 = Input capture buffer is empty
bit 2-0	ICM<2:0>: Input Capture Mode Select bits
	 111 = Input capture functions as interrupt pin only when device is in Sleep or Idle mode (Rising edge detect only, all other control bits are not applicable.) 110 = Linused (module disabled)
	101 = Capture mode, every 16th rising edge
	100 = Capture mode, every 4th rising edge
	011 = Capture mode, every rising edge
	010 = Capture mode, every falling edge
	001 = Capture mode, every edge (rising and falling) (ICI<1:0> bits do not control interrupt generation for this mode)
	000 = Input capture module turned off

R-0 HSC	R-0 HSC	U-0	U-0	U-0	R/C-0 HS	R-0 HSC	R-0 HSC		
ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10		
bit 15							bit 8		
R/C-0 HS	R/C-0 HS	R-0 HSC	R/C-0 HSC	R/C-0 HSC	R-0 HSC	R-0 HSC	R-0 HSC		
IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF		
bit 7							bit 0		
Legend:		U = Unimpler	nented bit, rea	ad as '0'					
R = Readable	bit	W = Writable	bit	HS = Set in h	ardware	HSC = Hardwa	are set/cleared		
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown		
bit 15 ACKSTAT: Acknowledge Status bit (when operating as I ² C master, applicable to master transmit operation) 1 = NACK received from slave 0 = ACK received from slave Hardware set or clear at end of slave Acknowledge.									
bit 14 TRSTAT: Transmit Status bit (when operating as I ² C master, applicable to master transmit operation) 1 = Master transmit is in progress (8 bits + ACK) 0 = Master transmit is not in progress Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.									
bit 13-11	Unimplemented: Read as '0'								
bit 10	BCL: Master	Bus Collision	Detect bit						
	1 = A bus coll 0 = No collisio Hardware set	lision has been on at detection of	detected dur	ing a master o	peration				
hit 9	GCSTAT: Ger	neral Call Stati	is hit						
	1 = General o 0 = General o Hardware set	all address wa all address wa when address	s received s not received matches gen	d eral call addre	ess. Hardware c	lear at Stop det	ection.		
bit 8	ADD10: 10-bi	it Address Stat	us bit						
	1 = 10-bit add 0 = 10-bit add Hardware set	dress was mato dress was not r at match of 2r	ched natched id byte of mat	ched 10-bit ad	dress. Hardwar	e clear at Stop	detection.		
bit 7	IWCOL: Write	e Collision Dete	ect bit						
	1 = An attemp 0 = No collision Hardware set	ot to write the li on at occurrence	2CxTRN regis	ster failed beca	ause the I ² C mo	dule is busy			
bit 6	I2COV: Recei	ive Overflow Fl	laα bit			contraro).			
	1 = A byte wa 0 = No overflo Hardware set	as received whi ow at attempt to t	ile the I2CxRC	CV register is s SR to I2CxRC	still holding the p	orevious byte oftware).			
bit 5	D_A: Data/Ac 1 = Indicates 0 = Indicates Hardware clea	ddress bit (whe that the last by that the last by ar at device ad	n operating a rte received w rte received w dress match.	s I ² C slave) as data as device add Hardware set	ress by reception of	slave byte.			
bit 4	P: Stop bit					-			
	 F: Stop bit 1 = Indicates that a Stop bit has been detected last 0 = Stop bit was not detected last Hardware set or clear when Start, Repeated Start or Stop detected. 								

REGISTER 16-2: I2CxSTAT: I2Cx STATUS REGISTER

18.5 ADC Control Registers

REGISTER 18-1: AD1CON1: ADC1 CONTROL REGISTER 1

R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0			
ADON	_	ADSIDL	_	_	AD12B	FORM	<1:0>			
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/C-0			
						HC,HS	HC, HS			
	SSRC<2:0>		—	SIMSAM	ASAM	SAMP	DONE			
bit 7							bit 0			
Legend:		HC = Cleared I	oy hardware	HS = Set by h	nardware	C = Clea	r only bit			
R = Readable	bit	W = Writable b	bit	U = Unimpler	nented bit, read	1 as '0'				
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own			
bit 15	ADON: ADC	Operating Mode	e bit							
	1 = ADC model = ADC is constant	dule is operating ff	9							
hit 14		" ted: Read as '(, [,]							
bit 13		n in Idle Mode h	, it							
bit to	1 = Discontinue module operation when device enters Idle mode									
	0 = Continue module operation in Idle mode									
bit 12-11	Unimplemented: Read as '0'									
bit 10	AD12B: 10-bit or 12-bit Operation Mode bit									
	1 = 12-bit, 1-channel ADC operation									
bit 9-8	FORM<1:0>:	Data Output Fo	ormat bits							
	For 10-bit ope	eration:								
	11 = Signed f	fractional (Dout	= sddd ddd	d dd00 0000	, where $s = .NC$	OT.d<9>)				
	10 = Fraction	al (DOUT = ddd	d dddd dd0(0000)		(d<0>)				
	01 = Olymetric	(DOUT = 0000	00dd dddd o	dddd dddd, M dddd)		.u~9~)				
	For 12-bit ope	eration:		,						
	11 = Signed f	ractional (Dout	= sddd dddd	d dddd 0000	, where $s = .NC$	DT.d<11>)				
	10 = Fraction 01 = Signed I	al (DOUT = ddd Integer (Dout =	d dddd dddo sess sddd	d 0000) dddd dddd M	vhere s = NOT	d<11>)				
	00 = Integer	(DOUT = 0000)	dddd dddd o	iddd)						
bit 7-5	SSRC<2:0>:	Sample Clock S	Source Select	bits						
	111 = Interna	I counter ends	sampling and	starts conversi	on (auto-conve	rt)				
	110 = Reserv	red	nton (ol ondo o	ompling and at	tarta conversion					
	101 = Motor 100 = Reserv	control PVVIVIZ I ved	nterval ends s	ampling and si	tans conversion	1				
	011 = Motor (Control PWM1 i	nterval ends s	ampling and st	tarts conversior	ı				
	010 = GP tim	er 3 compare e	nds sampling	and starts conv	version					
	000 = Clearin	transition on IN no sample hit er	i u pin ends sa Ids sampling a	ampling and sta and starts conve	ans conversion ersion					
bit 4	Unimplemen	ted: Read as '()'							
bit 3	SIMSAM: Sin	nultaneous San	ple Select bit	(applicable onl	ly when CHPS<	<1:0> = 01 or 1	x)			
	When AD12E	B = 1, SIMSAM	is: U-0, Unim	plemented, R	ead as '0'		,			
	1 = Samples	CH0, CH1, CH	2, CH3 simulta	aneously (wher	n CHPS<1:0> =	= 1x); or				
		CH0 and CH1	simultaneously	y (when CHPS	<1:U> = 01)					
	0 - Samples	multiple channe	ere murvioually	in sequence						

NOTES:

22.1 DC Characteristics

TABLE 22-1: OPERATING MIPS VS. VOLTAGE

	Voo Bango	Tomp Pango	Max MIPS
Characteristic	(in Volts)	(in °C)	dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304
_	VBOR-3.6V ⁽¹⁾	-40°C to +85°C	40
—	Vbor-3.6V ⁽¹⁾	-40°C to +125°C	40

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules such as the ADC will have degraded performance. Device functionality is tested but not characterized. Refer to parameter BO10 in Table 22-11 for the minimum and maximum BOR values.

TABLE 22-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Тур	Max	Unit	
Industrial Temperature Devices						
Operating Junction Temperature Range	TJ	-40	—	+125	°C	
Operating Ambient Temperature Range	TA	-40	—	+85	°C	
Extended Temperature Devices						
Operating Junction Temperature Range	TJ	-40	—	+155	°C	
Operating Ambient Temperature Range	TA	-40	—	+125	°C	
Power Dissipation: Internal chip power dissipation: $PINT = VDD x (IDD - \Sigma IOH)$	PD	I	Pint + Pi/c)	W	
$I/O = \Sigma (\{VDD - VOH\} x IOH) + \Sigma (VOL x IOL)$	Power Dissipation: $I/O = \Sigma (\{VDD - VOH\} \times IOH) + \Sigma (VOL \times IOL)$					
Maximum Allowed Power Dissipation	PDMAX	(TJ - TA)/θJ	A	W	

TABLE 22-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Тур	Max	Unit	Notes
Package Thermal Resistance, 44-pin QFN	θja	32		°C/W	1
Package Thermal Resistance, 44-pin TFQP	θја	45	—	°C/W	1
Package Thermal Resistance, 28-pin SPDIP	θја	45	—	°C/W	1
Package Thermal Resistance, 28-pin SOIC	θја	50	—	°C/W	1
Package Thermal Resistance, 28-pin SSOP	θја	71	—	°C/W	1
Package Thermal Resistance, 28-pin QFN-S	θJA	35	_	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ JA) numbers are achieved by package simulations.

TABLE 22-11: ELECTRICAL CHARACTERISTICS: BOR								
DC CHAF	RACTERIS	TICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended					
Param No.	Symbol	Characteristic ⁽¹⁾		Min	Тур	Мах	Units	Conditions
BO10	VBOR	BOR Event on VDD transition high-to-low		2.40	_	2.55	V	See Note 2
Note 1	1. Parameters are for design guidance only and are not tested in manufacturing							

meters are for design guidance only and are not tested in manufacturing.

2: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules such as the ADC will have degraded performance. Device functionality is tested but not characterized.

TABLE 22-12: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial						
				-		-40°C ≤TA ≤+125°C for Extended			
Param No.	Symbol	Characteristic ⁽³⁾	Min	Min Typ ⁽¹⁾ Max		Units	Conditions		
		Program Flash Memory							
D130	Eр	Cell Endurance	10,000	—	—	E/W	-40° C to +125° C		
D131	Vpr	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage		
D132B	VPEW	VDD for Self-Timed Write	VMIN	—	3.6	V	VMIN = Minimum operating voltage		
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40° C to +125° C		
D135	IDDP	Supply Current during Programming	—	10	—	mA			
D136a	Trw	Row Write Time	1.32	—	1.74	ms	Trw = 11064 FRC cycles, Ta = +85°C, See Note 2		
D136b	Trw	Row Write Time	1.28	—	1.79	ms	Trw = 11064 FRC cycles, Ta = +150°C, See Note 2		
D137a	TPE	Page Erase Time	20.1	—	26.5	ms	TPE = 168517 FRC cycles, TA = +85°C, See Note 2		
D137b	TPE	Page Erase Time	19.5	—	27.3	ms	TPE = 168517 FRC cycles, TA = +150°C, See Note 2		
D138a	Tww	Word Write Cycle Time	42.3	—	55.9	μs	Tww = 355 FRC cycles, TA = +85°C, See Note 2		
D138b	Tww	Word Write Cycle Time	41.1	_	57.6	μs	Tww = 355 FRC cycles, TA = +150°C, See Note 2		

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

2: Other conditions: FRC = 7.37 MHz, TUN<5:0> = b'011111 (for Min), TUN<5:0> = b'100000 (for Max). This parameter depends on the FRC accuracy (see Table 22-18) and the value of the FRC Oscillator Tuning register (see Register 8-4). For complete details on calculating the Minimum and Maximum time see Section 5.3 "Programming Operations".

3: These parameters are assured by design, but are not characterized or tested in manufacturing.

TABLE 22-13: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Standard (unless of Operating	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended							
Param No.	Symbol	Characteristics	Min	Тур	Мах	Units	Comments	
_	Cefc	External Filter Capacitor Value ⁽¹⁾	4.7	10	_	μF	Capacitor must be low series resistance (< 5 ohms)	
Note 1:	Typical VCAP voltage = 2.5V when VDD ≥ VDDMIN.							

TABLE 22-21:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMERTIMING REQUIREMENTS

AC CHARACTERISTICS				ard Ope s otherv ting tem	rating C wise sta perature	Condition Ited) e -40°C -40°C	ns: 3.0V to 3.6V S ≤TA ≤+85°C for Industrial S ≤TA ≤+125°C for Extended
Param No.	Symbol	Characteristic	Min	Typ ⁽²⁾	Max	Units	Conditions
SY10	ТмсL	MCLR Pulse-Width (low) ⁽¹⁾	2	_	_	μs	-40°C to +85°C
SY11	Tpwrt	Power-up Timer Period		2 4 16 32 64 128	_	ms	-40°C to +85°C User programmable
SY12	TPOR	Power-on Reset Delay ⁽³⁾	3	10	30	μs	-40°C to +85°C
SY13	Tioz	I/O High-Impedance from MCLR Low or Watchdog Timer Reset ⁽¹⁾	0.68	0.72	1.2	μs	_
SY20	Twdt1	Watchdog Timer Time-out Period ⁽¹⁾	—	_	_	ms	See Section 19.4 "Watchdog Timer (WDT)" and LPRC parameter F21a (Table 22-19).
SY30	Tost	Oscillator Start-up Time	_	1024 Tosc	—	—	Tosc = OSC1 period
SY35	TFSCM	Fail-Safe Clock Monitor Delay ⁽¹⁾	—	500	900	μs	-40°C to +85°C

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

3: These parameters are characterized, but are not tested in manufacturing.



dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

Section Name	Update Description
Section 18.0 "Special Features"	Added FICD register information for address 0xF8000E in the Device Configuration Register Map (see Table 18-1).
	Added FICD register content (BKBUG, COE, JTAGEN, and ICS<1:0> to the dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 Configuration Bits Description (see Table 18-2).
	Added a note regarding the placement of low-ESR capacitors, after the second paragraph of Section 18.2 " On-Chip Voltage Regulator " and to Figure 18-1.
	Removed the words "if enabled" from the second sentence in the fifth paragraph of Section 18.3 "BOR: Brown-out Reset" .
Section 21.0 "Electrical Characteristics"	Updated Max MIPS value for -40°C to +125°C temperature range in Operating MIPS vs. Voltage (see Table 21-1).
	Removed Typ value for parameter DC12 (see Table 22-4).
	Updated MIPS conditions for parameters DC24c, DC44c, DC72a, DC72f and DC72g (see Table 21-5, Table 21-6 and Table 21-8).
	Added Note 4 (reference to new table containing digital-only and analog pin information to I/O Pin Input Specifications (see Table 21-9).
	Updated Typ, Min, and Max values for Program Memory parameters D136, D137, and D138 (see Table 21-12).
	Updated Max value for Internal RC Accuracy parameter F21 for -40°C \leq TA \leq +125°C condition and added Note 2 (see Table 21-19).
	Removed all values for Reset, Watchdog Timer, Oscillator Start-up Timer, and Power-up Timer parameter SY20 and updated conditions, which now refers to Section 18.4 "Watchdog Timer (WDT) " and LPRC parameter F21a (see Table 21-21).
	Updated Min and Typ values for parameters AD60, AD61, AD62 and AD63 and removed Note 3 (see Table 21-37).
	Updated Min and Typ values for parameters AD60, AD61, AD62 and AD63 and removed Note 3 (see Table 21-38).

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Revision E (November 2009)

The revision includes the following global update:

• Added Note 2 to the shaded table that appears at the beginning of each chapter. This new note provides information regarding the availability of registers and their associated bits

This revision also includes minor typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in the following table.

TABLE A-4: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, 16-bit Digital Signal Controllers"	Added information on high temperature operation (see " Operating Range: ").
Section 10.0 "I/O Ports"	Changed the reference to digital-only pins to 5V tolerant pins in the second paragraph of Section 10.2 "Open-Drain Configuration" .
Section 17.0 "Universal Asynchronous Receiver Transmitter (UART)"	Updated the two baud rate range features to: 10 Mbps to 38 bps at 40 MIPS.
Section 18.0 "10-bit/12-bit Analog-to-Digital Converter (ADC)"	Updated the ADC1 block diagrams (see Figure 18-1 and Figure 18-2).
Section 19.0 "Special Features"	Updated the second paragraph and removed the fourth paragraph in Section 19.1 "Configuration Bits" .
Section 22.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings for high temperature and added Note 4. Updated the SPIx Module Slave Mode (CKE = 1) Timing Characteristics (see Figure 22-12). Updated the Internal RC Accuracy parameter numbers (see Table 22-18 and Table 22-19).
Section 23.0 "High Temperature Electrical Characteristics"	Added new chapter with high temperature specifications.
"Product Identification System"	Added the "H" definition for high temperature.

Revision F (November 2009)

This revision includes minor typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in the following table.

TABLE A-5: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, 16-bit Digital Signal Controllers"	Updated MIPS rating from 16 to 20 for high temperature devices in " Operating Range: " and in TABLE 22-1: "Operating MIPS vs. Voltage".