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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

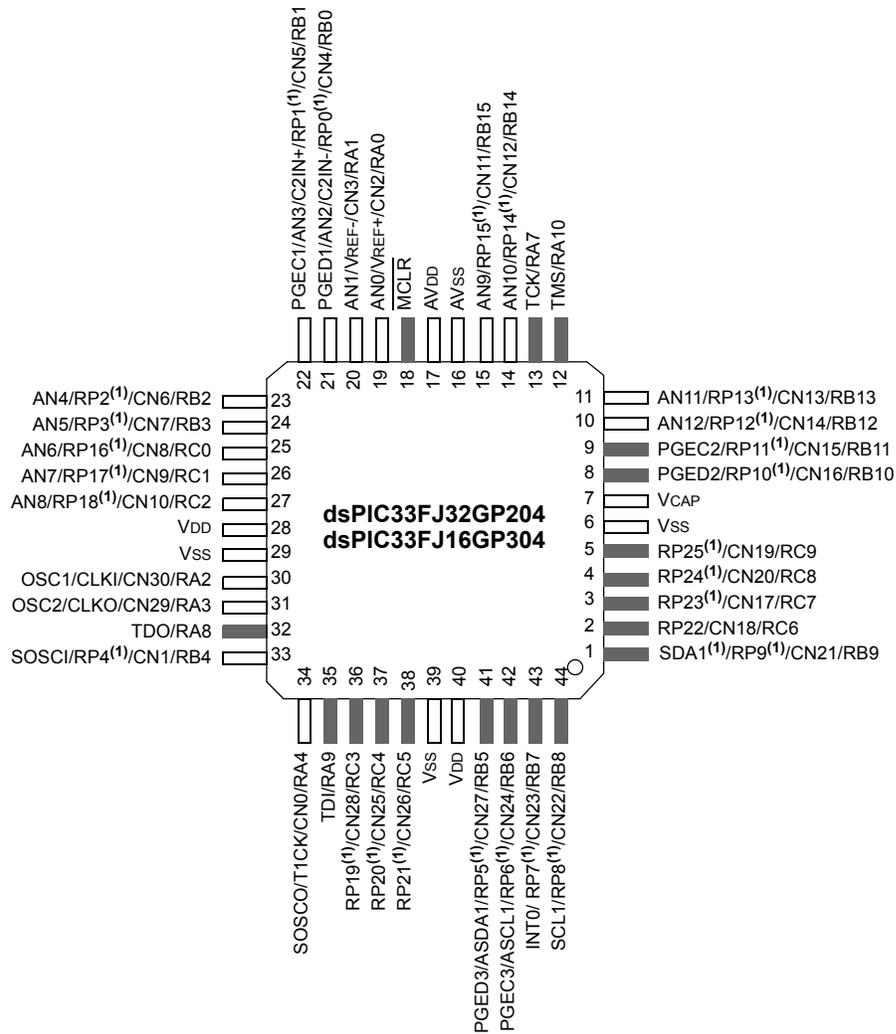
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DCI, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 13x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj32gp204-i-ml">https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj32gp204-i-ml</a>

# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

## Pin Diagrams (Continued)

### 44-Pin TQFP

■ = Pins are up to 5V tolerant



**Note 1:** The RPN pins can be used by any remappable peripheral. See [Table 1](#) for the list of available peripherals.

# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

**TABLE 1-1: PINOUT I/O DESCRIPTIONS**

Pin Name	Pin Type	Buffer Type	PPS	Description
AN0-AN12	I	Analog	No	Analog input channels.
CLKI	I	ST/CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	I	ST/CMOS	No	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	O	—	No	32.768 kHz low-power oscillator crystal output.
CN0-CN30	I	ST	No	Change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
IC1-IC2	I	ST	Yes	Capture inputs 1/2.
IC7-IC8	I	ST	Yes	Capture inputs 7/8.
OCFA	I	ST	Yes	Compare Fault A input (for Compare Channels 1 and 2).
OC1-OC2	O	—	Yes	Compare outputs 1 through 2.
INT0	I	ST	No	External interrupt 0.
INT1	I	ST	Yes	External interrupt 1.
INT2	I	ST	Yes	External interrupt 2.
RA0-RA4	I/O	ST	No	PORTA is a bidirectional I/O port.
RA7-RA10	I/O	ST	No	
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port.
RC0-RC9	I/O	ST	No	PORTC is a bidirectional I/O port.
T1CK	I	ST	No	Timer1 external clock input.
T2CK	I	ST	Yes	Timer2 external clock input.
T3CK	I	ST	Yes	Timer3 external clock input.
$\overline{U1CTS}$	I	ST	Yes	UART1 clear to send.
$\overline{U1RTS}$	O	—	Yes	UART1 ready to send.
U1RX	I	ST	Yes	UART1 receive.
U1TX	O	—	Yes	UART1 transmit.
SCK1	I/O	ST	Yes	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	Yes	SPI1 data in.
SDO1	O	—	Yes	SPI1 data out.
SS1	I/O	ST	Yes	SPI1 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
TMS	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.
PGED1	I/O	ST	No	Data I/O pin for programming/debugging communication channel 1.
PGEC1	I	ST	No	Clock input pin for programming/debugging communication channel 1.
PGED2	I/O	ST	No	Data I/O pin for programming/debugging communication channel 2.
PGEC2	I	ST	No	Clock input pin for programming/debugging communication channel 2.
PGED3	I/O	ST	No	Data I/O pin for programming/debugging communication channel 3.
PGEC3	I	ST	No	Clock input pin for programming/debugging communication channel 3.

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power  
 ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input  
 PPS = Peripheral Pin Select

# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

## 3.0 CPU

**Note 1:** This data sheet summarizes the features of the dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. “CPU”** (DS70204) of the “dsPIC33F/PIC24H Family Reference Manual”, which is available from the Microchip web site: ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for DSP. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. The actual amount of program memory implemented varies by device. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double word move (MOV.D) instruction and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

The dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can serve as a data, address or address offset register. The 16th working register (W15) operates as a software Stack Pointer (SP) for interrupts and calls.

The dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 instruction set has two classes of instructions: MCU and DSP. These two instruction classes are seamlessly integrated into a single CPU. The instruction set includes many addressing modes and is designed for optimum C compiler efficiency. For most instructions, the dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 is capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing  $A + B = C$  operations to be executed in a single cycle.

A block diagram of the CPU is shown in [Figure 3-1](#). The programmer's model for the dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 is shown in [Figure 3-2](#).

## 3.1 Data Addressing Overview

The data space can be addressed as 32K words or 64 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear data space. Certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device-specific.

Overhead-free circular buffers (Modulo Addressing mode) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. Furthermore, the X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms.

The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page (PSVPAG) register. The program to data space mapping feature lets any instruction access program space as if it were data space.

## 3.2 DSP Engine Overview

The DSP engine features a high-speed 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bidirectional barrel shifter. The barrel shifter is capable of shifting a 40-bit value up to 16 bits right or left, in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal real-time performance. The MAC instruction and other associated instructions can concurrently fetch two data operands from memory while multiplying two W registers and accumulating and optionally saturating the result in the same cycle. This instruction functionality requires that the RAM data space be split for these instructions and linear for all others. Data space partitioning is achieved in a transparent and flexible manner through dedicating certain working registers to each address space.

# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

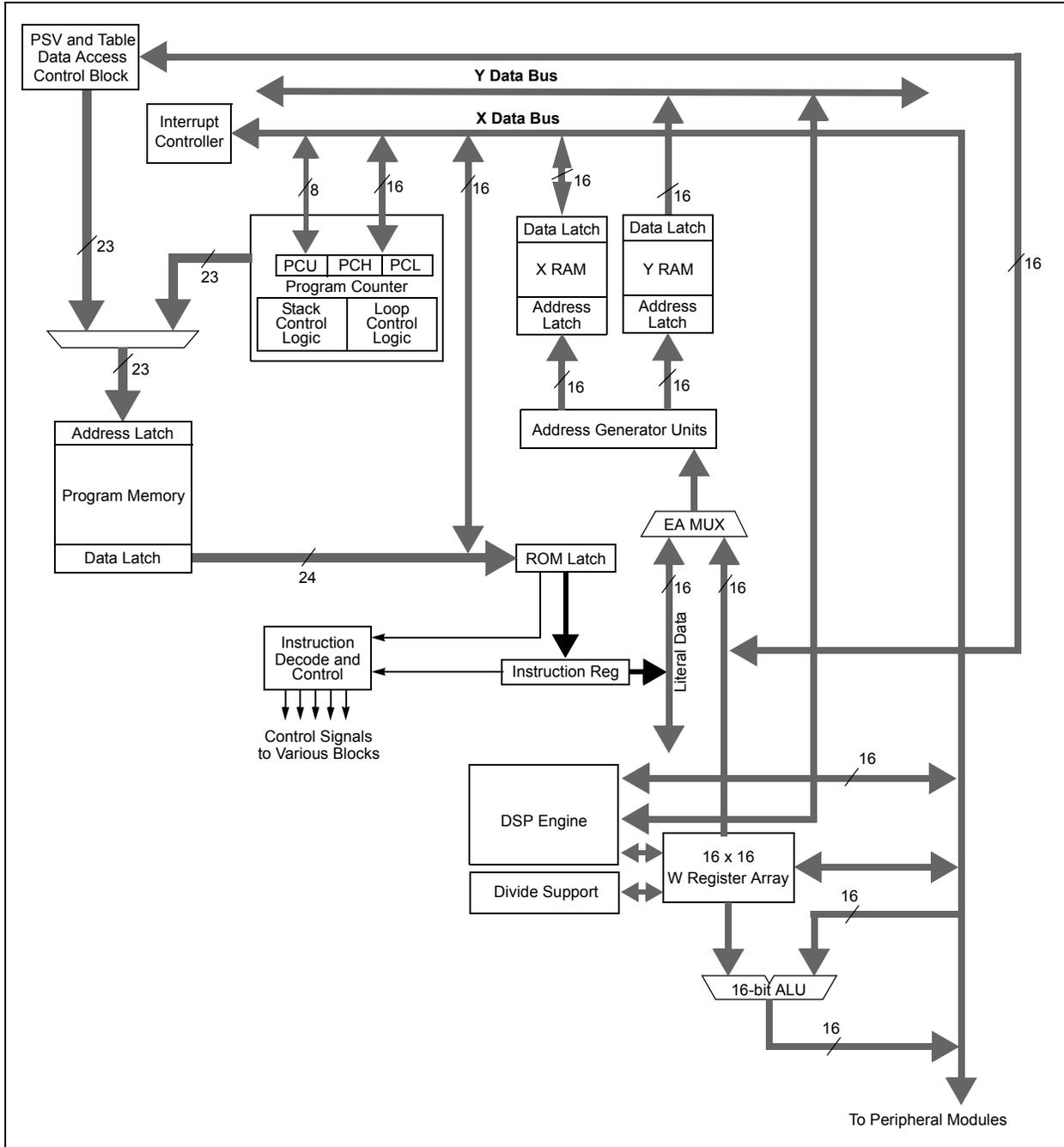
## 3.3 Special MCU Features

The dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 features a 17-bit by 17-bit single-cycle multiplier that is shared by both the MCU ALU and DSP engine. The multiplier can perform signed, unsigned and mixed-sign multiplication. Using a 17-bit by 17-bit multiplier for 16-bit by 16-bit multiplication not only allows you to perform mixed-sign multiplication, it also achieves accurate results for special operations, such as  $(-1.0) \times (-1.0)$ .

The dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 supports 16/16 and 32/16 divide operations, both fractional and integer. All divide instructions are iterative operations. They must be executed within a `REPEAT` loop, resulting in a total execution time of 19 instruction cycles. The divide operation can be interrupted during any of those 19 cycles without loss of data.

A 40-bit barrel shifter is used to perform up to a 16-bit left or right shift in a single cycle. The barrel shifter can be used by both MCU and DSP instructions.

**FIGURE 3-1: dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 CPU CORE BLOCK DIAGRAM**



# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

## 4.0 MEMORY ORGANIZATION

**Note:** This data sheet summarizes the features of the dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 4. “Program Memory”** (DS70202) of the “*dsPIC33F/PIC24H Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

The dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 architecture features separate program and data memory spaces and buses. This architecture also allows the direct access of program memory from the data space during code execution.

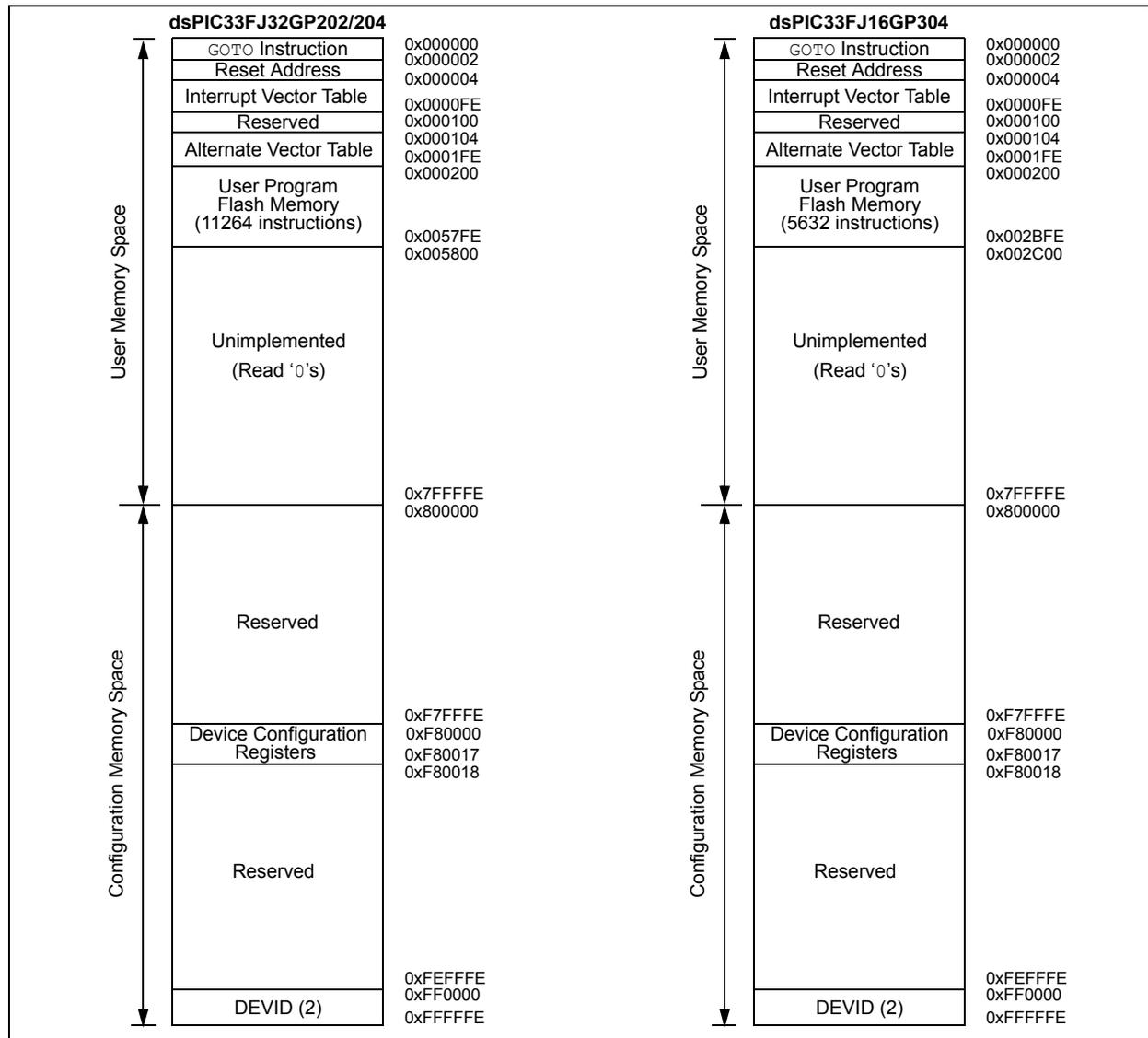
## 4.1 Program Address Space

The program address memory space of the dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit Program Counter (PC) during program execution, or from table operation or data space remapping as described in **Section 4.8 “Interfacing Program and Data Memory Spaces”**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFFFF). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

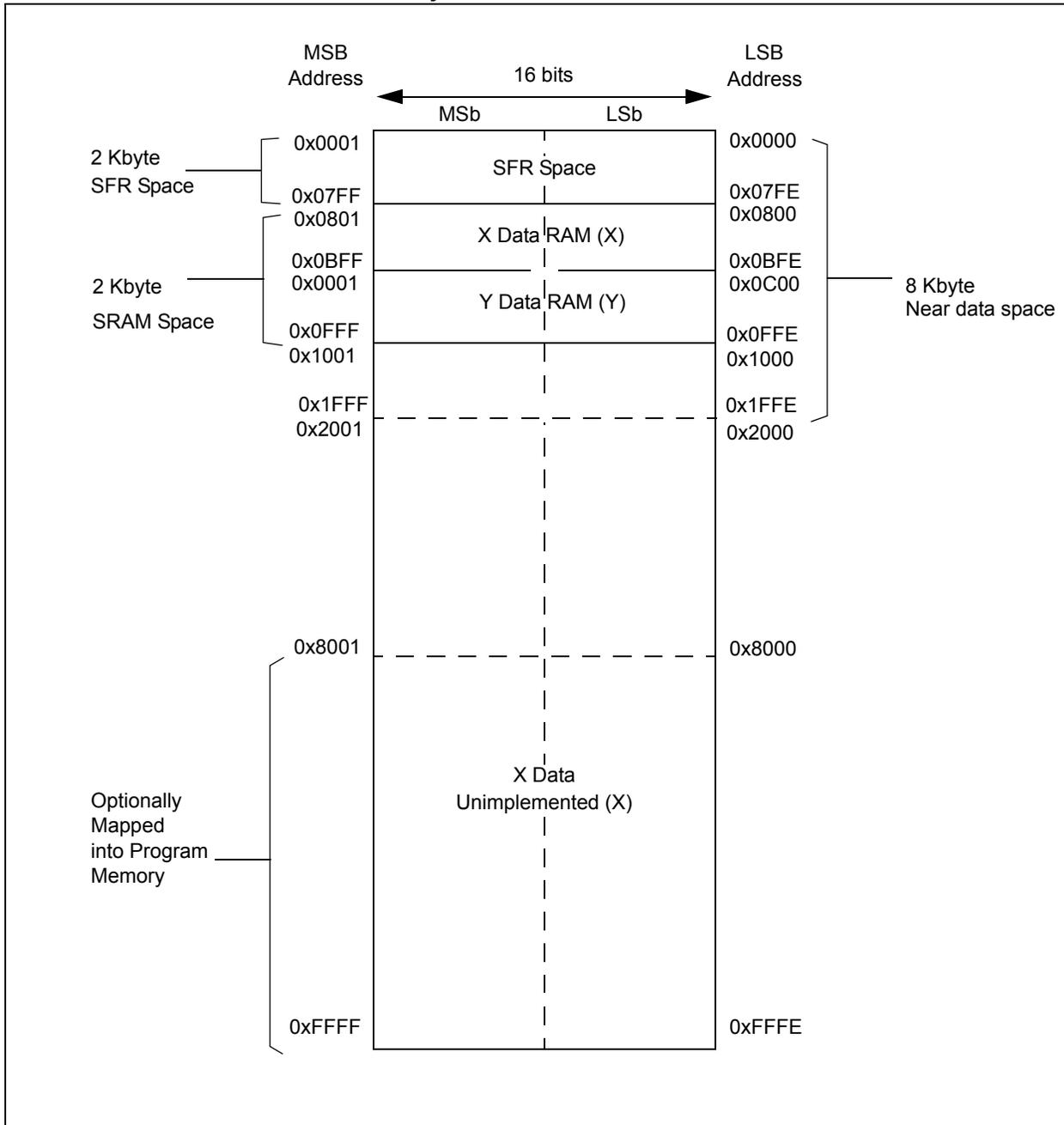
The memory maps for the dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 devices are shown in **Figure 4-1**.

**FIGURE 4-1: PROGRAM MEMORY FOR dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 DEVICES**



# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

**FIGURE 4-3: DATA MEMORY MAP FOR dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 DEVICES WITH 2 Kbytes RAM**



**TABLE 4-8: I2C1 REGISTER MAP**

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	0200	—	—	—	—	—	—	—	—	Receive Register								0000
I2C1TRN	0202	—	—	—	—	—	—	—	—	Transmit Register								00FF
I2C1BRG	0204	—	—	—	—	—	—	—	Baud Rate Generator Register								0000	
I2C1CON	0206	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1STAT	0208	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
I2C1ADD	020A	—	—	—	—	—	—	Address Register								0000		
I2C1MSK	020C	—	—	—	—	—	—	Address Mask Register								0000		

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-9: UART1 REGISTER MAP**

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL<1:0>		STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART Transmit Register								xxxx	
U1RXREG	0226	—	—	—	—	—	—	—	UART Receive Register								0000	
U1BRG	0228	Baud Rate Generator Prescaler															0000	

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-10: SPI1 REGISTER MAP**

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	—	—	—	—	SPROV	—	—	—	—	SPIITBF	SPIIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE<2:0>		PPRE<1:0>		0000	
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	—	0000
SPI1BUF	0248	SPI1 Transmit and Receive Buffer Register															0000	

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

## 4.8 Interfacing Program and Data Memory Spaces

The dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 architecture uses a 24-bit wide program space and a 16-bit wide data space. The architecture is also a modified Harvard scheme, meaning that data can also be present in the program space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304 architecture provides two methods by which program space can be accessed during operation:

- Using table instructions to access individual bytes or words anywhere in the program space
- Remapping a portion of the program space into the data space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look ups from a large table of static data. The application can only access the least significant word of the program word.

### 4.8.1 ADDRESSING PROGRAM SPACE

Since the address ranges for the data and program spaces are 16 and 24 bits, respectively, a method is needed to create a 23-bit or 24-bit program address from 16-bit data registers. The solution depends on the interface method to be used.

For table operations, the 8-bit Table Page register (TBLPAG) is used to define a 32K word region within the program space. This is concatenated with a 16-bit EA to arrive at a full 24-bit program space address. In this format, the Most Significant bit of TBLPAG is used to determine if the operation occurs in the user memory (TBLPAG<7> = 0) or the configuration memory (TBLPAG<7> = 1).

For remapping operations, the 8-bit Program Space Visibility register (PSVPAG) is used to define a 16K word page in the program space. When the Most Significant bit of the EA is '1', PSVPAG is concatenated with the lower 15 bits of the EA to form a 23-bit program space address. Unlike table operations, this limits remapping operations strictly to the user memory area.

Table 4-25 and Figure 4-7 show how the program EA is created for table operations and remapping accesses from the data EA. Here, P<23:0> refers to a program space word, and D<15:0> refers to a data space word.

**TABLE 4-25: PROGRAM SPACE ADDRESS CONSTRUCTION**

Access Type	Access Space	Program Space Address				
		<23>	<22:16>	<15>	<14:1>	<0>
Instruction Access (Code Execution)	User	0	PC<22:1>			0
		0xx xxxx xxxx xxxx xxxx xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG<7:0>		Data EA<15:0>		
		0xxx xxxxx xxxxx xxxxx xxxxx xxxxx				
	Configuration	TBLPAG<7:0>		Data EA<15:0>		
		1xxx xxxxx xxxxx xxxxx xxxxx xxxxx				
Program Space Visibility (Block Remap/Read)	User	0	PSVPAG<7:0>		Data EA<14:0> <sup>(1)</sup>	
		0	xxxx xxxxx xxx xxxxx xxxxx xxxxx			

**Note 1:** Data EA<15> is always '1' in this case, but is not used in calculating the program space address. Bit 15 of the address is PSVPAG<0>.

# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

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NOTES:

# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

## REGISTER 7-8: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IE	OC2IE	IC2IE	—	T1IE	OC1IE	IC1IE	INT0IE
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15-14      **Unimplemented:** Read as '0'
- bit 13      **AD1IE:** ADC1 Conversion Complete Interrupt Enable bit  
             1 = Interrupt request enabled  
             0 = Interrupt request not enabled
- bit 12      **U1TXIE:** UART1 Transmitter Interrupt Enable bit  
             1 = Interrupt request enabled  
             0 = Interrupt request not enabled
- bit 11      **U1RXIE:** UART1 Receiver Interrupt Enable bit  
             1 = Interrupt request enabled  
             0 = Interrupt request not enabled
- bit 10      **SPI1IE:** SPI1 Event Interrupt Enable bit  
             1 = Interrupt request enabled  
             0 = Interrupt request not enabled
- bit 9      **SPI1EIE:** SPI1 Error Interrupt Enable bit  
             1 = Interrupt request enabled  
             0 = Interrupt request not enabled
- bit 8      **T3IE:** Timer3 Interrupt Enable bit  
             1 = Interrupt request enabled  
             0 = Interrupt request not enabled
- bit 7      **T2IE:** Timer2 Interrupt Enable bit  
             1 = Interrupt request enabled  
             0 = Interrupt request not enabled
- bit 6      **OC2IE:** Output Compare Channel 2 Interrupt Enable bit  
             1 = Interrupt request enabled  
             0 = Interrupt request not enabled
- bit 5      **IC2IE:** Input Capture Channel 2 Interrupt Enable bit  
             1 = Interrupt request enabled  
             0 = Interrupt request not enabled
- bit 4      **Unimplemented:** Read as '0'
- bit 3      **T1IE:** Timer1 Interrupt Enable bit  
             1 = Interrupt request enabled  
             0 = Interrupt request not enabled
- bit 2      **OC1IE:** Output Compare Channel 1 Interrupt Enable bit  
             1 = Interrupt request enabled  
             0 = Interrupt request not enabled

# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

## 9.6 Power-Saving Control Registers

**REGISTER 9-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1**

U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
—	—	T3MD	T2MD	T1MD	—	—	—
bit 15						bit 8	

R/W-0	U-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0
I2C1MD	—	U1MD	—	SPI1MD	—	—	AD1MD <sup>(1)</sup>
bit 7						bit 0	

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

- bit 15-14      **Unimplemented:** Read as '0'
- bit 13        **T3MD:** Timer3 Module Disable bit  
1 = Timer3 module is disabled  
0 = Timer3 module is enabled
- bit 12        **T2MD:** Timer2 Module Disable bit  
1 = Timer2 module is disabled  
0 = Timer2 module is enabled
- bit 11        **T1MD:** Timer1 Module Disable bit  
1 = Timer1 module is disabled  
0 = Timer1 module is enabled
- bit 10-8      **Unimplemented:** Read as '0'
- bit 7         **I2C1MD:** I2C1 Module Disable bit  
1 = I2C1 module is disabled  
0 = I2C1 module is enabled
- bit 6         **Unimplemented:** Read as '0'
- bit 5         **U1MD:** UART1 Module Disable bit  
1 = UART1 module is disabled  
0 = UART1 module is enabled
- bit 4         **Unimplemented:** Read as '0'
- bit 3         **SPI1MD:** SPI1 Module Disable bit  
1 = SPI1 module is disabled  
0 = SPI1 module is enabled
- bit 2-1      **Unimplemented:** Read as '0'
- bit 0         **AD1MD:** ADC1 Module Disable bit<sup>(1)</sup>  
1 = ADC1 module is disabled  
0 = ADC1 module is enabled

**Note 1:** PCFGx bits have no effect if the ADC module is disabled by setting this bit. In this case, all port pins multiplexed with ANx will be in Digital mode.

# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

## REGISTER 10-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	
—	—	—	T3CKR<4:0>					
bit 15								bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	
—	—	—	T2CKR<4:0>					
bit 7								bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **T3CKR<4:0>:** Assign Timer3 External Clock (T3CK) to the corresponding RPn pin

11111 = Input tied to Vss

11001 = Input tied to RP25

•  
•  
•

00001 = Input tied to RP1

00000 = Input tied to RP0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **T2CKR<4:0>:** Assign Timer2 External Clock (T2CK) to the corresponding RPn pin

11111 = Input tied to Vss

11001 = Input tied to RP25

•  
•  
•

00001 = Input tied to RP1

00000 = Input tied to RP0

# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

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## REGISTER 15-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)

- bit 4-2      **SPRE<2:0>**: Secondary Prescale bits (Master mode)<sup>(3)</sup>  
            111 = Secondary prescale 1:1  
            110 = Secondary prescale 2:1  
            •  
            •  
            •  
            000 = Secondary prescale 8:1
- bit 1-0      **PPRE<1:0>**: Primary Prescale bits (Master mode)<sup>(3)</sup>  
            11 = Primary prescale 1:1  
            10 = Primary prescale 4:1  
            01 = Primary prescale 16:1  
            00 = Primary prescale 64:1

- Note 1:** The CKE bit is not used in the Framed SPI modes. Program this bit to '0' for the Framed SPI modes (FRMEN = 1).
- 2:** This bit must be cleared when FRMEN = 1.
- 3:** Do not set both Primary and Secondary prescalers to a value of 1:1.

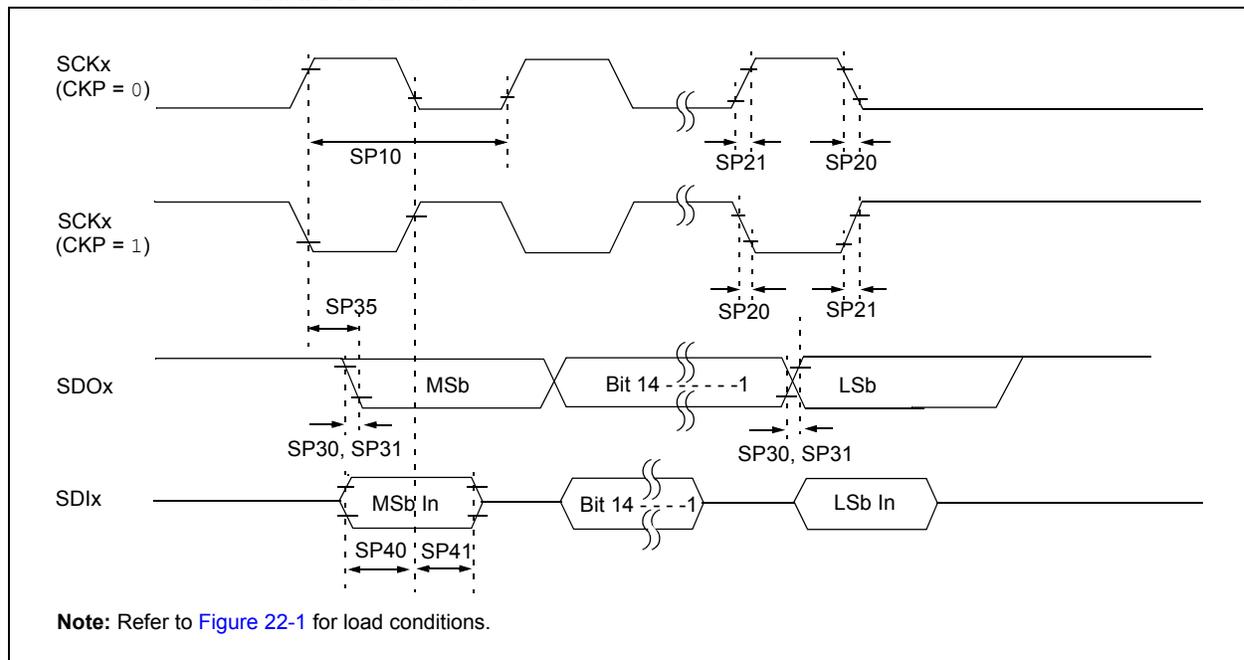
# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

**TABLE 20-2: INSTRUCTION SET OVERVIEW**

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
1	ADD	ADD <i>Acc</i>	Add Accumulators	1	1	OA,OB,SA,SB
		ADD <i>f</i>	$f = f + WREG$	1	1	C,DC,N,OV,Z
		ADD <i>f, WREG</i>	$WREG = f + WREG$	1	1	C,DC,N,OV,Z
		ADD <i>#lit10, Wn</i>	$Wd = lit10 + Wd$	1	1	C,DC,N,OV,Z
		ADD <i>Wb, Ws, Wd</i>	$Wd = Wb + Ws$	1	1	C,DC,N,OV,Z
		ADD <i>Wb, #lit5, Wd</i>	$Wd = Wb + lit5$	1	1	C,DC,N,OV,Z
		ADD <i>Wso, #Slit4, Acc</i>	16-bit Signed Add to Accumulator	1	1	OA,OB,SA,SB
2	ADDC	ADDC <i>f</i>	$f = f + WREG + (C)$	1	1	C,DC,N,OV,Z
		ADDC <i>f, WREG</i>	$WREG = f + WREG + (C)$	1	1	C,DC,N,OV,Z
		ADDC <i>#lit10, Wn</i>	$Wd = lit10 + Wd + (C)$	1	1	C,DC,N,OV,Z
		ADDC <i>Wb, Ws, Wd</i>	$Wd = Wb + Ws + (C)$	1	1	C,DC,N,OV,Z
		ADDC <i>Wb, #lit5, Wd</i>	$Wd = Wb + lit5 + (C)$	1	1	C,DC,N,OV,Z
3	AND	AND <i>f</i>	$f = f .AND. WREG$	1	1	N,Z
		AND <i>f, WREG</i>	$WREG = f .AND. WREG$	1	1	N,Z
		AND <i>#lit10, Wn</i>	$Wd = lit10 .AND. Wd$	1	1	N,Z
		AND <i>Wb, Ws, Wd</i>	$Wd = Wb .AND. Ws$	1	1	N,Z
		AND <i>Wb, #lit5, Wd</i>	$Wd = Wb .AND. lit5$	1	1	N,Z
4	ASR	ASR <i>f</i>	$f = \text{Arithmetic Right Shift } f$	1	1	C,N,OV,Z
		ASR <i>f, WREG</i>	$WREG = \text{Arithmetic Right Shift } f$	1	1	C,N,OV,Z
		ASR <i>Ws, Wd</i>	$Wd = \text{Arithmetic Right Shift } Ws$	1	1	C,N,OV,Z
		ASR <i>Wb, Wns, Wnd</i>	$Wnd = \text{Arithmetic Right Shift } Wb \text{ by } Wns$	1	1	N,Z
		ASR <i>Wb, #lit5, Wnd</i>	$Wnd = \text{Arithmetic Right Shift } Wb \text{ by } lit5$	1	1	N,Z
5	BCLR	BCLR <i>f, #bit4</i>	Bit Clear <i>f</i>	1	1	None
		BCLR <i>Ws, #bit4</i>	Bit Clear <i>Ws</i>	1	1	None
6	BRA	BRA <i>C, Expr</i>	Branch if Carry	1	1 (2)	None
		BRA <i>GE, Expr</i>	Branch if greater than or equal	1	1 (2)	None
		BRA <i>GEU, Expr</i>	Branch if unsigned greater than or equal	1	1 (2)	None
		BRA <i>GT, Expr</i>	Branch if greater than	1	1 (2)	None
		BRA <i>GTU, Expr</i>	Branch if unsigned greater than	1	1 (2)	None
		BRA <i>LE, Expr</i>	Branch if less than or equal	1	1 (2)	None
		BRA <i>LEU, Expr</i>	Branch if unsigned less than or equal	1	1 (2)	None
		BRA <i>LT, Expr</i>	Branch if less than	1	1 (2)	None
		BRA <i>LTU, Expr</i>	Branch if unsigned less than	1	1 (2)	None
		BRA <i>N, Expr</i>	Branch if Negative	1	1 (2)	None
		BRA <i>NC, Expr</i>	Branch if Not Carry	1	1 (2)	None
		BRA <i>NN, Expr</i>	Branch if Not Negative	1	1 (2)	None
		BRA <i>NOV, Expr</i>	Branch if Not Overflow	1	1 (2)	None
		BRA <i>NZ, Expr</i>	Branch if Not Zero	1	1 (2)	None
		BRA <i>OA, Expr</i>	Branch if Accumulator A overflow	1	1 (2)	None
		BRA <i>OB, Expr</i>	Branch if Accumulator B overflow	1	1 (2)	None
		BRA <i>OV, Expr</i>	Branch if Overflow	1	1 (2)	None
		BRA <i>SA, Expr</i>	Branch if Accumulator A saturated	1	1 (2)	None
		BRA <i>SB, Expr</i>	Branch if Accumulator B saturated	1	1 (2)	None
		BRA <i>Expr</i>	Branch Unconditionally	1	2	None
BRA <i>Z, Expr</i>	Branch if Zero	1	1 (2)	None		
BRA <i>Wn</i>	Computed Branch	1	2	None		
7	BSET	BSET <i>f, #bit4</i>	Bit Set <i>f</i>	1	1	None
		BSET <i>Ws, #bit4</i>	Bit Set <i>Ws</i>	1	1	None
8	BSW	BSW.C <i>Ws, Wb</i>	Write C bit to $Ws<Wb>$	1	1	None
		BSW.Z <i>Ws, Wb</i>	Write Z bit to $Ws<Wb>$	1	1	None
9	BTG	BTG <i>f, #bit4</i>	Bit Toggle <i>f</i>	1	1	None
		BTG <i>Ws, #bit4</i>	Bit Toggle <i>Ws</i>	1	1	None

# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

**FIGURE 22-12: SPIx MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS**



**TABLE 22-31: SPIx MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Typ <sup>(2)</sup>	Max	Units	Conditions
SP10	TscP	Maximum SCK Frequency	—	—	9	MHz	-40°C to +125°C and see <b>Note 3</b>
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See parameter <b>DO32</b> and <b>Note 4</b>
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See parameter <b>DO31</b> and <b>Note 4</b>
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See parameter <b>DO32</b> and <b>Note 4</b>
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See parameter <b>DO31</b> and <b>Note 4</b>
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	—
SP36	TdoV2sch, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	—
SP40	TdiV2sch, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**Note 2:** Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

**Note 3:** The minimum clock period for SCKx is 111 ns. The clock generated in Master mode must not violate this specification.

**Note 4:** Assumes 50 pF load on all SPIx pins.

# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

**TABLE 22-38: ADC MODULE SPECIFICATIONS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ	Max.	Units	Conditions
<b>Device Supply</b>							
AD01	AVDD	Module VDD Supply <sup>(2)</sup>	Greater of VDD – 0.3 or 3.0	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module VSS Supply <sup>(2)</sup>	VSS – 0.3	—	VSS + 0.3	V	—
<b>Reference Inputs</b>							
AD05	VREFH	Reference Voltage High	AVSS + 2.5	—	AVDD	V	See <b>Note 1</b>
AD05a			3.0	—	3.6	V	VREFH = AVDD VREFL = AVSS = 0, see <b>Note 2</b>
AD06	VREFL	Reference Voltage Low	AVSS	—	AVDD – 2.5	V	See <b>Note 1</b>
AD06a			0	—	0	V	VREFH = AVDD VREFL = AVSS = 0, see <b>Note 2</b>
AD07	VREF	Absolute Reference Voltage <sup>(2)</sup>	2.5	—	3.6	V	VREF = VREFH - VREFL
AD08	IREF	Current Drain	—	250	550	$\mu\text{A}$	ADC operating, See <b>Note 1</b>
			—	—	10	$\mu\text{A}$	ADC off, See <b>Note 1</b>
AD08a	IAD	Operating Current	—	7.0	9.0	mA	10-bit ADC mode, See <b>Note 2</b>
			—	2.7	3.2	mA	12-bit ADC mode, See <b>Note 2</b>
<b>Analog Input</b>							
AD12	VINH	Input Voltage Range VINH <sup>(2)</sup>	VINL	—	VREFH	V	This voltage reflects Sample and Hold Channels 0, 1, 2, and 3 (CH0-CH3), positive input
AD13	VINL	Input Voltage Range VINL <sup>(2)</sup>	VREFL	—	AVSS + 1V	V	This voltage reflects Sample and Hold Channels 0, 1, 2, and 3 (CH0-CH3), negative input
AD17	RIN	Recommended Impedance of Analog Voltage Source <sup>(3)</sup>	—	—	200	$\Omega$	10-bit ADC
			—	—	200	$\Omega$	12-bit ADC

**Note 1:** These parameters are not characterized or tested in manufacturing.

**Note 2:** These parameters are characterized, but are not tested in manufacturing.

**Note 3:** These parameters are assured by design, but are not characterized or tested in manufacturing.

# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

**TABLE 23-15: ADC MODULE SPECIFICATIONS**

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
<b>Reference Inputs</b>							
HAD08	IREF	Current Drain	—	250	600	$\mu\text{A}$	ADC operating, See <b>Note 1</b>
			—	—	50	$\mu\text{A}$	ADC off, See <b>Note 1</b>

**Note 1:** These parameters are not characterized or tested in manufacturing.

**2:** These parameters are characterized, but are not tested in manufacturing.

**TABLE 23-16: ADC MODULE SPECIFICATIONS (12-BIT MODE)<sup>(3)</sup>**

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
<b>ADC Accuracy (12-bit Mode) – Measurements with External VREF+/VREF-<sup>(1)</sup></b>							
HAD20a	Nr	Resolution <sup>(3)</sup>	12 data bits			bits	—
HAD21a	INL	Integral Nonlinearity	-2	—	+2	LSb	V <sub>INL</sub> = AV <sub>SS</sub> = V <sub>REFL</sub> = 0V, AV <sub>DD</sub> = V <sub>REFH</sub> = 3.6V
HAD22a	DNL	Differential Nonlinearity	> -1	—	< 1	LSb	V <sub>INL</sub> = AV <sub>SS</sub> = V <sub>REFL</sub> = 0V, AV <sub>DD</sub> = V <sub>REFH</sub> = 3.6V
HAD23a	GERR	Gain Error	-2	—	10	LSb	V <sub>INL</sub> = AV <sub>SS</sub> = V <sub>REFL</sub> = 0V, AV <sub>DD</sub> = V <sub>REFH</sub> = 3.6V
HAD24a	E <sub>OFF</sub>	Offset Error	-3	—	5	LSb	V <sub>INL</sub> = AV <sub>SS</sub> = V <sub>REFL</sub> = 0V, AV <sub>DD</sub> = V <sub>REFH</sub> = 3.6V
<b>ADC Accuracy (12-bit Mode) – Measurements with Internal VREF+/VREF-<sup>(1)</sup></b>							
HAD20a	Nr	Resolution <sup>(3)</sup>	12 data bits			bits	—
HAD21a	INL	Integral Nonlinearity	-2	—	+2	LSb	V <sub>INL</sub> = AV <sub>SS</sub> = 0V, AV <sub>DD</sub> = 3.6V
HAD22a	DNL	Differential Nonlinearity	> -1	—	< 1	LSb	V <sub>INL</sub> = AV <sub>SS</sub> = 0V, AV <sub>DD</sub> = 3.6V
HAD23a	GERR	Gain Error	2	—	20	LSb	V <sub>INL</sub> = AV <sub>SS</sub> = 0V, AV <sub>DD</sub> = 3.6V
HAD24a	E <sub>OFF</sub>	Offset Error	2	—	10	LSb	V <sub>INL</sub> = AV <sub>SS</sub> = 0V, AV <sub>DD</sub> = 3.6V
<b>Dynamic Performance (12-bit Mode)<sup>(2)</sup></b>							
HAD33a	F <sub>NYQ</sub>	Input Signal Bandwidth	—	—	200	kHz	—

**Note 1:** These parameters are characterized, but are tested at 20 ksps only.

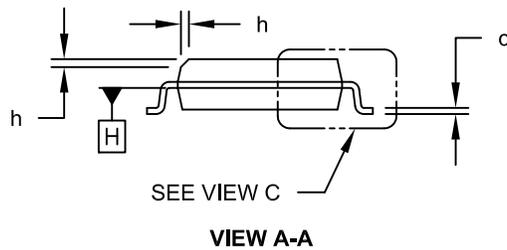
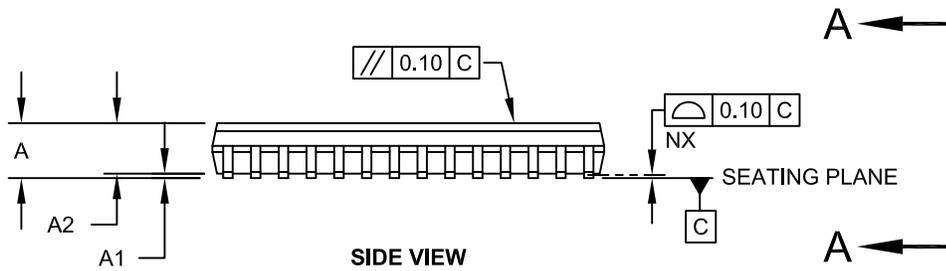
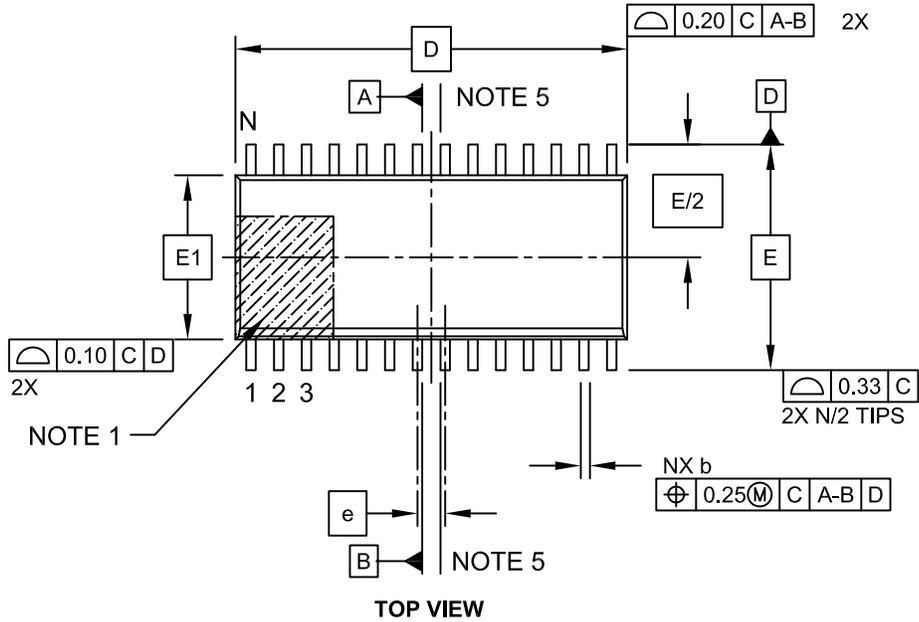
**2:** These parameters are characterized by similarity, but are not tested in manufacturing.

**3:** Injection currents  $> |0|$  can affect the ADC results by approximately 4-6 counts.

# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

## 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-052C Sheet 1 of 2

# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

## Revision D (October 2009)

This revision includes minor typographical and formatting changes throughout the data sheet text.

Global changes include:

- Changed all instances of OSC1 to OSC1 and OSC0 to OSC2.
- Changed all instances of PGCx/EMUCx and PGDx/EMUDx (where x = 1, 2 or 3) to PGECx and PGEDx.

Changed all instances of VDDCORE and VDDCORE/VCAP to VCAP/VDDCORE

All other major changes are referenced by their respective section in the following table.

**TABLE A-3: MAJOR SECTION UPDATES**

Section Name	Update Description
<b>“High-Performance, 16-bit Digital Signal Controllers”</b>	Added Note 2 to the 28-Pin QFN-S and 44-Pin QFN pin diagrams, which references pin connections to Vss.
<b>Section 8.0 “Oscillator Configuration”</b>	Updated the Oscillator System Diagram (see Figure 8-1). Added Note 1 to the Oscillator Tuning (OSCTUN) register (see Register 8-4).
<b>Section 10.0 “I/O Ports”</b>	Removed Table 10-1 and added reference to pin diagrams for I/O pin availability and functionality.
<b>Section 15.0 “Serial Peripheral Interface (SPI)”</b>	Added Note 2 to the SPIx Control Register 1 (see Register 15-2).
<b>Section 17.0 “Universal Asynchronous Receiver Transmitter (UART)”</b>	Updated the UTXINV bit settings in the UxSTA register and added Note 1 (see Register 17-2).
<b>Section 22.0 “Electrical Characteristics”</b>	Updated the Min value for parameter DC12 (RAM Retention Voltage) and added Note 4 to the DC Temperature and Voltage Specifications (see Table 22-4). Updated the Min value for parameter DI35 (see Table 22-20). Updated AD08 and added reference to Note 2 for parameters AD05a, AD06a and AD08a (see Table 22-34).

# dsPIC33FJ32GP202/204 and dsPIC33FJ16GP304

## Revision H (July 2011)

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in the following table.

**TABLE A-7: MAJOR SECTION UPDATES**

Section Name	Update Description
<b>Section 19.0 “Special Features”</b>	Added Note 3 to the Connections for the On-chip Voltage Regulator diagram (see Figure 19-1).
<b>Section 22.0 “Electrical Characteristics”</b>	Removed Note 3 and parameter DC10 (V <sub>CORE</sub> ) from the DC Temperature and Voltage Specifications (see Table 22-4).  Updated the Characteristics definition and Conditions for parameter BO10 in the Electrical Characteristics: BOR (see Table 22-11).  Added Note 1 to the Internal Voltage Regulator Specifications (see Table 22-13).

## Revision J (June 2012)

This revision includes typographical and formatting changes throughout the data sheet text.

In addition, where applicable, new sections were added to each peripheral chapter that provide information and links to related resources, as well as helpful tips. For examples, see [Section 8.2 “Oscillator Resources”](#) and [Section 18.3 “ADC Helpful Tips”](#).

All other major changes are referenced by their respective section in the following table.

**TABLE A-8: MAJOR SECTION UPDATES**

Section Name	Update Description
<a href="#">Section 22.0 “Electrical Characteristics”</a>	Added Note 1 to the Operating MIPS vs. Voltage (see <a href="#">Table 22-1</a> ). Updated the notes in the following tables: <ul style="list-style-type: none"><li>• Operating Current (I<sub>DD</sub>) (see <a href="#">Table 22-5</a>)</li><li>• Idle Current (I<sub>IDLE</sub>) (see <a href="#">Table 22-6</a>)</li><li>• Power-Down Current (I<sub>PD</sub>) (see <a href="#">Table 22-7</a>)</li><li>• Doze Current (I<sub>DOZE</sub>) (see <a href="#">Table 22-8</a>)</li></ul> Updated the conditions for Program Memory parameters D136b, D137b, and D138b (T <sub>A</sub> = +150°C) (see <a href="#">Table 22-12</a> ).
<a href="#">Section 23.0 “High Temperature Electrical Characteristics”</a>	Removed Table 23-8: DC Characteristics: Program Memory.
<a href="#">Section 24.0 “DC and AC Device Characteristics Graphs”</a>	Added new chapter.