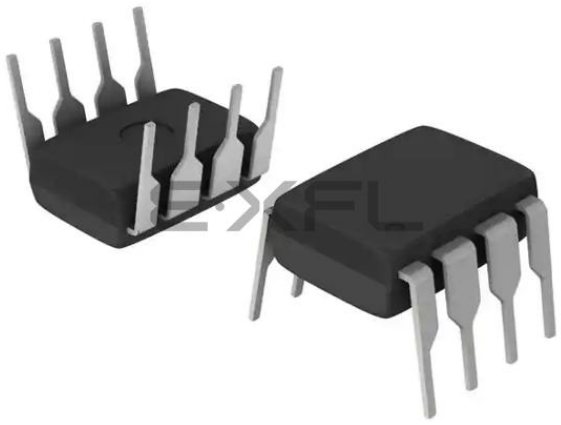

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	3
Program Memory Size	384B (256 x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic10f200-e-p

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC10F200/202/204/206 devices can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC10F200/202/204/206 devices use a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architectures where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide, making it possible to have all single-word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (1 μs @ 4 MHz) except for program branches.

The table below lists program memory (Flash) and data memory (RAM) for the PIC10F200/202/204/206 devices.

TABLE 3-1: PIC10F2XX MEMORY

Device	Memory	
	Program	Data
PIC10F200	256 x 12	16 x 8
PIC10F202	512 x 12	24 x 8
PIC10F204	256 x 12	16 x 8
PIC10F206	512 x 12	24 x 8

The PIC10F200/202/204/206 devices can directly or indirectly address its register files and data memory. All Special Function Registers (SFR), including the PC, are mapped in the data memory. The PIC10F200/202/204/206 devices have a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation, on any register, using any addressing mode. This symmetrical nature and lack of “special optimal situations” make programming with the PIC10F200/202/204/206 devices simple, yet efficient. In addition, the learning curve is reduced significantly.

The PIC10F200/202/204/206 devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two’s complement in nature. In two-operand instructions, one operand is typically the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC) and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1 and Figure 3-2, with the corresponding device pins described in Table 3-2.

FIGURE 3-1: PIC10F200/202 BLOCK DIAGRAM

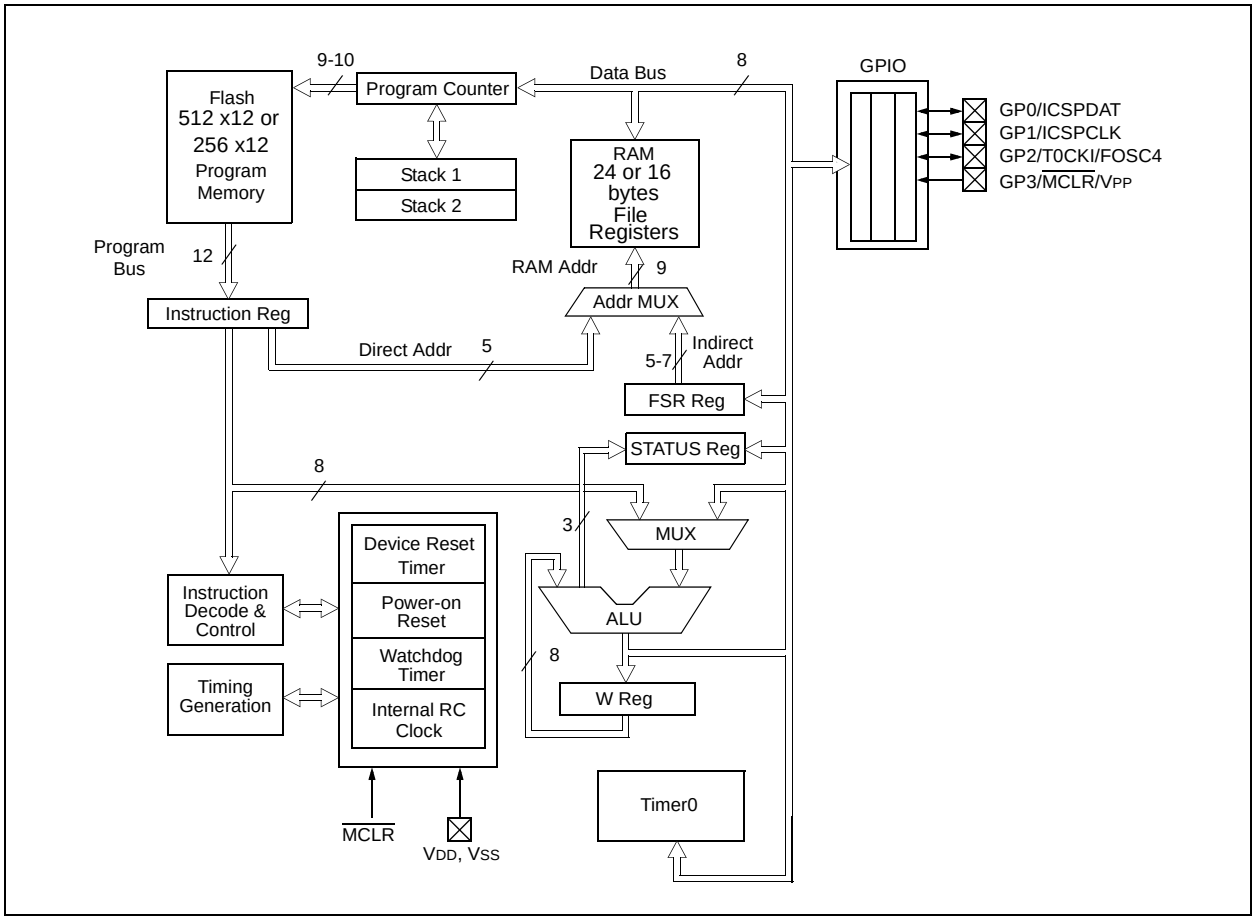


FIGURE 3-2: PIC10F204/206 BLOCK DIAGRAM

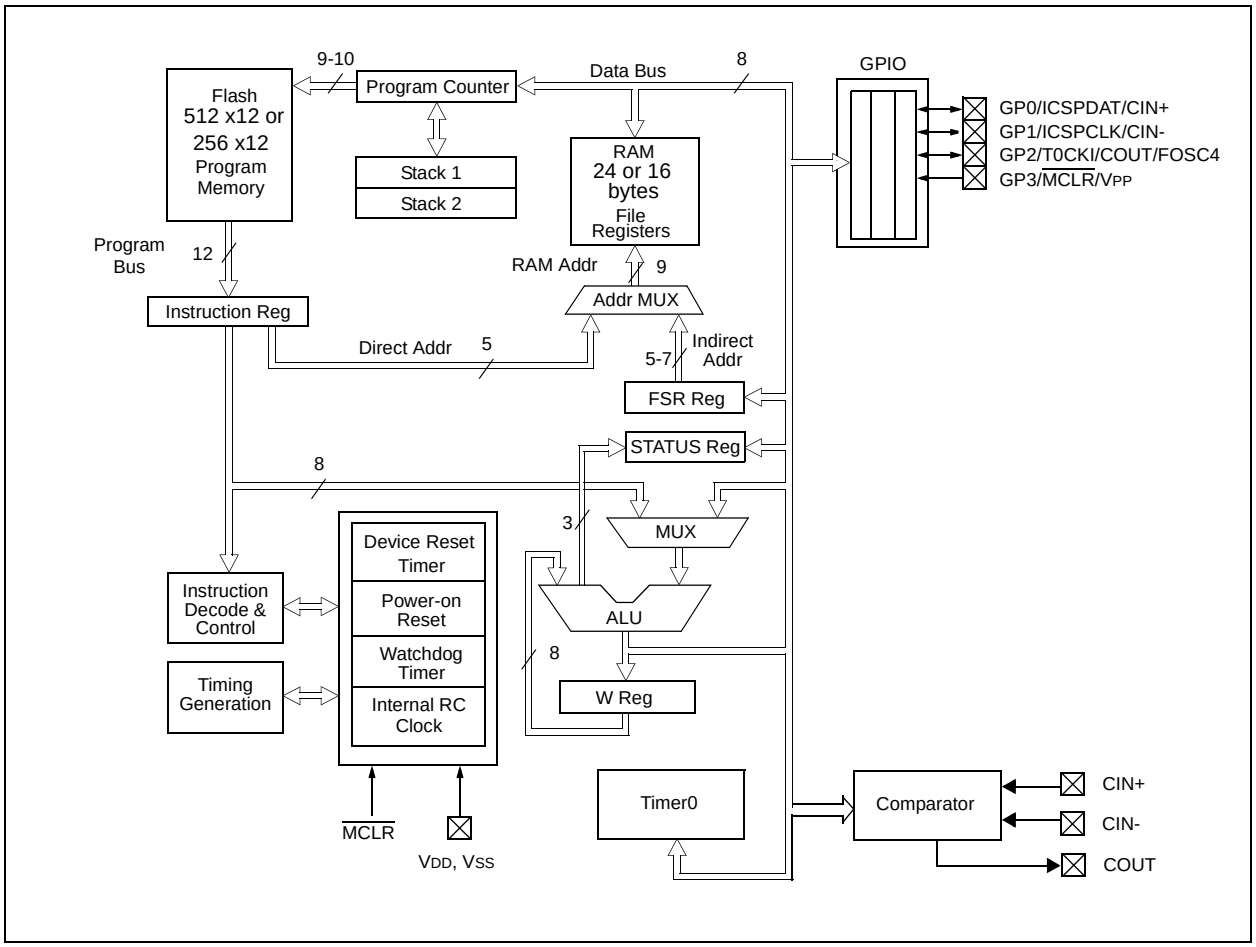
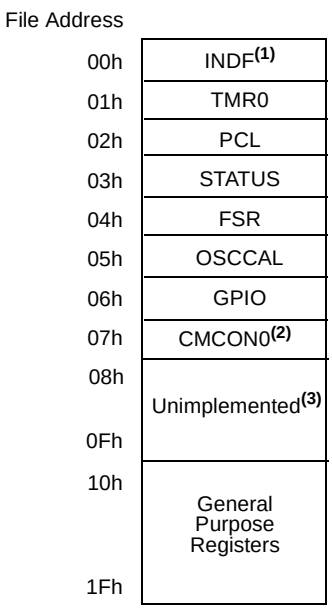


TABLE 3-2: PIC10F200/202/204/206 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
GP0/ICSPDAT/CIN+	GP0	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	ICSPDAT	ST	CMOS	In-Circuit Serial Programming™ data pin.
	CIN+	AN	—	Comparator input (PIC10F204/206 only).
GP1/ICSPCLK/CIN-	GP1	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	ICSPCLK	ST	CMOS	In-Circuit Serial Programming clock pin.
	CIN-	AN	—	Comparator input (PIC10F204/206 only).
GP2/T0CKI/COUT/ FOSC4	GP2	TTL	CMOS	Bidirectional I/O pin.
	T0CKI	ST	—	Clock input to TMR0.
	COUT	—	CMOS	Comparator output (PIC10F204/206 only).
	FOSC4	—	CMOS	Oscillator/4 output.
GP3/$\overline{\text{MCLR}}$/V_{PP}	GP3	TTL	—	Input pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear (Reset). When configured as $\overline{\text{MCLR}}$, this pin is an active-low Reset to the device. Voltage on GP3/$\overline{\text{MCLR}}$/V_{PP} must not exceed V_{DD} during normal device operation or the device will enter Programming mode. Weak pull-up always on if configured as $\overline{\text{MCLR}}$.
	V_{PP}	HV	—	Programming voltage input.
V_{DD}	V_{DD}	P	—	Positive supply for logic and I/O pins.
V_{SS}	V_{SS}	P	—	Ground reference for logic and I/O pins.

Legend: I = Input, O = Output, I/O = Input/Output, P = Power, — = Not used, TTL = TTL input, ST = Schmitt Trigger input, AN = Analog input

FIGURE 4-3: PIC10F200/204 REGISTER FILE MAP

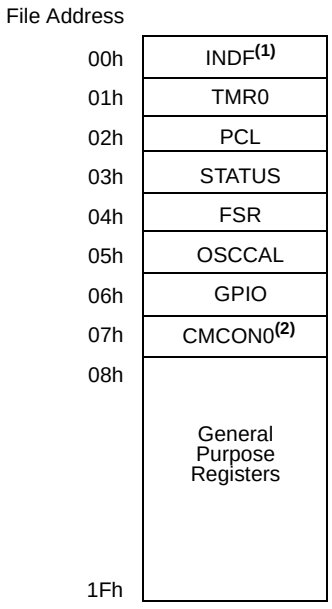


Note 1: Not a physical register. See **Section 4.9 "Indirect Data Addressing: INDF and FSR Registers"**.

2: PIC10F204 only. Unimplemented on the PIC10F200 and reads as 00h.

3: Unimplemented, read as 00h.

FIGURE 4-4: PIC10F202/206 REGISTER FILE MAP



Note 1: Not a physical register. See **Section 4.9 "Indirect Data Addressing: INDF and FSR Registers"**.

2: PIC10F206 only. Unimplemented on the PIC10F202 and reads as 00h.

4.6 OSCCAL Register

The Oscillator Calibration (OSCCAL) register is used to calibrate the internal precision 4 MHz oscillator. It contains seven bits for calibration**.**

Note:	Erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be read prior to erasing the part so it can be reprogrammed correctly later.

After you move in the calibration constant, do not change the value. See **Section 9.2.2 "Internal 4 MHz Oscillator"**.

REGISTER 4-3: OSCCAL REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0
CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	FOSC4
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-1 **CAL<6:0>:** Oscillator Calibration bits

0111111 = Maximum frequency
•
•
•
0000001
0000000 = Center frequency
1111111
•
•
•
1000000 = Minimum frequency

bit 0 **FOSC4:** INTOSC/4 Output Enable bit(1)

1 = INTOSC/4 output onto GP2
0 = GP2/T0CKI/COUT applied to GP2

Note 1: Overrides GP2/T0CKI/COUT control registers when enabled.

TABLE 5-2: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	TRISGPIO	—	—	—	—	I/O Control Register				---- 1111	---- 1111
N/A	OPTION	$\overline{\text{GPWU}}$	$\overline{\text{GPPU}}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
03h	STATUS	GPWUF	CWUF	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	00-1 1xxx	qq-q quuu(1), (2)
06h	GPIO	—	—	—	—	GP3	GP2	GP1	GP0	---- xxxx	---- uuuu

Legend: Shaded cells are not used by PORT registers, read as '0', – = unimplemented, read as '0', x = unknown, u = unchanged, q = depends on condition.

Note 1: If Reset was due to wake-up on pin change, then bit 7 = 1. All other Resets will cause bit 7 = 0.

2: If Reset was due to wake-up on comparator change, then bit 6 = 1. All other Resets will cause bit 6 = 0.

5.4 I/O Programming Considerations

5.4.1 BIDIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and rewrite the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit 2 of GPIO will cause all eight bits of GPIO to be read into the CPU, bit 2 to be set and the GPIO value to be written to the output latches. If another bit of GPIO is used as a bidirectional I/O pin (say bit 0), and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit 0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential Read-Modify-Write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired OR", "wired AND"). The resulting high output currents may damage the chip.

EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial GPIO Settings
;GPIO<3:2> Inputs
;GPIO<1:0> Outputs
;
;                 GPIO latch   GPIO pins
;                 ----------   ----------
 BCF    GPIO,  1 ;---- pp01    ---- pp11
 BCF    GPIO,  0 ;---- pp10    ---- pp11
 MOVLW  007h;
 TRIS   GPIO     ;---- pp10    ---- pp11
;
```

Note 1: The user may have expected the pin values to be ---- pp00. The 2nd BCF caused GP1 to be latched as the pin value (High).

5.4.2 SUCCESSIVE OPERATIONS ON I/O PORTS

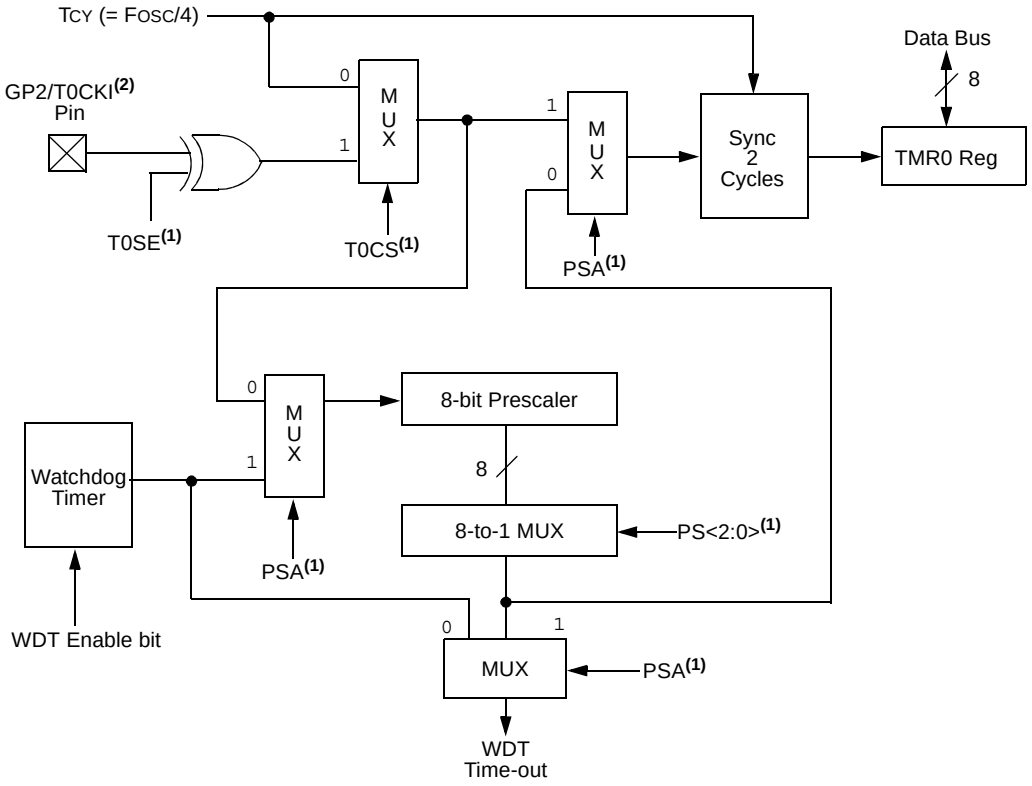
The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction causes that file to be read into the CPU. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

To change the prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A CLRWDT instruction should be executed before switching the prescaler.

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT              ;Clear WDT and
                    ;prescaler
MOVLW  'xxxx0xxx'   ;Select TMR0, new
                    ;prescale value and
                    ;clock source
OPTION
```

FIGURE 6-5: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note 1: T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

2: T0CKI is shared with pin GP2 on the PIC10F200/202/204/206.

8.0 COMPARATOR MODULE

The comparator module contains one Analog comparator. The inputs to the comparator are multiplexed with GP0 and GP1 pins. The output of the comparator can be placed on GP2.

The CMCON0 register, shown in Register 8-1, controls the comparator operation. A block diagram of the comparator is shown in Figure 8-1.

REGISTER 8-1: CMCON0 REGISTER

R-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
CMPOUT	$\overline{\text{COUTEN}}$	POL	$\overline{\text{CMPT0CS}}$	CMPON	CNREF	CPREF	$\overline{\text{CWU}}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **CMPOUT:** Comparator Output bit
1 = $V_{IN}+ > V_{IN}-$
0 = $V_{IN}+ < V_{IN}-$

bit 6 **$\overline{\text{COUTEN}}$:** Comparator Output Enable bit(1, 2)
1 = Output of comparator is NOT placed on the COUT pin
0 = Output of comparator is placed in the COUT pin

bit 5 **POL:** Comparator Output Polarity bit(2)
1 = Output of comparator not inverted
0 = Output of comparator inverted

bit 4 **$\overline{\text{CMPT0CS}}$:** Comparator TMR0 Clock Source bit(2)
1 = TMR0 clock source selected by T0CS control bit
0 = Comparator output used as TMR0 clock source

bit 3 **CMPON:** Comparator Enable bit
1 = Comparator is on
0 = Comparator is off

bit 2 **CNREF:** Comparator Negative Reference Select bit(2)
1 = CIN- pin(3)
0 = Internal voltage reference

bit 1 **CPREF:** Comparator Positive Reference Select bit(2)
1 = CIN+ pin(3)
0 = CIN- pin(3)

bit 0 **$\overline{\text{CWU}}$:** Comparator Wake-up on Change Enable bit(2)
1 = Wake-up on comparator change is disabled
0 = Wake-up on comparator change is enabled.

Note 1: Overrides T0CS bit for TRIS control of GP2.

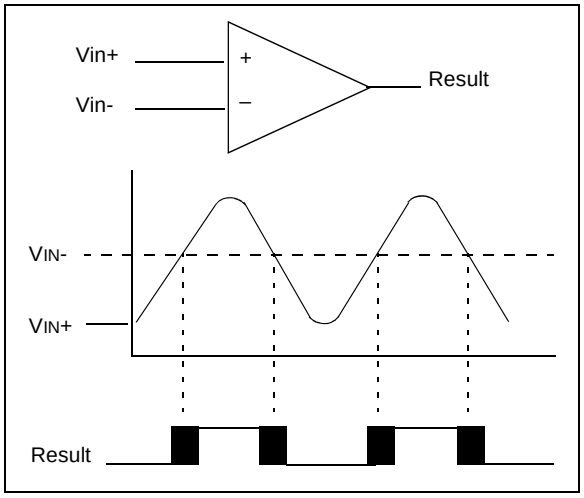
2: When the comparator is turned on, these control bits assert themselves. When the comparator is off, these bits have no effect on the device operation and the other control registers have precedence.

3: PIC10F204/206 only.

8.2 Comparator Operation

A single comparator is shown in Figure 8-2 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 8-2 represent the uncertainty due to input offsets and response time. See Table 12-1 for Common Mode Voltage.

FIGURE 8-2: SINGLE COMPARATOR



8.3 Comparator Reference

An internal reference signal may be used depending on the Comparator Operating mode. The analog signal that is present at VIN- is compared to the signal at VIN+ and the digital output of the comparator is adjusted accordingly (Figure 8-2). Please see Table 12-1 for internal reference specifications.

8.4 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output is to have a valid level. If the comparator inputs are changed, a delay must be used to allow the comparator to settle to its new state. Please see Table 12-1 for comparator response time specifications.

8.5 Comparator Output

The comparator output is read through CMCON0 register. This bit is read-only. The comparator output may also be used internally, see Figure 8-1.

Note:	Analog levels on any pin that is defined as a digital input may cause the input buffer to consume more current than is specified.

8.6 Comparator Wake-up Flag

The comparator wake-up flag is set whenever all of the following conditions are met:

- $\overline{CWU}$ = 0 (CMCON0<0>)
- CMCON0 has been read to latch the last known state of the CMPOUT bit (`MOVF CMCON0, W`)
- Device is in Sleep
- The output of the comparator has changed state

The wake-up flag may be cleared in software or by another device Reset.

8.7 Comparator Operation During Sleep

When the comparator is active and the device is placed in Sleep mode, the comparator remains active. While the comparator is powered-up, higher Sleep currents than shown in the power-down current specification will occur. To minimize power consumption while in Sleep mode, turn off the comparator before entering Sleep.

8.8 Effects of a Reset

A Power-on Reset (POR) forces the CMCON0 register to its Reset state. This forces the comparator module to be in the comparator Reset mode. This ensures that all potential inputs are analog inputs. Device current is minimized when analog inputs are present at Reset time. The comparator will be powered-down during the Reset interval.

8.9 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 8-3. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and VSS. The analog input therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

FIGURE 8-3: ANALOG INPUT MODE

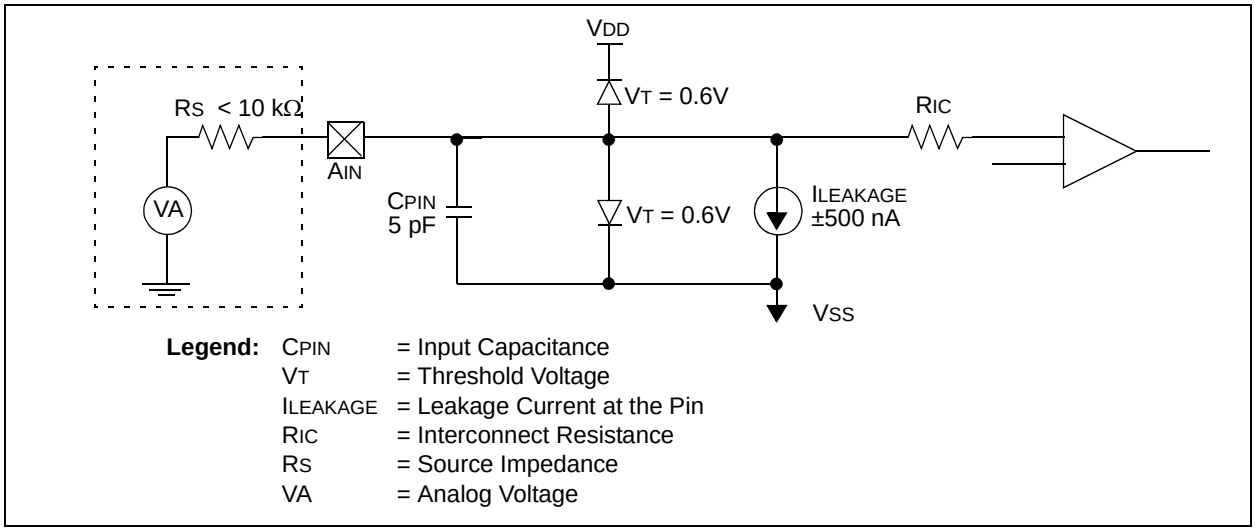


TABLE 8-2: REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other Resets
03h	STATUS	GPWUF	CWUF	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	00-1 1xxx	qq0q quuu
07h	CMCON0	CMPOUT	$\overline{COUTEN}$	POL	$\overline{CMPT0CS}$	CMPON	CNREF	CPREF	$\overline{CWU}$	1111 1111	uuuu uuuu
N/A	TRISGPIO	—	—	—	—	I/O Control Register				---- 1111	---- 1111

Legend: x = Unknown, u = Unchanged, – = Unimplemented, read as '0', q = Depends on condition.

IORWF	Inclusive OR W with f
Syntax:	[*label*] IORWF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(W).OR. (f) → (dest)
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

MOVF	Move f
Syntax:	[*label*] MOVF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(f) → (dest)
Status Affected:	Z
Description:	The contents of register 'f' are moved to destination 'd'. If 'd' is '0', destination is the W register. If 'd' is '1', the destination is file register 'f'. 'd' = 1 is useful as a test of a file register, since status flag Z is affected.

MOVLW	Move literal to W
Syntax:	[*label*] MOVLW k
Operands:	$0 \le k \le 255$
Operation:	k → (W)
Status Affected:	None
Description:	The 8-bit literal 'k' is loaded into the W register. The "don't cares" will assembled as '0's.

MOVWF	Move W to f
Syntax:	[*label*] MOVWF f
Operands:	$0 \le f \le 31$
Operation:	(W) → (f)
Status Affected:	None
Description:	Move data from the W register to register 'f'.

NOP	No Operation
Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.

OPTION	Load OPTION Register
Syntax:	[*label*] OPTION
Operands:	None
Operation:	(W) → Option
Status Affected:	None
Description:	The content of the W register is loaded into the OPTION register.

TRIS	Load TRIS Register
Syntax:	[*label*] TRIS f
Operands:	f = 6
Operation:	(W) → TRIS register f
Status Affected:	None
Description:	TRIS register 'f' (f = 6 or 7) is loaded with the contents of the W register

XORLW	Exclusive OR literal with W
Syntax:	[*label*] XORLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) .XOR. k → (W)
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the 8-bit literal 'k'. The result is placed in the W register.

XORWF	Exclusive OR W with f
Syntax:	[*label*] XORWF f,d
Operands:	0 ≤ f ≤ 31 d ∈ [0,1]
Operation:	(W) .XOR. (f) → (dest)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

11.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

11.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

11.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

11.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

11.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

11.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

12.1 DC Characteristics: PIC10F200/202/204/206 (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +85°C (industrial)				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	2.0		5.5	V	See Figure 12-1
D002	VDR	**RAM Data Retention Voltage(2)**	1.5*	—	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	Vss	—	V	
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	
D010	IDD	**Supply Current(3)**					
			— —	175 0.63	275 1.1	µA mA	VDD = 2.0V VDD = 5.0V
D020	IPD	**Power-down Current(4)**					
			— —	0.1 0.35	1.2 2.4	µA µA	VDD = 2.0V VDD = 5.0V
D022	IWDT	**WDT Current(5)**					
			— —	1.0 7	3 16	µA µA	VDD = 2.0V VDD = 5.0V
D023	ICMP	**Comparator Current(5)**					
			— —	12 44	23 80	µA µA	VDD = 2.0V VDD = 5.0V
D024	IVREF	**Internal Reference Current(5,6)**					
			—	85 175	115 195	µA µA	VDD = 2.0V VDD = 5.0V

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ.") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:
All I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in Sleep mode.

4: Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS.

5: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled.

6: Measured with the comparator enabled.

TABLE 12-6: THERMAL CONSIDERATIONS

Standard Operating Conditions (unless otherwise specified)					
Param. No.	**Sym.**	**Characteristic**	**Typ.**	**Units**	**Conditions**
TH01	θ_{JA}	Thermal Resistance Junction to Ambient	60	°C/W	6-pin SOT-23 package
			80	°C/W	8-pin PDIP package
			90	°C/W	8-pin DFN package
TH02	θ_{JC}	Thermal Resistance Junction to Case	31.4	°C/W	6-pin SOT-23 package
			24	°C/W	8-pin PDIP package
			24	°C/W	8-pin DFN package
TH03	T_{JMAX}	Maximum Junction Temperature	150	°C	
TH04	PD	Power Dissipation	—	W	$PD = P_{INTERNAL} + P_{I/O}$
TH05	$P_{INTERNAL}$	Internal Power Dissipation	—	W	$P_{INTERNAL} = I_{DD} \times V_{DD}$ (1)
TH06	$P_{I/O}$	I/O Power Dissipation	—	W	$P_{I/O} = \Sigma (I_{OL} * V_{OL}) + \Sigma (I_{OH} * (V_{DD} - V_{OH}))$
TH07	P_{DER}	Derated Power	—	W	$P_{DER} = PD_{MAX} (T_J - T_A)/\theta_{JA}$ (2)

Note 1: I_{DD} is current to run the chip alone without driving any load on the output pins.
2: T_A = Ambient Temperature; T_J = Junction Temperature.

13.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified VDD range). This is for **information only** and devices are ensured to operate properly only within the specified range.

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "MAXIMUM", "Max.", "MINIMUM" or "Min." represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.

FIGURE 13-1: IDD vs. VDD OVER FOSC

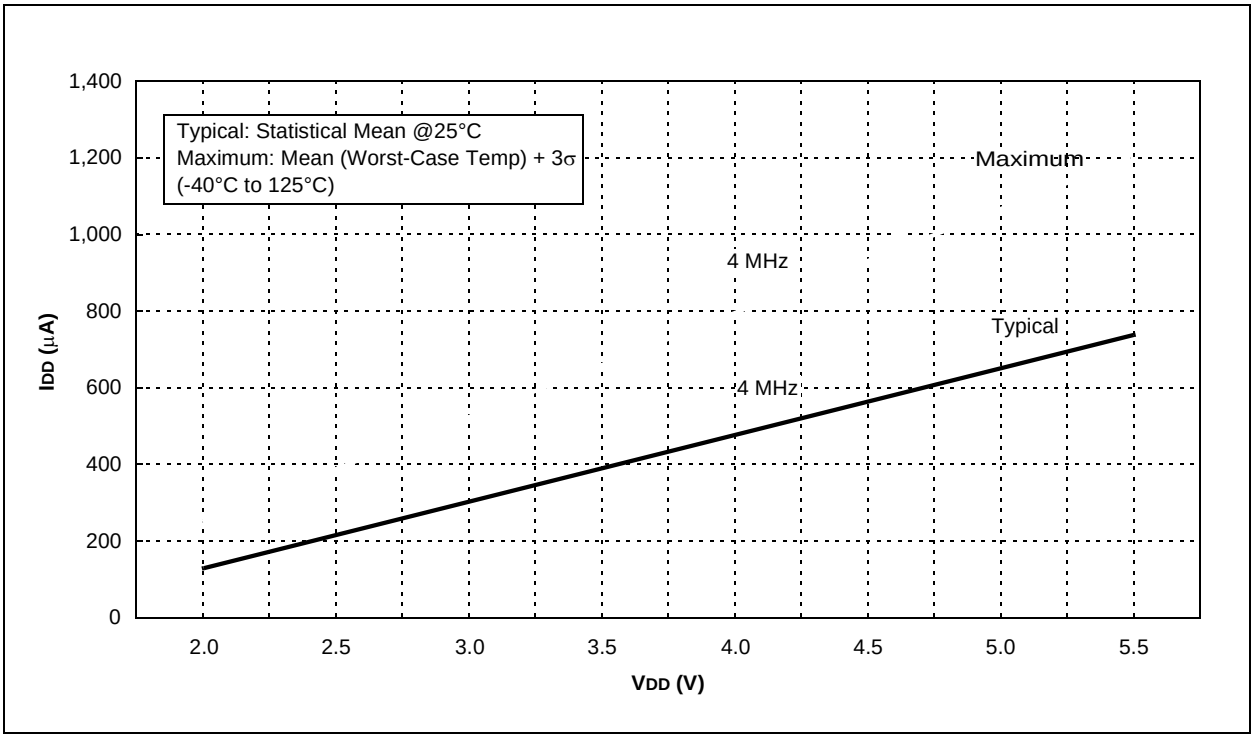


FIGURE 13-12: TTL INPUT THRESHOLD VIN VS. VDD

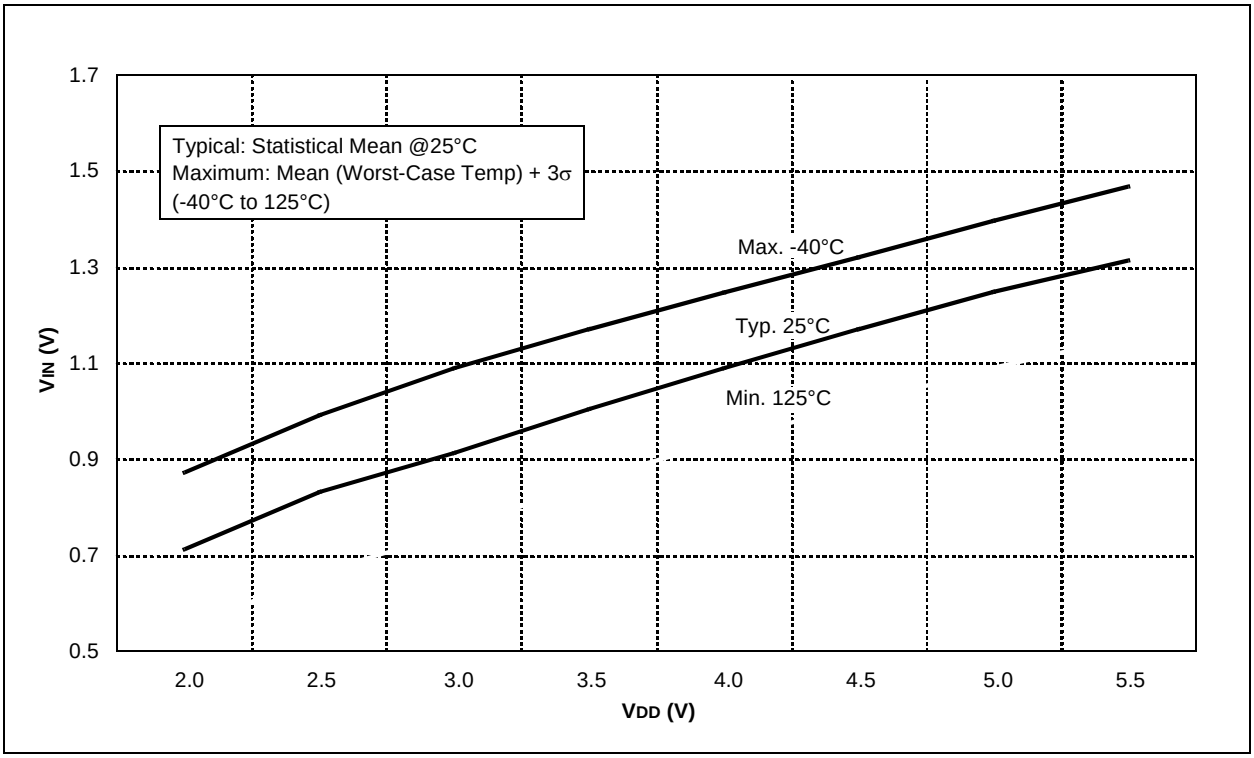
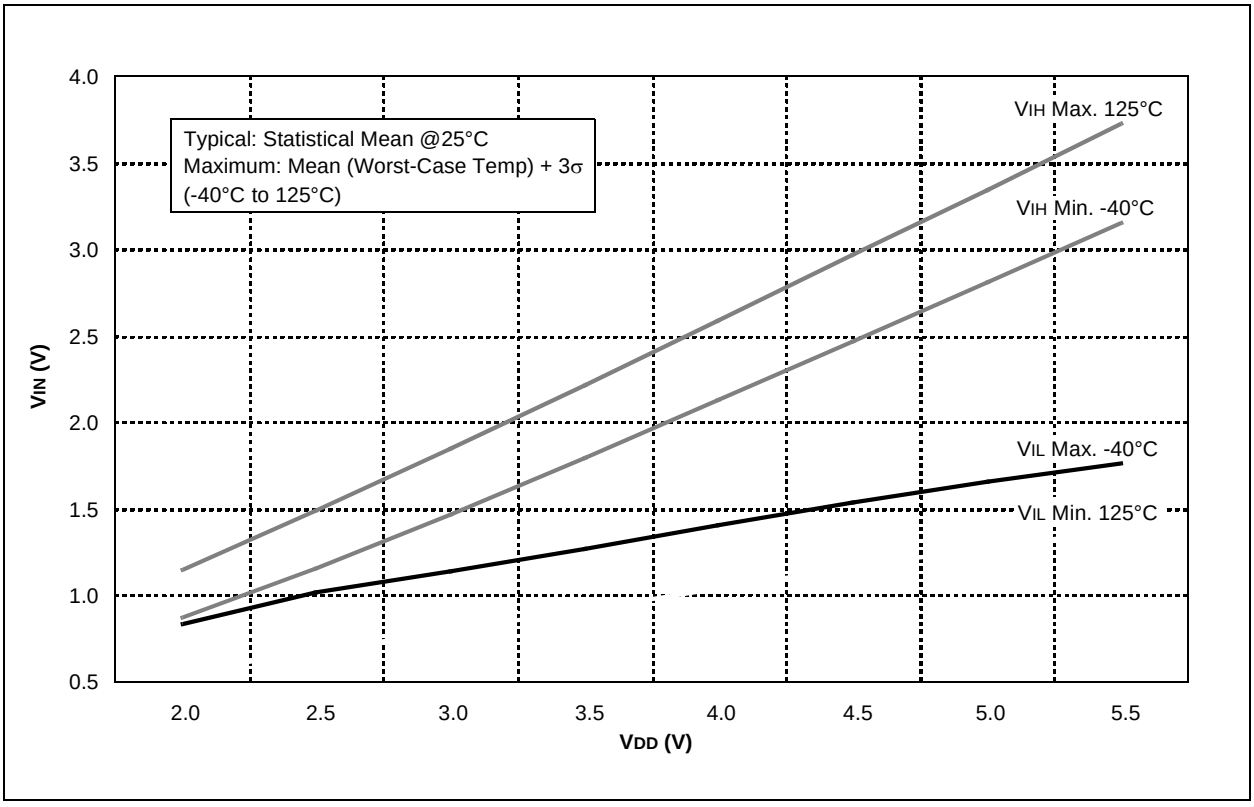


FIGURE 13-13: SCHMITT TRIGGER INPUT THRESHOLD VIN VS. VDD



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