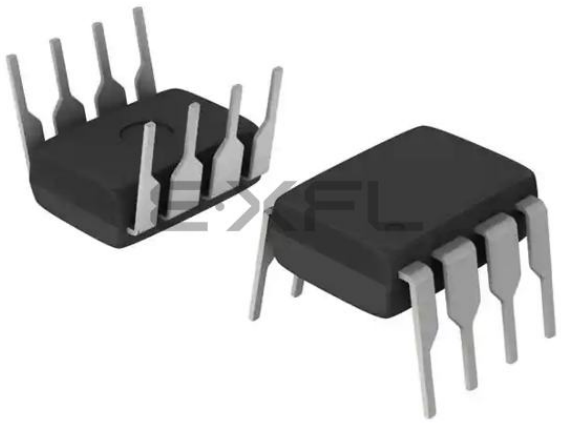

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	3
Program Memory Size	768B (512 x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic10f202-i-p

1.0 GENERAL DESCRIPTION

The PIC10F200/202/204/206 devices from Microchip Technology are low-cost, high-performance, 8-bit, fully-static, Flash-based CMOS microcontrollers. They employ a RISC architecture with only 33 single-word/ single-cycle instructions. All instructions are single cycle (1 μs) except for program branches, which take two cycles. The PIC10F200/202/204/206 devices deliver performance in an order of magnitude higher than their competitors in the same price category. The 12-bit wide instructions are highly symmetrical, resulting in a typical 2:1 code compression over other 8-bit microcontrollers in its class. The easy-to-use and easy to remember instruction set reduces development time significantly.

The PIC10F200/202/204/206 products are equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external Reset circuitry. INTRC Internal Oscillator mode is provided, thereby preserving the limited number of I/O available. Power-Saving Sleep mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The PIC10F200/202/204/206 devices are available in cost-effective Flash, which is suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in Flash programmable microcontrollers, while benefiting from the Flash programmable flexibility.

The PIC10F200/202/204/206 products are supported by a full-featured macro assembler, a software simulator, an in-circuit debugger, a 'C' compiler, a low-cost development programmer and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1 Applications

The PIC10F200/202/204/206 devices fit in applications ranging from personal care appliances and security systems to low-power remote transmitters/receivers. The Flash technology makes customizing application programs (transmitter codes, appliance settings, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make these microcontrollers well suited for applications with space limitations. Low cost, low power, high performance, ease-of-use and I/O flexibility make the PIC10F200/202/204/206 devices very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, logic and PLDs in larger systems and coprocessor applications).

TABLE 1-1: PIC10F200/202/204/206 DEVICES

		PIC10F200	PIC10F202	PIC10F204	PIC10F206
Clock	Maximum Frequency of Operation (MHz)	4	4	4	4
Memory	Flash Program Memory	256	512	256	512
	Data Memory (bytes)	16	24	16	24
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0
	Wake-up from Sleep on Pin Change	Yes	Yes	Yes	Yes
	Comparators	0	0	1	1
Features	I/O Pins	3	3	3	3
	Input-Only Pins	1	1	1	1
	Internal Pull-ups	Yes	Yes	Yes	Yes
	In-Circuit Serial Programming™	Yes	Yes	Yes	Yes
	Number of Instructions	33	33	33	33
	Packages	6-pin SOT-23 8-pin PDIP, DFN	6-pin SOT-23 8-pin PDIP, DFN	6-pin SOT-23 8-pin PDIP, DFN	6-pin SOT-23 8-pin PDIP, DFN

The PIC10F200/202/204/206 devices have Power-on Reset, selectable Watchdog Timer, selectable code-protect, high I/O current capability and precision internal oscillator.
The PIC10F200/202/204/206 devices use serial programming with data pin GP0 and clock pin GP1.

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4.4 STATUS Register

This register contains the arithmetic status of the ALU, the Reset status and the page preselect bit.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS`, will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where u = unchanged).

Therefore, it is recommended that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS register. These instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions which do affect Status bits, see **Section 10.0 "Instruction Set Summary"**.

REGISTER 4-1: STATUS REGISTER

R/W-0	R/W-0	U-1	R-1	R-1	R/W-x	R/W-x	R/W-x
GPWUF	CWUF(1)	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **GPWUF:** GPIO Reset bit
`1` = Reset due to wake-up from Sleep on pin change
`0` = After power-up or other Reset

bit 6 **CWUF:** Comparator Wake-up on Change Flag bit(1)
`1` = Reset due to wake-up from Sleep on comparator change
`0` = After power-up or other Reset conditions.

bit 5 **Reserved:** Do not use. Use of this bit may affect upward compatibility with future products.

bit 4 **$\overline{TO}$:** Time-out bit
`1` = After power-up, `CLRWDT` instruction or `SLEEP` instruction
`0` = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Borrow}$ bit (for `ADDWF` and `SUBWF` instructions)
`ADDWF`:
`1` = A carry from the 4th low-order bit of the result occurred
`0` = A carry from the 4th low-order bit of the result did not occur
`SUBWF`:
`1` = A borrow from the 4th low-order bit of the result did not occur
`0` = A borrow from the 4th low-order bit of the result occurred

bit 0 **C:** Carry/$\overline{Borrow}$ bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)

`ADDWF`:	`SUBWF`:	`RRF` or `RLF`:
`1` = A carry occurred	`1` = A borrow did not occur	Load bit with LSb or MSb, respectively
`0` = A carry did not occur	`0` = A borrow occurred	

Note 1: This bit is used on the PIC10F204/206. For code compatibility do not use this bit on the PIC10F200/202.

4.7 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

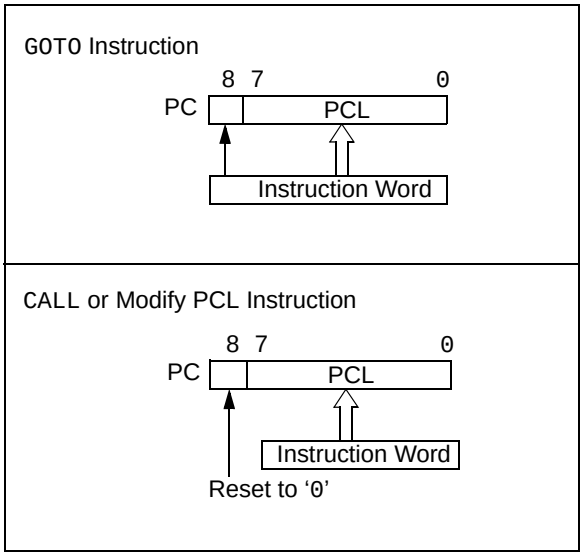
For a GOTO instruction, bits 8-0 of the PC are provided by the GOTO instruction word. The Program Counter Low (PCL) is mapped to PC<7:0>.

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-5).

Instructions where the PCL is the destination, or modify PCL instructions, include MOVWF PC, ADDWF PC and BSF PC,5.

Note:	Because PC<8> is cleared in the CALL instruction or any modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-5: LOADING OF PC BRANCH INSTRUCTIONS



4.7.1 EFFECTS OF RESET

The PC is set upon a Reset, which means that the PC addresses the last location in program memory (i.e., the oscillator calibration instruction). After executing MOVLW XX, the PC will roll over to location 0000h and begin executing user code.

4.8 Stack

The PIC10F200/204 devices have a 2-deep, 8-bit wide hardware PUSH/POP stack.

The PIC10F202/206 devices have a 2-deep, 9-bit wide hardware PUSH/POP stack.

A CALL instruction will PUSH the current value of Stack 1 into Stack 2 and then PUSH the current PC value, incremented by one, into Stack Level 1. If more than two sequential CALLs are executed, only the most recent two return addresses are stored.

A RETLW instruction will POP the contents of Stack Level 1 into the PC and then copy Stack Level 2 contents into level 1. If more than two sequential RETLWs are executed, the stack will be filled with the address previously stored in Stack Level 2.

Note 1:	The W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of the data look-up tables within the program memory.
2:	There are no Status bits to indicate stack overflows or stack underflow conditions.
3:	There are no instruction mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL and RETLW instructions.

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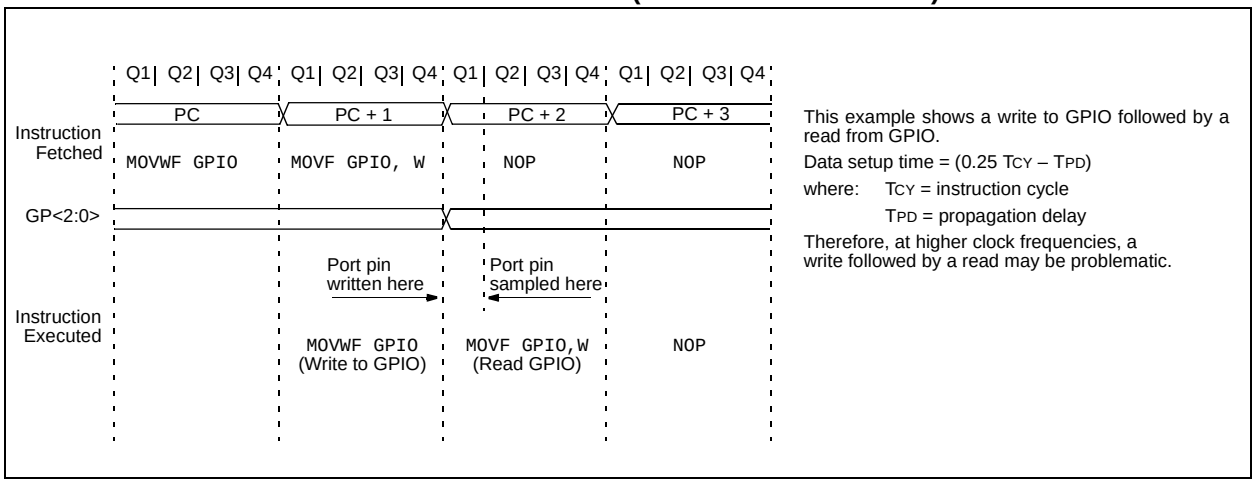
FIGURE 5-2: SUCCESSIVE I/O OPERATION (PIC10F200/202/204/206)



This example shows a write to GPIO followed by a read from GPIO.

Data setup time = (0.25 T_{CY} – T_{PD})

where: T_{CY} = instruction cycle

T_{PD} = propagation delay

Therefore, at higher clock frequencies, a write followed by a read may be problematic.

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6.0 TIMER0 MODULE AND TMR0 REGISTER (PIC10F200/202)

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select:
  - Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

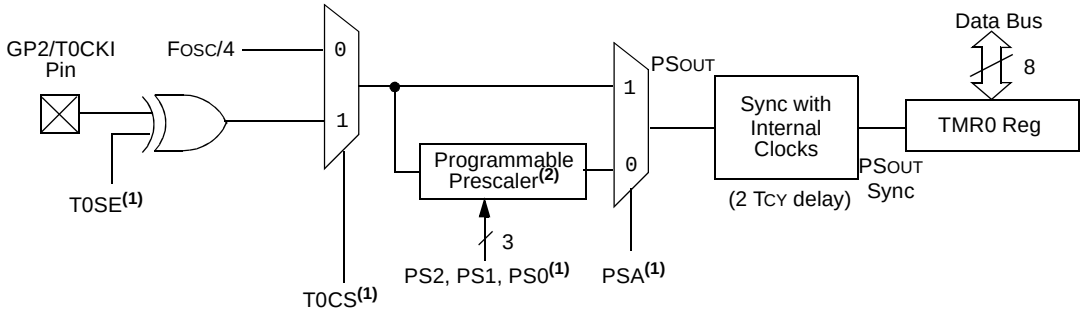
Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in **Section 6.1 "Using Timer0 with an External Clock (PIC10F200/202)"**.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit, PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, 1:256 are selectable. **Section 6.2 "Prescaler"** details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 6-1.

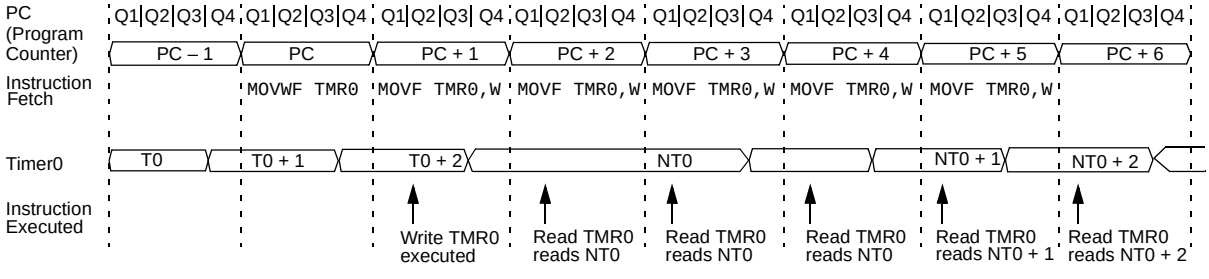
FIGURE 6-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.

2: The prescaler is shared with the Watchdog Timer (Figure 6-5).

FIGURE 6-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE



7.0 TIMER0 MODULE AND TMR0 REGISTER (PIC10F204/206)

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select:
  - Edge select for external clock
  - External clock from either the T0CKI pin or from the output of the comparator

Figure 7-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 7-2 and Figure 7-3). The user can work around this by writing an adjusted value to the TMR0 register.

There are two types of Counter mode. The first Counter mode uses the T0CKI pin to increment Timer0. It is selected by setting the T0CS bit (OPTION<5>), setting the CMPT0CS bit (CMCON0<4>) and setting the COUTEN bit (CMCON0<6>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in **Section 7.1 "Using Timer0 with an External Clock (PIC10F204/206)"**.

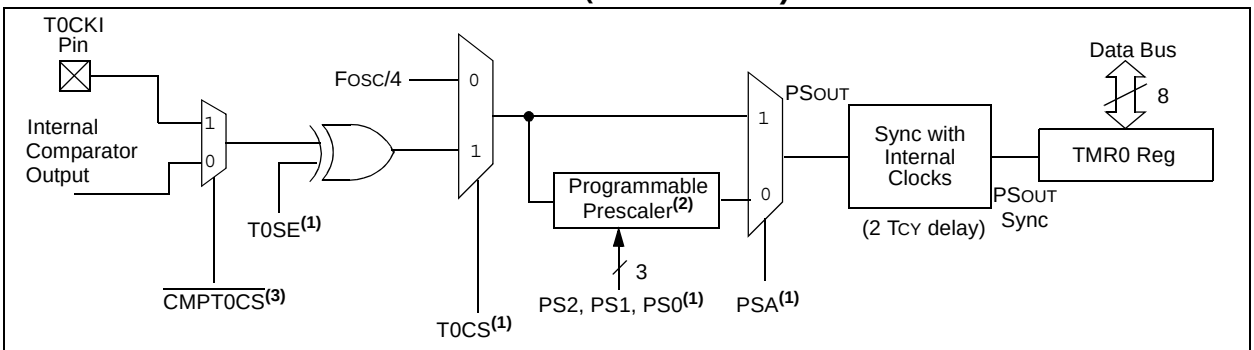
The second Counter mode uses the output of the comparator to increment Timer0. It can be entered in two different ways. The first way is selected by setting the T0CS bit (OPTION<5>) and clearing the CMPT0CS bit (CMCON<4>); (COUTEN [CMCON<6>]) does not affect this mode of operation. This enables an internal connection between the comparator and the Timer0.

The second way is selected by setting the T0CS bit (OPTION<5>), setting the CMPT0CS bit (CMCON0<4>) and clearing the COUTEN bit (CMCON0<6>). This allows the output of the comparator onto the T0CKI pin, while keeping the T0CKI input active. Therefore, any comparator change on the COUT pin is fed back into the T0CKI input. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input as discussed in **Section 7.1 "Using Timer0 with an External Clock (PIC10F204/206)"**

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit, PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. **Section 7.2 "Prescaler"** details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 7-1.

FIGURE 7-1: TIMER0 BLOCK DIAGRAM (PIC10F204/206)



Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.
2: The prescaler is shared with the Watchdog Timer (Figure 7-5).
3: Bit CMPT0CS is located in the CMCON0 register, CMCON0<4>.

FIGURE 9-2: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

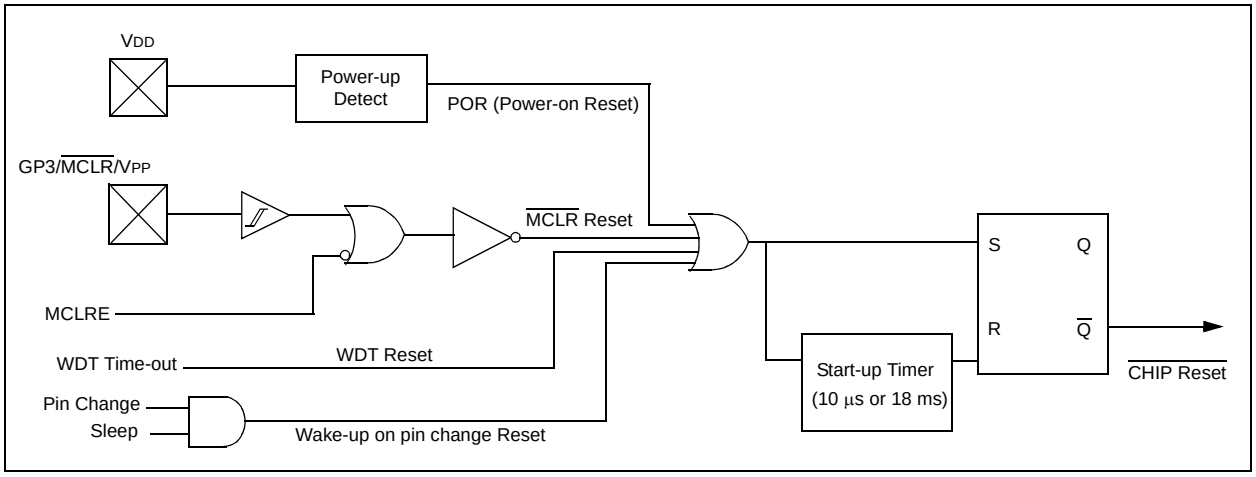


FIGURE 9-3: TIME-OUT SEQUENCE ON POWER-UP (MCLR PULLED LOW)

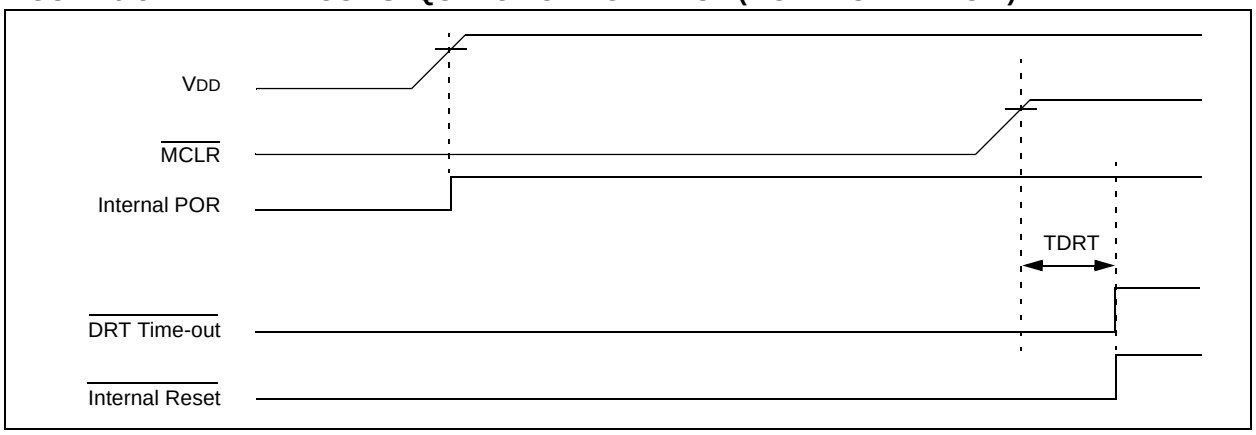
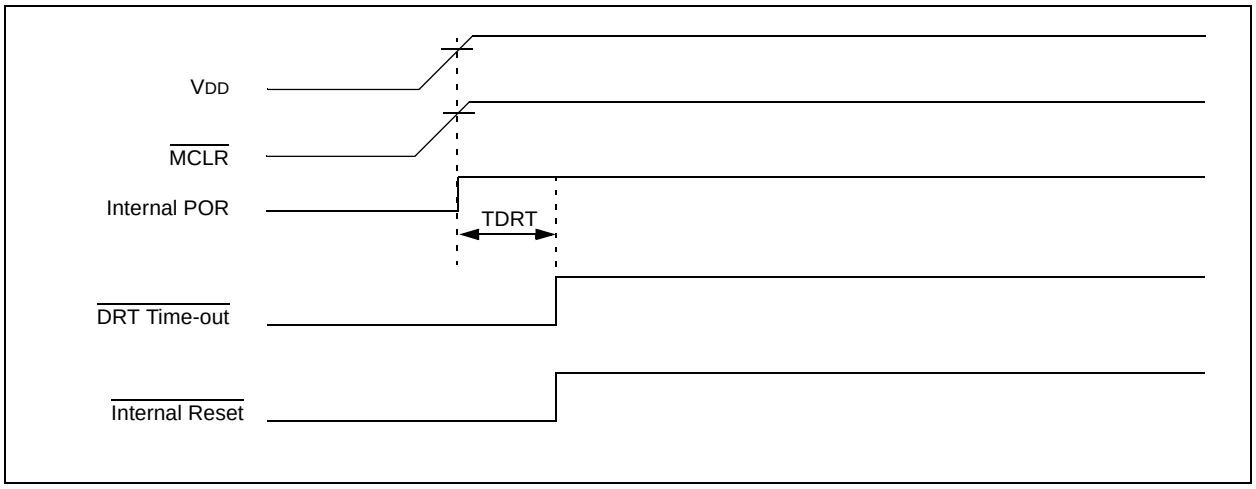


FIGURE 9-4: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): FAST VDD RISE TIME



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9.5 Device Reset Timer (DRT)

On the PIC10F200/202/204/206 devices, the DRT runs any time the device is powered-up.

The DRT operates on an internal oscillator. The processor is kept in Reset as long as the DRT is active. The DRT delay allows VDD to rise above VDD min. and for the oscillator to stabilize.

The on-chip DRT keeps the devices in a Reset condition for approximately 18 ms after MCLR has reached a logic high (VIH MCLR) level. Programming GP3/MCLR/VPP as MCLR and using an external RC network connected to the MCLR input is not required in most cases. This allows savings in cost-sensitive and/or space restricted applications, as well as allowing the use of the GP3/MCLR/VPP pin as a general purpose input.

The Device Reset Time delays will vary from chip-to-chip due to VDD, temperature and process variation. See AC parameters for details.

Reset sources are POR, MCLR, WDT time-out and wake-up on pin change. See **Section 9.9.2 "Wake-up from Sleep"**, Notes 1, 2 and 3.

TABLE 9-3: DRT PERIOD

Oscillator	POR Reset	Subsequent Resets
INTOSC	18 ms (typical)	10 µs (typical)

9.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator, which does not require any external components. This RC oscillator is separate from the internal 4 MHz oscillator. This means that the WDT will run even if the main processor clock has been stopped, for example, by execution of a SLEEP instruction. During normal operation or Sleep, a WDT Reset or wake-up Reset, generates a device Reset.

The TO bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset.

The WDT can be permanently disabled by programming the configuration WDTE as a '0' (see **Section 9.1 "Configuration Bits"**). Refer to the PIC10F200/202/204/206 Programming Specifications to determine how to access the Configuration Word.

9.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, a time-out period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

Under worst-case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

9.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device Reset.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum Sleep time before a WDT wake-up Reset.

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9.7 Time-out Sequence, Power-down and Wake-up from Sleep Status Bits (TO, PD, GPWUF, CWUF)

The $\overline{TO}$, $\overline{PD}$, GPWUF and CWUF bits in the STATUS register can be tested to determine if a Reset condition has been caused by a power-up condition, a $\overline{MCLR}$, Watchdog Timer (WDT) Reset, wake-up on comparator change or wake-up on pin change.

TABLE 9-5: $\overline{TO}$, $\overline{PD}$, GPWUF, CWUF STATUS AFTER RESET

CWUF	GPWUF	$\overline{TO}$	$\overline{PD}$	Reset Caused By
0	0	0	0	WDT wake-up from Sleep
0	0	0	u	WDT time-out (not from Sleep)
0	0	1	0	$\overline{MCLR}$ wake-up from Sleep
0	0	1	1	Power-up
0	0	u	u	$\overline{MCLR}$ not during Sleep
0	1	1	0	Wake-up from Sleep on pin change
1	0	1	0	Wake-up from Sleep on comparator change

Legend: u = unchanged, x = unknown, – = unimplemented bit, read as '0', q = value depends on condition.

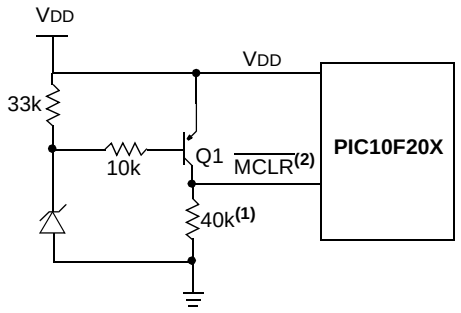
Note 1: The $\overline{TO}$, $\overline{PD}$, GPWUF and CWUF bits maintain their status (u) until a Reset occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{TO}$, $\overline{PD}$, GPWUF or CWUF Status bits.

9.8 Reset on Brown-out

A Brown-out Reset is a condition where device power (V_{DD}) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

To reset PIC10F200/202/204/206 devices when a Brown-out Reset occurs, external brown-out protection circuits may be built, as shown in Figure 9-7 and Figure 9-8.

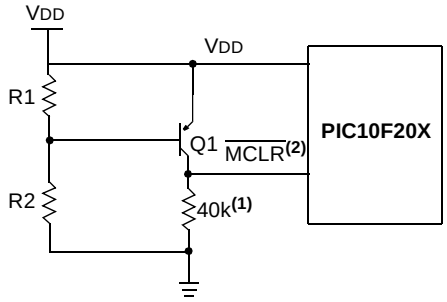
FIGURE 9-7: BROWN-OUT PROTECTION CIRCUIT 1



Note 1: This circuit will activate Reset when V_{DD} goes below Vz + 0.7V (where Vz = Zener voltage).

2: Pin must be confirmed as $\overline{MCLR}$.

FIGURE 9-8: BROWN-OUT PROTECTION CIRCUIT 2



Note 1: This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when V_{DD} is below a certain level such that:

$$V_{DD} \bullet \frac{R1}{R1 + R2} = 0.7V$$

2: Pin must be confirmed as $\overline{MCLR}$.

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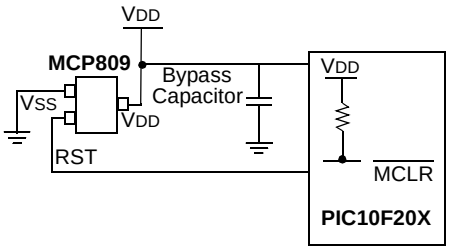
FIGURE 9-9: BROWN-OUT PROTECTION CIRCUIT 3



Note: This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. There are seven different trip point selections to accommodate 5V to 3V systems.

9.9 Power-down Mode (Sleep)

A device may be powered-down (Sleep) and later powered-up (wake-up from Sleep).

9.9.1 SLEEP

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (STATUS<4>) is set, the $\overline{PD}$ bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low or high-impedance).

Note: A Reset generated by a WDT time-out does not drive the $\overline{MCLR}$ pin low.

For lowest current consumption while powered-down, the T0CKI input should be at VDD or VSS and the GP3/$\overline{MCLR}$/VPP pin must be at a logic high level if $\overline{MCLR}$ is enabled.

9.9.2 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

1. An external Reset input on GP3/$\overline{MCLR}$/VPP pin, when configured as $\overline{MCLR}$.
2. A Watchdog Timer time-out Reset (if WDT was enabled).
3. A change on input pin GP0, GP1 or GP3 when wake-up on change is enabled.
4. A comparator output change has occurred when wake-up on comparator change is enabled.

These events cause a device Reset. The $\overline{TO}$, $\overline{PD}$ GPWUF and CWUF bits can be used to determine the cause of device Reset. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The GPWUF bit indicates a change in state while in Sleep at pins GP0, GP1 or GP3 (since the last file or bit operation on GP port). The CWUF bit indicates a change in the state while in Sleep of the comparator output.

Caution: Right before entering Sleep, read the input pins. When in Sleep, wake-up occurs when the values at the pins change from the state they were in at the last reading. If a wake-up on change occurs and the pins are not read before re-entering Sleep, a wake-up will occur immediately even if no pins change while in Sleep mode.

Note: The WDT is cleared when the device wakes from Sleep, regardless of the wake-up source.

TABLE 10-2: INSTRUCTION SET SUMMARY

Mnemonic, Operands		Description	Cycles	12-Bit Opcode			Status Affected	Notes
				MSb		LSb		
ADDWF	f, d	Add W and f	1	0001	11df	ffff	C, DC, Z	**1, 2, 4**
ANDWF	f, d	AND W with f	1	0001	01df	ffff	Z	**2, 4**
CLRF	f	Clear f	1	0000	011f	ffff	Z	**4**
CLRW	—	Clear W	1	0000	0100	0000	Z	
COMF	f, d	Complement f	1	0010	01df	ffff	Z	
DECF	f, d	Decrement f	1	0000	11df	ffff	Z	**2, 4**
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	0010	11df	ffff	None	**2, 4**
INCF	f, d	Increment f	1	0010	10df	ffff	Z	**2, 4**
INCFSZ	f, d	Increment f, Skip if 0	1(2)	0011	11df	ffff	None	**2, 4**
IORWF	f, d	Inclusive OR W with f	1	0001	00df	ffff	Z	**2, 4**
MOVF	f, d	Move f	1	0010	00df	ffff	Z	**2, 4**
MOVWF	f	Move W to f	1	0000	001f	ffff	None	**1, 4**
NOP	—	No Operation	1	0000	0000	0000	None	
RLF	f, d	Rotate left f through Carry	1	0011	01df	ffff	C	**2, 4**
RRF	f, d	Rotate right f through Carry	1	0011	00df	ffff	C	**2, 4**
SUBWF	f, d	Subtract W from f	1	0000	10df	ffff	C, DC, Z	**1, 2, 4**
SWAPF	f, d	Swap f	1	0011	10df	ffff	None	**2, 4**
XORWF	f, d	Exclusive OR W with f	1	0001	10df	ffff	Z	**2, 4**
BIT-ORIENTED FILE REGISTER OPERATIONS								
BCF	f, b	Bit Clear f	1	0100	bbbf	ffff	None	**2, 4**
BSF	f, b	Bit Set f	1	0101	bbbf	ffff	None	**2, 4**
BTFSC	f, b	Bit Test f, Skip if Clear	1(2)	0110	bbbf	ffff	None	
BTFSS	f, b	Bit Test f, Skip if Set	1(2)	0111	bbbf	ffff	None	
LITERAL AND CONTROL OPERATIONS								
ANDLW	k	AND literal with W	1	1110	kkkk	kkkk	Z	
CALL	k	Call Subroutine	2	1001	kkkk	kkkk	None	**1**
CLRWDT		Clear Watchdog Timer	1	0000	0000	0100	$\overline{TO}$, $\overline{PD}$	
GOTO	k	Unconditional branch	2	101k	kkkk	kkkk	None	
IORLW	k	Inclusive OR literal with W	1	1101	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	1100	kkkk	kkkk	None	
OPTION	—	Load OPTION register	1	0000	0000	0010	None	
RETLW	k	Return, place Literal in W	2	1000	kkkk	kkkk	None	
SLEEP	—	Go into Standby mode	1	0000	0000	0011	$\overline{TO}$, $\overline{PD}$	
TRIS	f	Load TRIS register	1	0000	0000	0fff	None	**3**
XORLW	k	Exclusive OR literal to W	1	1111	kkkk	kkkk	Z	

Note 1: The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for GOTO. See **Section 4.7 "Program Counter"**.

2: When an I/O register is modified as a function of itself (e.g. MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

3: The instruction TRIS f, where f = 6, causes the contents of the W register to be written to the tri-state latches of PORTB. A '1' forces the pin to a high-impedance state and disables the output buffers.

4: If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared (if assigned to TMR0).

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ADDWF	Add W and f
Syntax:	[*label*] ADDWF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(W) + (f) → (dest)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register and register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

ANDLW	AND literal with W
Syntax:	[*label*] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W).AND. (k) → (W)
Status Affected:	Z
Description:	The contents of the W register are AND'ed with the 8-bit literal 'k'. The result is placed in the W register.

ANDWF	AND W with f
Syntax:	[*label*] ANDWF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(W) .AND. (f) → (dest)
Status Affected:	Z
Description:	The contents of the W register are AND'ed with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	$0 \le f \le 31$ $0 \le b \le 7$
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	Bit Set f
Syntax:	[*label*] BSF f,b
Operands:	$0 \le f \le 31$ $0 \le b \le 7$
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

BTFSC	Bit Test f, Skip if Clear
Syntax:	[*label*] BTFSC f,b
Operands:	$0 \le f \le 31$ $0 \le b \le 7$
Operation:	skip if (f<b>) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', then the next instruction is skipped. If bit 'b' is '0', then the next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a 2-cycle instruction.

RETLW **Return with literal in W**

Syntax: [*label*] RETLW k

Operands: $0 \le k \le 255$

Operation: $k \rightarrow (W)$;
$TOS \rightarrow PC$

Status Affected: None

Description: The W register is loaded with the 8-bit literal ‘k’. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.

RLF **Rotate Left f through Carry**

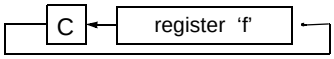
Syntax: [*label*] RLF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register ‘f’ are rotated one bit to the left through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.



RRF **Rotate Right f through Carry**

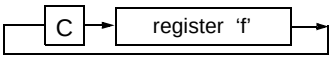
Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register ‘f’ are rotated one bit to the right through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.



SLEEP **Enter SLEEP Mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: $00h \rightarrow WDT$;
$0 \rightarrow$ WDT prescaler;
$1 \rightarrow \overline{TO}$;
$0 \rightarrow \overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$, RBWUF

Description: Time-out Status bit ($\overline{TO}$) is set. The Power-down Status bit ($\overline{PD}$) is cleared.

RBWUF is unaffected.

The WDT and its prescaler are cleared.

The processor is put into Sleep mode with the oscillator stopped. See **Section 9.9 “Power-down Mode (Sleep)”** for more details.

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(f) - (W) \rightarrow (dest)$

Status Affected: C, DC, Z

Description: Subtract (2’s complement method) the W register from register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(f<3:0>) \rightarrow (dest<7:4>)$;
$(f<7:4>) \rightarrow (dest<3:0>)$

Status Affected: None

Description: The upper and lower nibbles of register ‘f’ are exchanged. If ‘d’ is ‘0’, the result is placed in W register. If ‘d’ is ‘1’, the result is placed in register ‘f’.

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11.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

11.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

11.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

11.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

11.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

FIGURE 13-4: COMPARATOR IPD vs. VDD (COMPARATOR ENABLED)

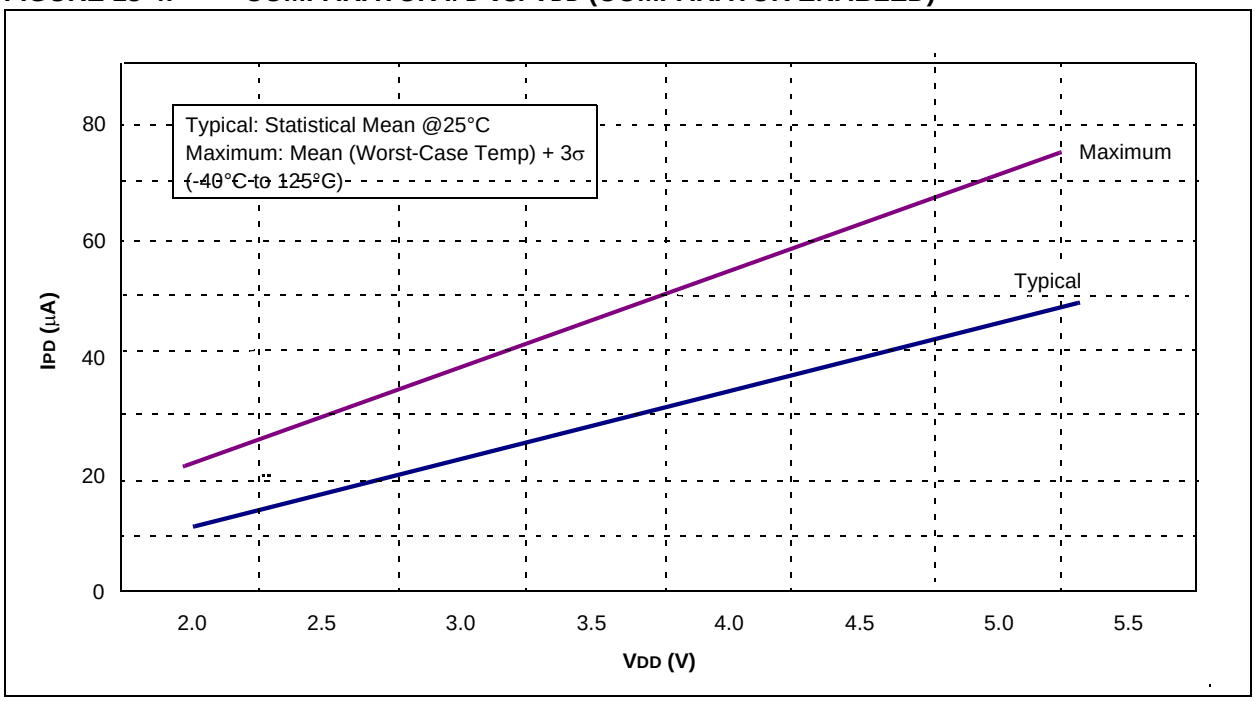


FIGURE 13-5: TYPICAL WDT IPD vs. VDD

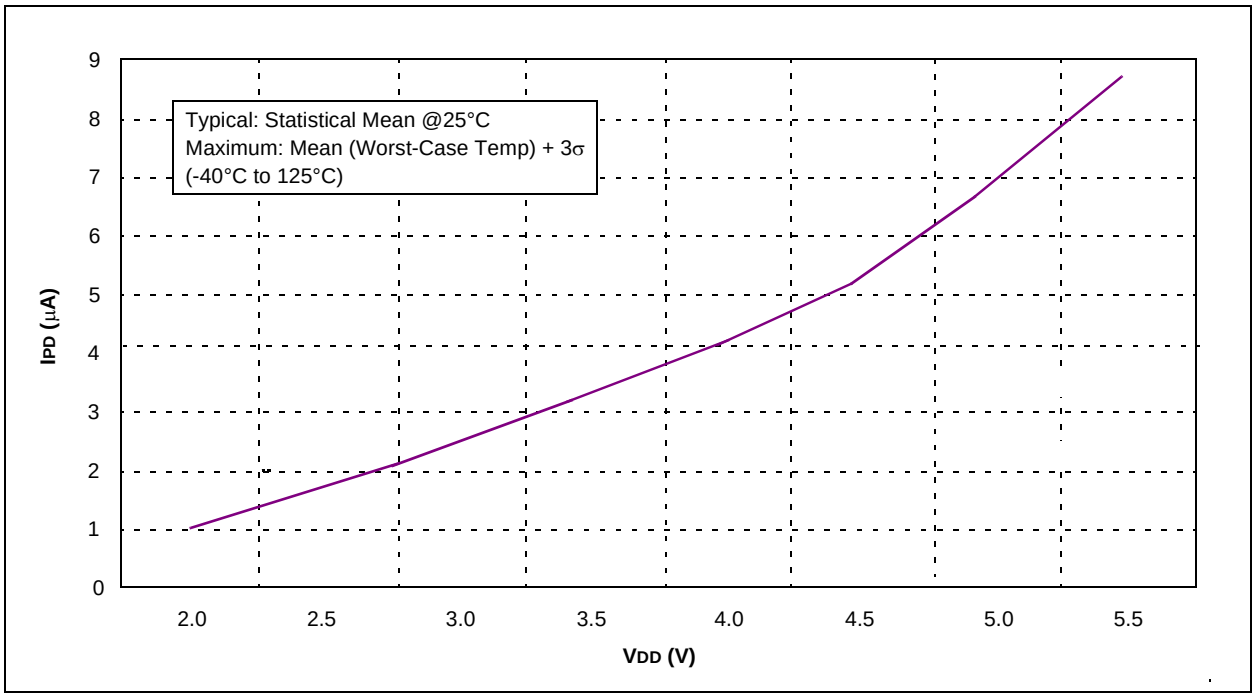


FIGURE 13-8: VOL vs. IOL OVER TEMPERATURE (VDD = 3.0V)

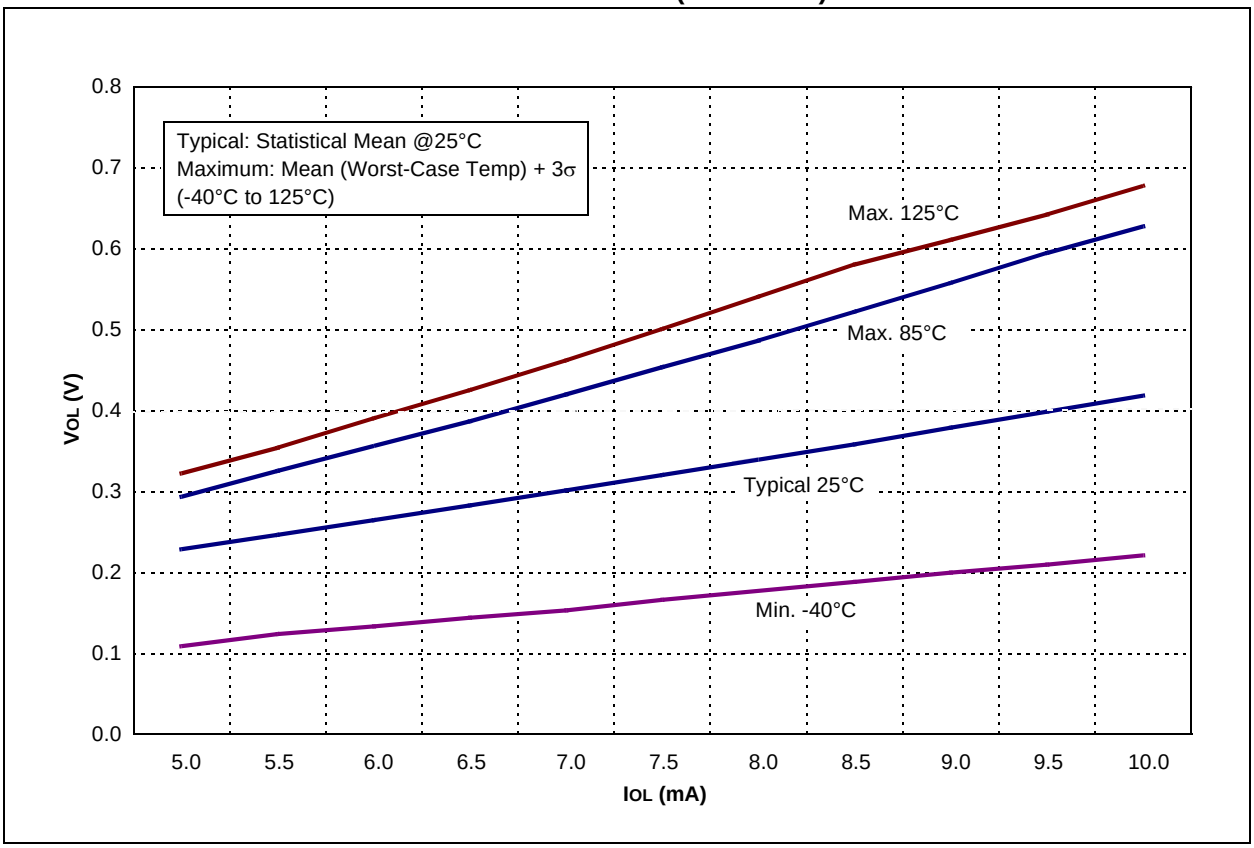


FIGURE 13-9: VOL vs. IOL OVER TEMPERATURE (VDD = 5.0V)

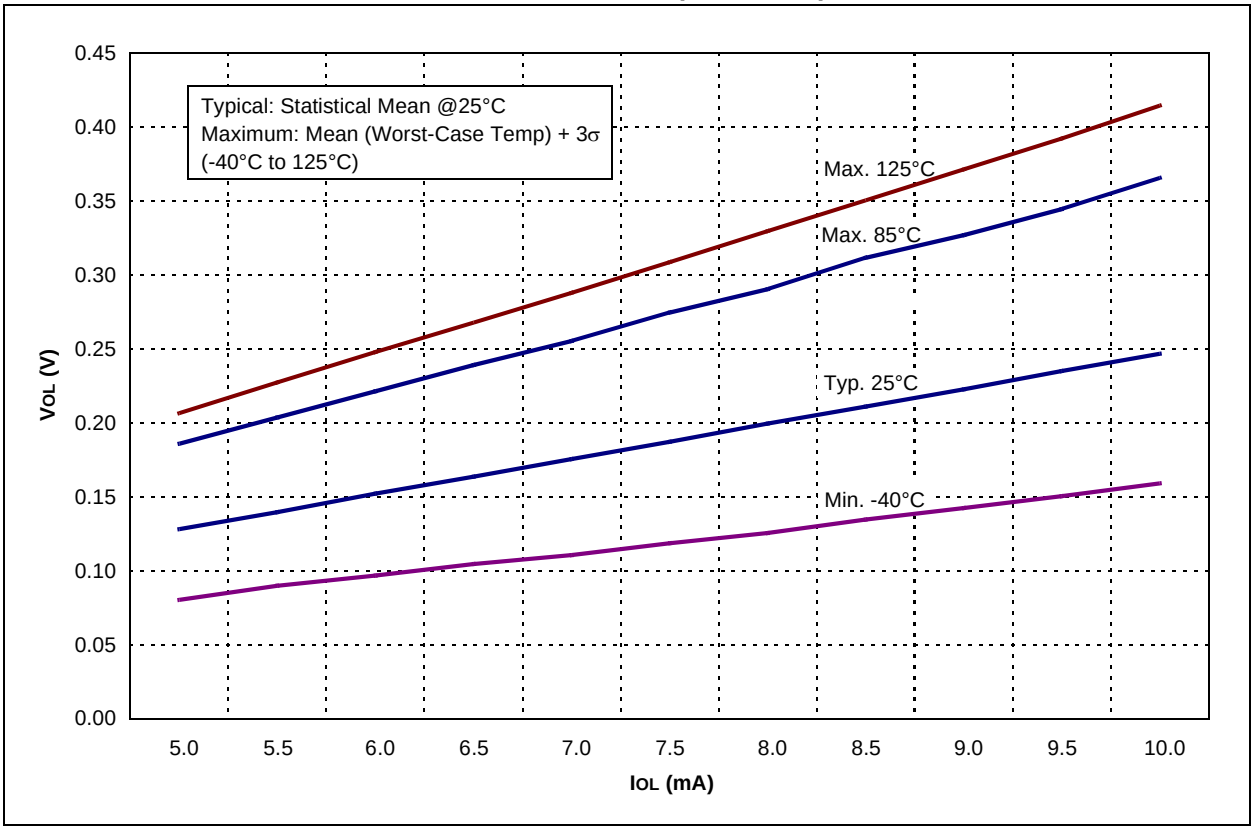


TABLE 14-1: 8-LEAD 2x3 DFN (MC) PACKAGE TOP MARKING

Part Number	Marking
PIC10F200-I/MC	BA0
PIC10F200-E/MC	BB0
PIC10F202-I/MC	BC0
PIC10F202-E/MC	BD0
PIC10F204-I/MC	BE0
PIC10F204-E/MC	BF0
PIC10F206-I/MC	BG0
PIC10F206-E/MC	BH0

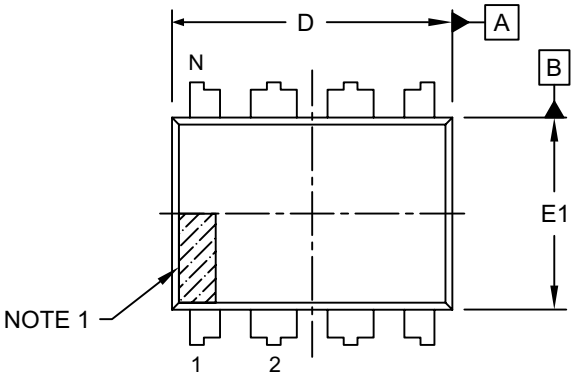
TABLE 14-2: 6-LEAD SOT-23 (OT) PACKAGE TOP MARKING

Part Number	Marking
PIC10F200-I/OT	00NN
PIC10F200-E/OT	00NN
PIC10F202-I/OT	02NN
PIC10F202-E/OT	02NN
PIC10F204-I/OT	04NN
PIC10F204-E/OT	04NN
PIC10F206-I/OT	06NN
PIC10F206-E/OT	06NN

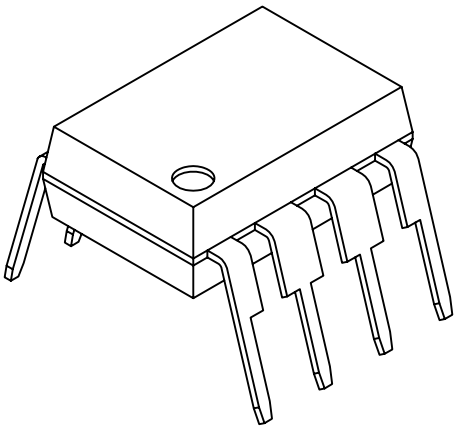
Note: NN represents the alphanumeric traceability code.

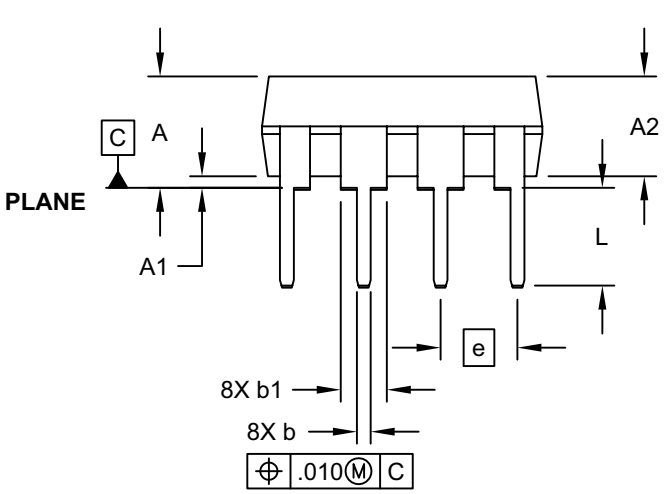
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

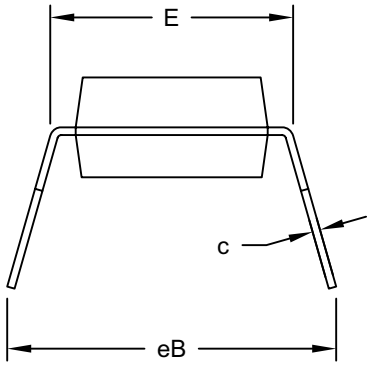


TOP VIEW





SIDE VIEW



END VIEW

Microchip Technology Drawing No. C04-018D Sheet 1 of 2

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