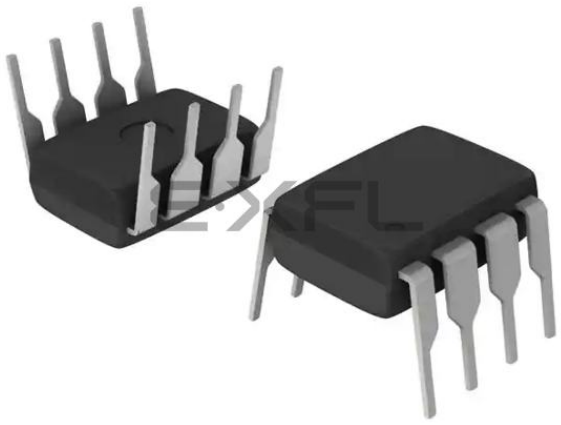

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	3
Program Memory Size	384B (256 x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic10f204-i-p

2.0 PIC10F200/202/204/206 DEVICE VARIETIES

A variety of packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC10F200/202/204/206 Product Identification System at the back of this data sheet to specify the correct part number.

2.1 Quick Turn Programming (QTP) Devices

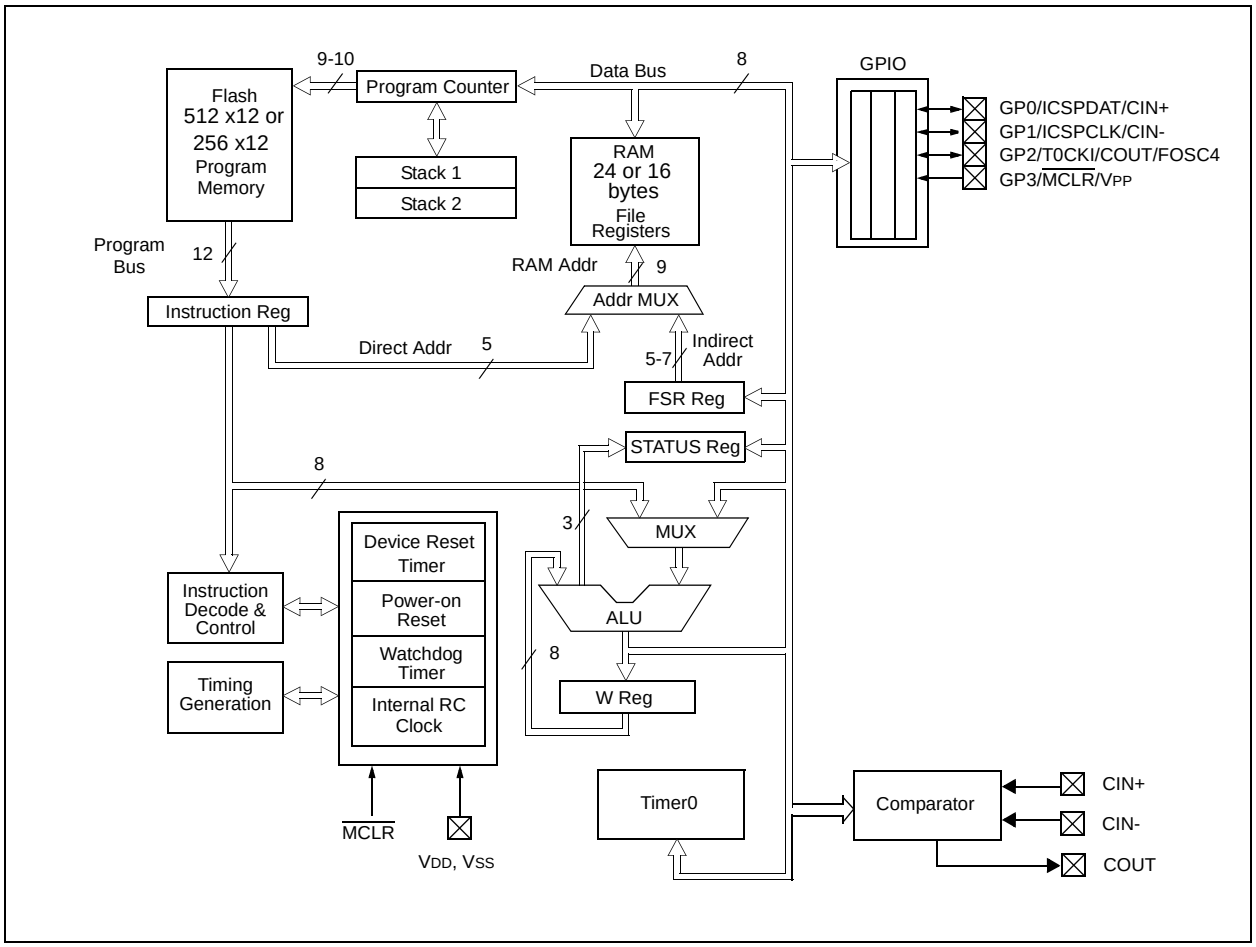
Microchip offers a QTP programming service for factory production orders. This service is made available for users who choose not to program medium-to-high quantity units and whose code patterns have stabilized. The devices are identical to the Flash devices but with all Flash locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

2.2 Serialized Quick Turn Programming^{SM} (SQTP^{SM}) Devices

Microchip offers a unique programming service, where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number, which can serve as an entry code, password or ID number.

FIGURE 3-2: PIC10F204/206 BLOCK DIAGRAM



4.3.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The Special Function Registers can be classified into two sets. The Special Function Registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTER (SFR) SUMMARY (PIC10F200/202/204/206)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset(2)	Register on Page
00h	INDF	Uses Contents of FSR to Address Data Memory (not a physical register)								xxxx xxxx	19
01h	TMR0	8-bit Real-Time Clock/Counter								xxxx xxxx	23, 27
02h(1)	PCL	Low-order 8 bits of PC								1111 1111	18
03h	STATUS	GPWUF	CWUF(5)	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	00-1 1xxx(3)	15
04h	FSR	Indirect Data Memory Address Pointer								111x xxxx	19
05h	OSCCAL	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	FOSC4	1111 1110	17
06h	GPIO	—	—	—	—	GP3	GP2	GP1	GP0	---- xxxx	20
07h(4)	CMCON0	CMPOUT	$\overline{COUTEN}$	POL	$\overline{CMPT0CS}$	CMPON	CNREF	CPREF	$\overline{CWU}$	1111 1111	28
N/A	TRISGPIO	—	—	—	—	I/O Control Register				---- 1111	31
N/A	OPTION	$\overline{GPWU}$	$\overline{GPPU}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	16

Legend: – = unimplemented, read as '0', x = unknown, u = unchanged, q = value depends on condition.

Note 1: The upper byte of the Program Counter is not directly accessible. See **Section 4.7 "Program Counter"** for an explanation of how to access these bits.

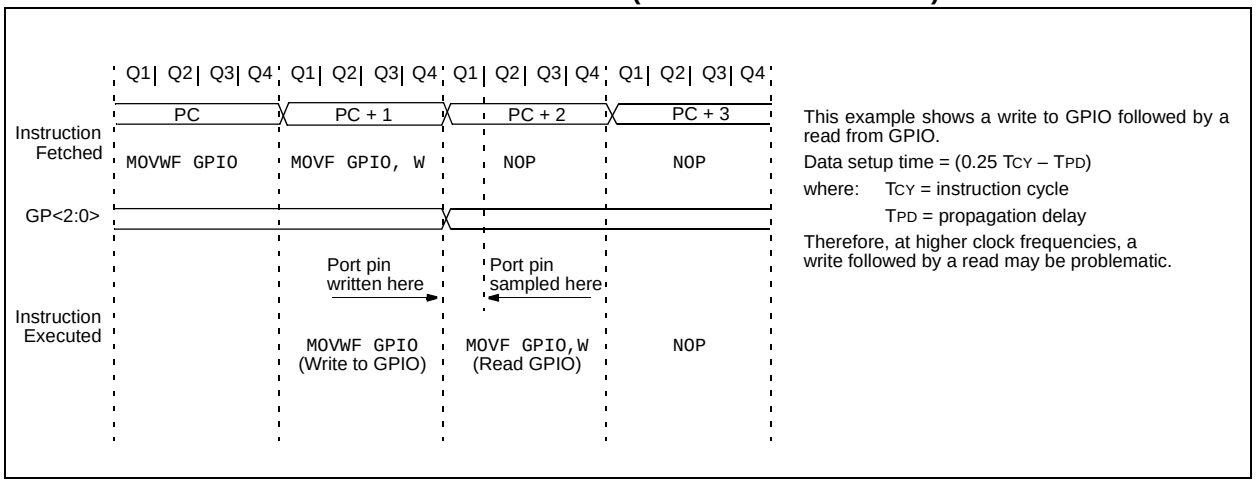
2: Other (non Power-up) Resets include external Reset through $\overline{MCLR}$, Watchdog Timer and wake-up on pin change Reset.

3: See Table 9-1 for other Reset specific values.

4: PIC10F204/206 only.

5: PIC10F204/206 only. On all other devices, this bit is reserved and should not be used.

FIGURE 5-2: SUCCESSIVE I/O OPERATION (PIC10F200/202/204/206)



This example shows a write to GPIO followed by a read from GPIO.

Data setup time = (0.25 T_{CY} – T_{PD})

where: T_{CY} = instruction cycle

T_{PD} = propagation delay

Therefore, at higher clock frequencies, a write followed by a read may be problematic.

6.0 TIMER0 MODULE AND TMR0 REGISTER (PIC10F200/202)

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select:
  - Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

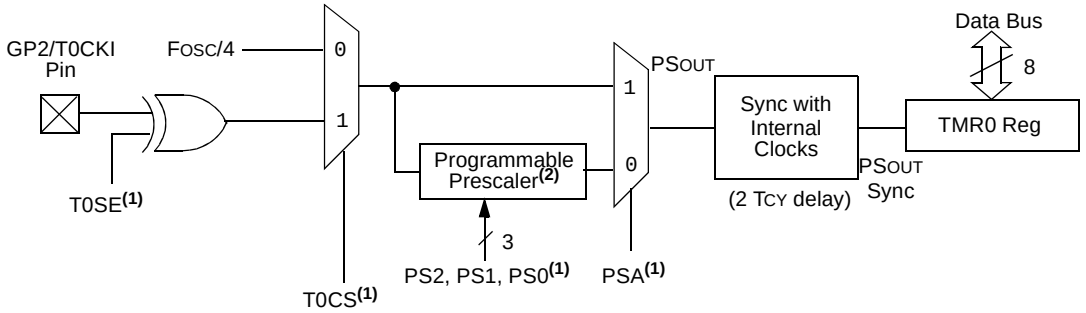
Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in **Section 6.1 "Using Timer0 with an External Clock (PIC10F200/202)"**.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit, PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, 1:256 are selectable. **Section 6.2 "Prescaler"** details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 6-1.

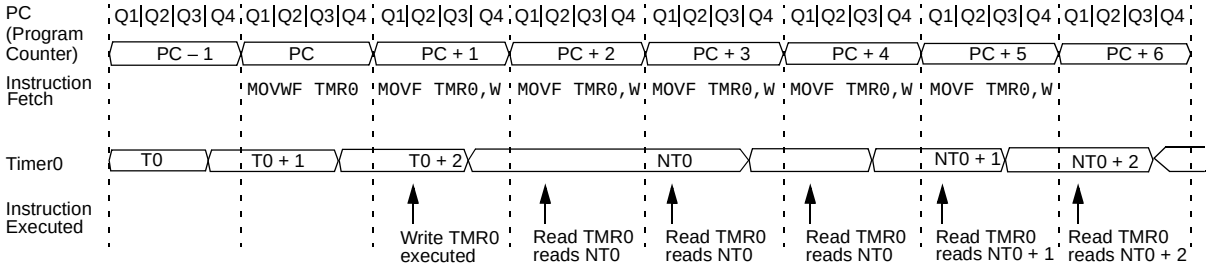
FIGURE 6-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.

2: The prescaler is shared with the Watchdog Timer (Figure 6-5).

FIGURE 6-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE

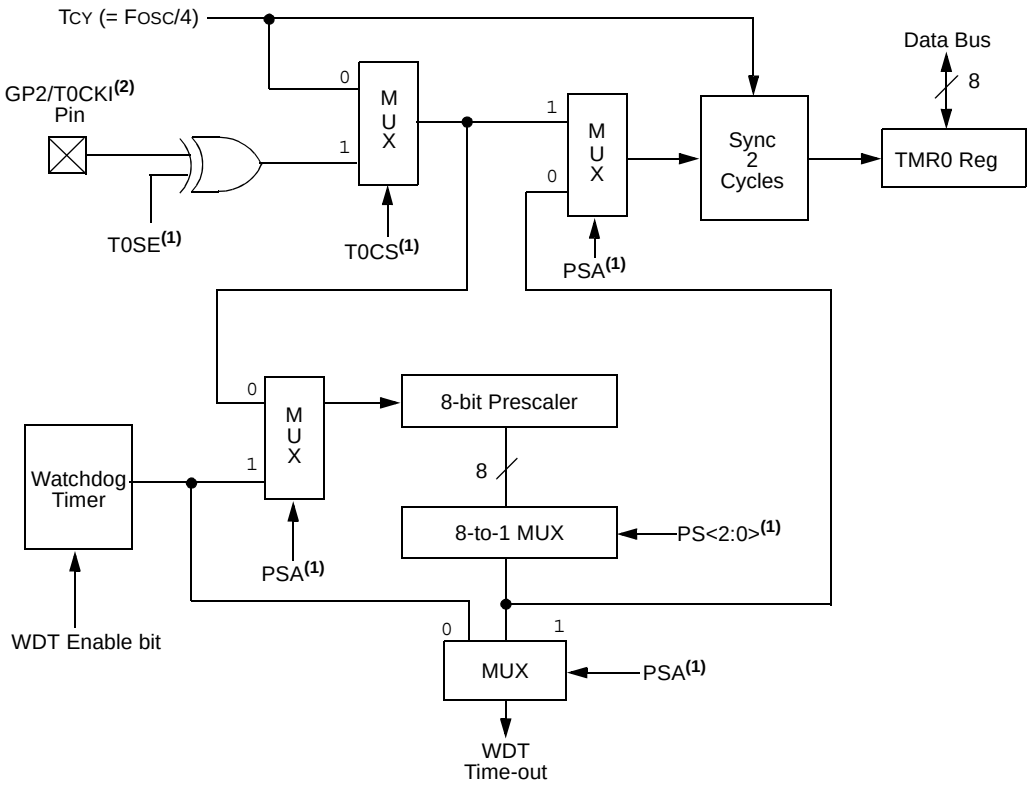


To change the prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A CLRWDT instruction should be executed before switching the prescaler.

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT              ;Clear WDT and
                    ;prescaler
MOVLW  'xxxx0xxx'   ;Select TMR0, new
                    ;prescale value and
                    ;clock source
OPTION
```

FIGURE 6-5: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



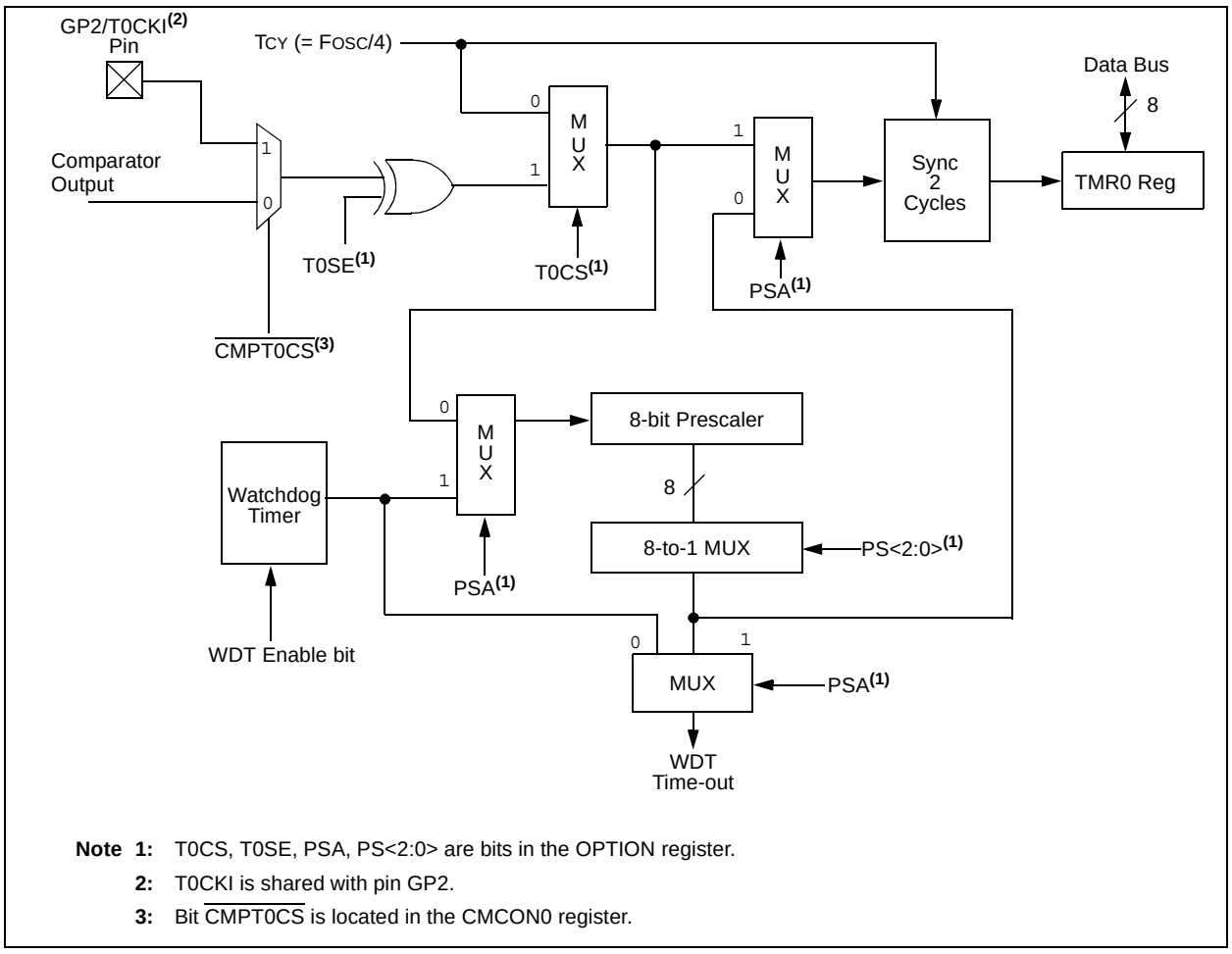
Note 1: T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

2: T0CKI is shared with pin GP2 on the PIC10F200/202/204/206.

EXAMPLE 7-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT              ;Clear WDT and
                    ;prescaler
MOVLW  'xxxx0xxx'   ;Select TMR0, new
                    ;prescale value and
                    ;clock source
OPTION
```

FIGURE 7-5: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note 1: T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

2: T0CKI is shared with pin GP2.

3: Bit $\overline{\text{CMPT0CS}}$ is located in the CMCON0 register.

8.0 COMPARATOR MODULE

The comparator module contains one Analog comparator. The inputs to the comparator are multiplexed with GP0 and GP1 pins. The output of the comparator can be placed on GP2.

The CMCON0 register, shown in Register 8-1, controls the comparator operation. A block diagram of the comparator is shown in Figure 8-1.

REGISTER 8-1: CMCON0 REGISTER

R-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
CMPOUT	$\overline{\text{COUTEN}}$	POL	$\overline{\text{CMPT0CS}}$	CMPON	CNREF	CPREF	$\overline{\text{CWU}}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **CMPOUT:** Comparator Output bit
1 = V_{IN}+ > V_{IN}-
0 = V_{IN}+ < V_{IN}-

bit 6 **$\overline{\text{COUTEN}}$:** Comparator Output Enable bit(1, 2)
1 = Output of comparator is NOT placed on the COUT pin
0 = Output of comparator is placed in the COUT pin

bit 5 **POL:** Comparator Output Polarity bit(2)
1 = Output of comparator not inverted
0 = Output of comparator inverted

bit 4 **$\overline{\text{CMPT0CS}}$:** Comparator TMR0 Clock Source bit(2)
1 = TMR0 clock source selected by T0CS control bit
0 = Comparator output used as TMR0 clock source

bit 3 **CMPON:** Comparator Enable bit
1 = Comparator is on
0 = Comparator is off

bit 2 **CNREF:** Comparator Negative Reference Select bit(2)
1 = CIN- pin(3)
0 = Internal voltage reference

bit 1 **CPREF:** Comparator Positive Reference Select bit(2)
1 = CIN+ pin(3)
0 = CIN- pin(3)

bit 0 **$\overline{\text{CWU}}$:** Comparator Wake-up on Change Enable bit(2)
1 = Wake-up on comparator change is disabled
0 = Wake-up on comparator change is enabled.

Note 1: Overrides T0CS bit for TRIS control of GP2.
2: When the comparator is turned on, these control bits assert themselves. When the comparator is off, these bits have no effect on the device operation and the other control registers have precedence.
3: PIC10F204/206 only.

9.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC10F200/202/204/206 microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving operating modes and offer code protection. These features are:

- Reset:
  - Power-on Reset (POR)
  - Device Reset Timer (DRT)
  - Watchdog Timer (WDT)
  - Wake-up from Sleep on pin change
  - Wake-up from Sleep on comparator change
- Sleep
- Code Protection
- ID Locations
- In-Circuit Serial Programming™
- Clock Out

The PIC10F200/202/204/206 devices have a Watchdog Timer, which can be shut off only through Configuration bit WDTE. It runs off of its own RC oscillator for added reliability. When using INTRC, there is an 18 ms delay only on VDD power-up. With this timer on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-Down mode. The user can wake-up from Sleep through a change on input pins, wake-up from comparator change, or through a Watchdog Timer time-out.

9.1 Configuration Bits

The PIC10F200/202/204/206 Configuration Words consist of 12 bits. Configuration bits can be programmed to select various device configurations. One bit is the Watchdog Timer enable bit, one bit is the $\overline{MCLR}$ enable bit and one bit is for code protection (see Register 9-1).

REGISTER 9-1: CONFIGURATION WORD FOR PIC10F200/202/204/206(1,2)

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	—	—	—	—	—	—	MCLRE	$\overline{CP}$	WDTE	—	—
bit 11											bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 11-5 **Unimplemented:** Read as ‘0’

bit 4 **MCLRE:** GP3/$\overline{MCLR}$ Pin Function Select bit
1 = GP3/$\overline{MCLR}$ pin function is $\overline{MCLR}$
0 = GP3/$\overline{MCLR}$ pin function is digital I/O, $\overline{MCLR}$ internally tied to VDD

bit 3 **$\overline{CP}$:** Code Protection bit
1 = Code protection off
0 = Code protection on

bit 2 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0 **Reserved:** Read as ‘0’

Note 1: Refer to the “*PIC10F200/202/204/206 Memory Programming Specifications*” (DS41228) to determine how to access the Configuration Word. The Configuration Word is not user addressable during device operation.

2: INTRC is the only oscillator mode offered on the PIC10F200/202/204/206.

9.2 Oscillator Configurations

9.2.1 OSCILLATOR TYPES

The PIC10F200/202/204/206 devices are offered with Internal Oscillator mode only.

- INTOSC: Internal 4 MHz Oscillator

9.2.2 INTERNAL 4 MHz OSCILLATOR

The internal oscillator provides a 4 MHz (nominal) system clock (see **Section 12.0 "Electrical Characteristics"** for information on variation over voltage and temperature).

In addition, a calibration instruction is programmed into the last address of memory, which contains the calibration value for the internal oscillator. This location is always uncode protected, regardless of the code-protect settings. This value is programmed as a MOVLW xx instruction where xx is the calibration value and is placed at the Reset vector. This will load the W register with the calibration value upon Reset and the PC will then roll over to the users program at address 0x000. The user then has the option of writing the value to the OSCCAL Register (05h) or ignoring it.

OSCCAL, when written to with the calibration value, will "trim" the internal oscillator to remove process variation from the oscillator frequency.

Note:	Erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be read prior to erasing the part so it can be reprogrammed correctly later.

9.3 Reset

The device differentiates between various kinds of Reset:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ Reset during normal operation
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT time-out Reset during normal operation
- WDT time-out Reset during Sleep
- Wake-up from Sleep on pin change
- Wake-up from Sleep on comparator change

Some registers are not reset in any way, they are unknown on POR and unchanged in any other Reset. Most other registers are reset to "Reset state" on Power-on Reset (POR), $\overline{\text{MCLR}}$, WDT or Wake-up on pin change Reset during normal operation. They are not affected by a WDT Reset during Sleep or $\overline{\text{MCLR}}$ Reset during Sleep, since these Resets are viewed as resumption of normal operation. The exceptions to this are $\overline{\text{TO}}$, $\overline{\text{PD}}$, GPWUF and CWUF bits. They are set or cleared differently in different Reset situations. These bits are used in software to determine the nature of Reset. See Table 9-1 for a full description of Reset states of all registers.

TABLE 9-1: RESET CONDITIONS FOR REGISTERS – PIC10F200/202/204/206

Register	Address	Power-on Reset	$\overline{\text{MCLR}}$ Reset, WDT Time-out, Wake-up On Pin Change, Wake on Comparator Change
W	—	qqqq qqqu(1)	qqqq qqqu(1)
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PCL	02h	1111 1111	1111 1111
STATUS	03h	00-1 1xxx	q00q quuu(2)
STATUS(3)	03h	00-1 1xxx	qq0q quuu(2)
FSR	04h	111x xxxx	111u uuuu
OSCCAL	05h	1111 1110	uuuu uuuu
GPIO	06h	---- xxxx	---- uuuu
CMCON(3)	07h	1111 1111	uuuu uuuu
OPTION	—	1111 1111	1111 1111
TRISGPIO	—	---- 1111	---- 1111

Legend: u = unchanged, x = unknown, – = unimplemented bit, read as '0', q = value depends on condition.
Note 1: Bits <7:2> of W register contain oscillator calibration values due to MOVLW XX instruction at top of memory.
2: See Table 9-2 for Reset value for specific conditions.
3: PIC10F204/206 only.

9.5 Device Reset Timer (DRT)

On the PIC10F200/202/204/206 devices, the DRT runs any time the device is powered-up.

The DRT operates on an internal oscillator. The processor is kept in Reset as long as the DRT is active. The DRT delay allows VDD to rise above VDD min. and for the oscillator to stabilize.

The on-chip DRT keeps the devices in a Reset condition for approximately 18 ms after MCLR has reached a logic high (VIH MCLR) level. Programming GP3/MCLR/VPP as MCLR and using an external RC network connected to the MCLR input is not required in most cases. This allows savings in cost-sensitive and/or space restricted applications, as well as allowing the use of the GP3/MCLR/VPP pin as a general purpose input.

The Device Reset Time delays will vary from chip-to-chip due to VDD, temperature and process variation. See AC parameters for details.

Reset sources are POR, MCLR, WDT time-out and wake-up on pin change. See **Section 9.9.2 "Wake-up from Sleep"**, Notes 1, 2 and 3.

TABLE 9-3: DRT PERIOD

Oscillator	POR Reset	Subsequent Resets
INTOSC	18 ms (typical)	10 µs (typical)

9.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator, which does not require any external components. This RC oscillator is separate from the internal 4 MHz oscillator. This means that the WDT will run even if the main processor clock has been stopped, for example, by execution of a SLEEP instruction. During normal operation or Sleep, a WDT Reset or wake-up Reset, generates a device Reset.

The TO bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset.

The WDT can be permanently disabled by programming the configuration WDTE as a '0' (see **Section 9.1 "Configuration Bits"**). Refer to the PIC10F200/202/204/206 Programming Specifications to determine how to access the Configuration Word.

9.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, a time-out period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

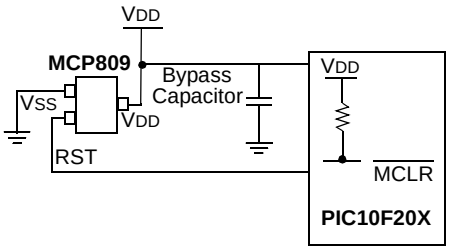
Under worst-case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

9.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device Reset.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum Sleep time before a WDT wake-up Reset.

FIGURE 9-9: BROWN-OUT PROTECTION CIRCUIT 3



Note: This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. There are seven different trip point selections to accommodate 5V to 3V systems.

9.9 Power-down Mode (Sleep)

A device may be powered-down (Sleep) and later powered-up (wake-up from Sleep).

9.9.1 SLEEP

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (STATUS<4>) is set, the $\overline{PD}$ bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low or high-impedance).

Note: A Reset generated by a WDT time-out does not drive the $\overline{MCLR}$ pin low.

For lowest current consumption while powered-down, the T0CKI input should be at VDD or VSS and the GP3/$\overline{MCLR}$/VPP pin must be at a logic high level if $\overline{MCLR}$ is enabled.

9.9.2 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

1. An external Reset input on GP3/$\overline{MCLR}$/VPP pin, when configured as $\overline{MCLR}$.
2. A Watchdog Timer time-out Reset (if WDT was enabled).
3. A change on input pin GP0, GP1 or GP3 when wake-up on change is enabled.
4. A comparator output change has occurred when wake-up on comparator change is enabled.

These events cause a device Reset. The $\overline{TO}$, $\overline{PD}$ GPWUF and CWUF bits can be used to determine the cause of device Reset. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The GPWUF bit indicates a change in state while in Sleep at pins GP0, GP1 or GP3 (since the last file or bit operation on GP port). The CWUF bit indicates a change in the state while in Sleep of the comparator output.

Caution: Right before entering Sleep, read the input pins. When in Sleep, wake-up occurs when the values at the pins change from the state they were in at the last reading. If a wake-up on change occurs and the pins are not read before re-entering Sleep, a wake-up will occur immediately even if no pins change while in Sleep mode.

Note: The WDT is cleared when the device wakes from Sleep, regardless of the wake-up source.

9.10 Program Verification/Code Protection

If the code protection bit has not been programmed, the on-chip program memory can be read out for verification purposes.

The first 64 locations and the last location (Reset vector) can be read, regardless of the code protection bit setting.

9.11 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify.

Use only the lower four bits of the ID locations and always program the upper eight bits as '0's.

9.12 In-Circuit Serial Programming™

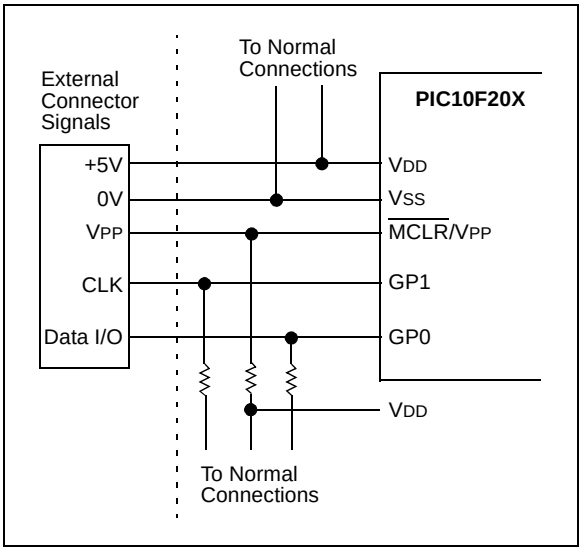
The PIC10F200/202/204/206 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware, to be programmed.

The devices are placed into a Program/Verify mode by holding the GP1 and GP0 pins low while raising the MCLR (V_{PP}) pin from V_{IL} to V_{IHH} (see programming specification). GP1 becomes the programming clock and GP0 becomes the programming data. Both GP1 and GP0 are Schmitt Trigger inputs in this mode.

After Reset, a 6-bit command is then supplied to the device. Depending on the command, 16 bits of program data are then supplied to or from the device, depending if the command was a Load or a Read. For complete details of serial programming, please refer to the PIC10F200/202/204/206 Programming Specifications.

A typical In-Circuit Serial Programming connection is shown in Figure 9-10.

FIGURE 9-10: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING™ CONNECTION



IORWF	Inclusive OR W with f
Syntax:	[*label*] IORWF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(W).OR. (f) → (dest)
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

MOVF	Move f
Syntax:	[*label*] MOVF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(f) → (dest)
Status Affected:	Z
Description:	The contents of register 'f' are moved to destination 'd'. If 'd' is '0', destination is the W register. If 'd' is '1', the destination is file register 'f'. 'd' = 1 is useful as a test of a file register, since status flag Z is affected.

MOVLW	Move literal to W
Syntax:	[*label*] MOVLW k
Operands:	$0 \le k \le 255$
Operation:	k → (W)
Status Affected:	None
Description:	The 8-bit literal 'k' is loaded into the W register. The "don't cares" will assembled as '0's.

MOVWF	Move W to f
Syntax:	[*label*] MOVWF f
Operands:	$0 \le f \le 31$
Operation:	(W) → (f)
Status Affected:	None
Description:	Move data from the W register to register 'f'.

NOP	No Operation
Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.

OPTION	Load OPTION Register
Syntax:	[*label*] OPTION
Operands:	None
Operation:	(W) → Option
Status Affected:	None
Description:	The content of the W register is loaded into the OPTION register.

12.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... 0 to +6.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} ..... 0 to +13.5V
Voltage on all other pins with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Total power dissipation(1) ..... 800 mW
Max. current out of V_{SS} pin ..... 80 mA
Max. current into V_{DD} pin ..... 80 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Max. output current sunk by any I/O pin ..... 25 mA
Max. output current sourced by any I/O pin ..... 25 mA
Max. output current sourced by I/O port ..... 75 mA
Max. output current sunk by I/O port ..... 75 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

†NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 12-1: COMPARATOR SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C								
Param. No.	**Sym.**	**Characteristics**		**Min.**	**Typ.†**	**Max.**	**Units**	**Comments**
D300	VOS	Input Offset Voltage		—	± 5.0	± 10	mV	(VDD - 1.5)/2
D301	VCM	Input Common Mode Voltage		0	—	VDD–1.5*	V	
D302	CMRR	Common Mode Rejection Ratio		55*	—	—	dB	
D303*	TRT	Response Time	Falling	—	150	600	ns	**(Note 1)**
			Rising	—	200	1000	ns	
D304*	TMC2COV	Comparator Mode Change to Output Valid		—	—	10*	µs	
D305	VIVRF	Internal Reference Voltage		0.55	0.6	0.65	V	2.0V ≤ VDD ≤ 5.5V -40°C ≤ TA ≤ ±125°C (extended)

* These parameters are characterized but not tested.

† Data in 'Typ.' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Response time is measured with one comparator input at (VDD - 1.5)/2 - 100 mV to (VDD - 1.5)/2 + 20 mV.

TABLE 12-2: PULL-UP RESISTOR RANGES

VDD (Volts)	**Temperature (°C)**	**Min.**	**Typ.**	**Max.**	**Units**
GP0/GP1					
2.0	-40	73K	105K	186K	Ω
	25	73K	113K	187K	Ω
	85	82K	123K	190K	Ω
	125	86K	132k	190K	Ω
5.5	-40	15K	21K	33K	Ω
	25	15K	22K	34K	Ω
	85	19K	26k	35K	Ω
	125	23K	29K	35K	Ω
GP3					
2.0	-40	63K	81K	96K	Ω
	25	77K	93K	116K	Ω
	85	82K	96k	116K	Ω
	125	86K	100K	119K	Ω
5.5	-40	16K	20k	22K	Ω
	25	16K	21K	23K	Ω
	85	24K	25k	28K	Ω
	125	26K	27K	29K	Ω

TABLE 12-3: CALIBRATED INTERNAL RC FREQUENCIES – PIC10F200/202/204/206

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +85°C (industrial), -40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in **Section 12.1 "DC Characteristics: PIC10F200/202/204/206 (Industrial)"**					
Param. No.	**Sym.**	**Characteristic**	**Freq. Tolerance**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
F10	FOSC	Internal Calibrated INTOSC Frequency(1,2)	± 1%	3.96	4.00	4.04	MHz	VDD=3.5V @ 25°C
			± 2%	3.92	4.00	4.08	MHz	2.5V ≤ VDD ≤ 5.5V 0°C ≤ TA ≤ +85°C (industrial)
			± 5%	3.80	4.00	4.20	MHz	2.0V ≤ VDD ≤ 5.5V -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended)

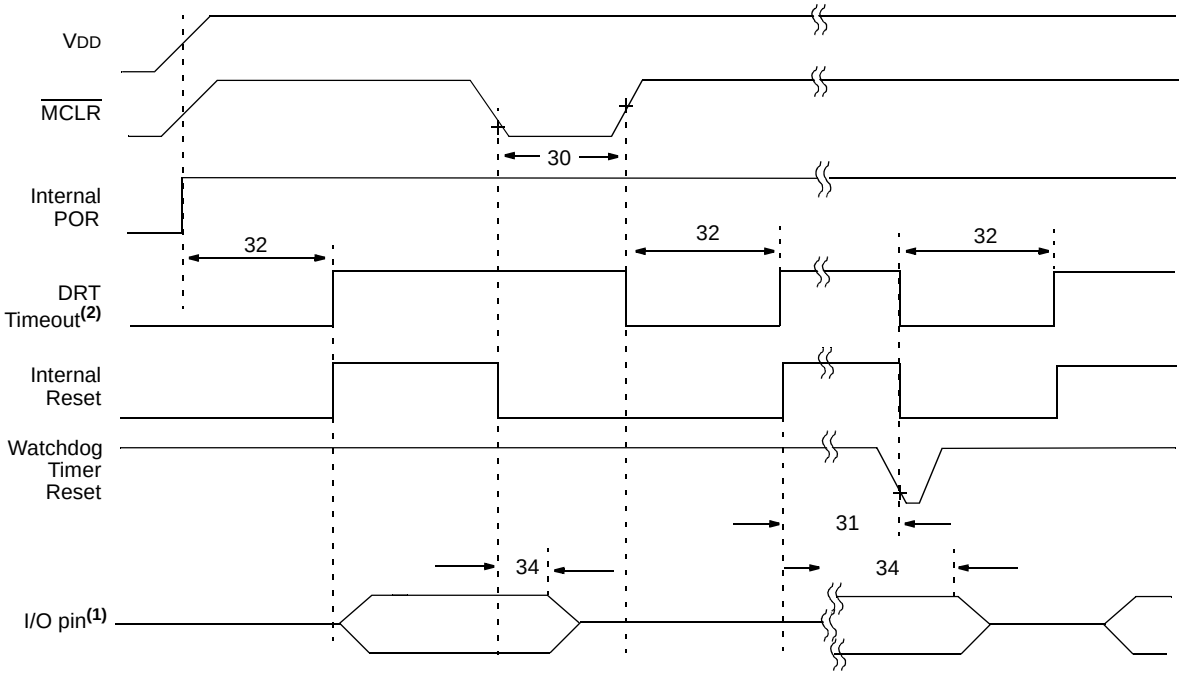
* These parameters are characterized but not tested.

† Data in the Typical ("Typ.") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

2: Under stable VDD conditions.

FIGURE 12-3: RESET, WATCHDOG TIMER AND DEVICE RESET TIMER TIMING – PIC10F200/202/204/206



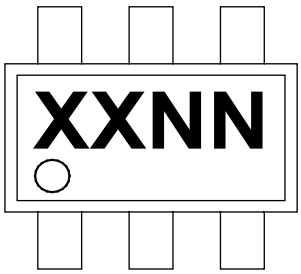
Note 1: I/O pins must be taken out of High-Impedance mode by enabling the output drivers in software.

2: Runs on POR only.

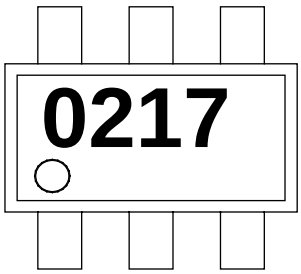
14.0 PACKAGING INFORMATION

14.1 Package Marking Information

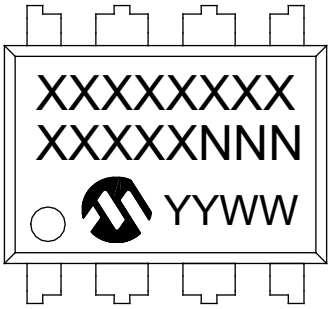
6-Lead SOT-23



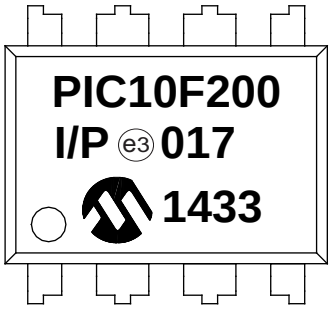
Example



8-Lead PDIP (300 mil)



Example



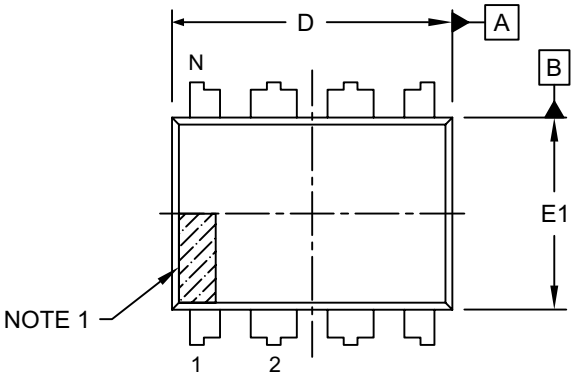
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

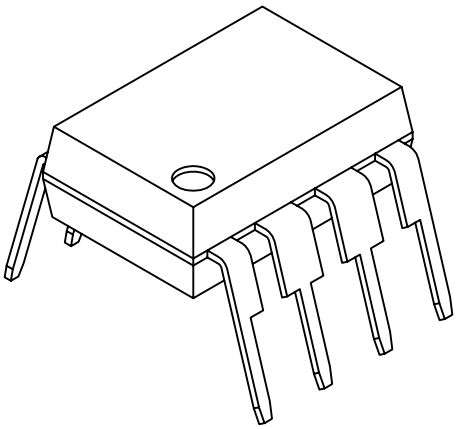
***** Standard PIC® device marking consists of Microchip part number, year code, week code, and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

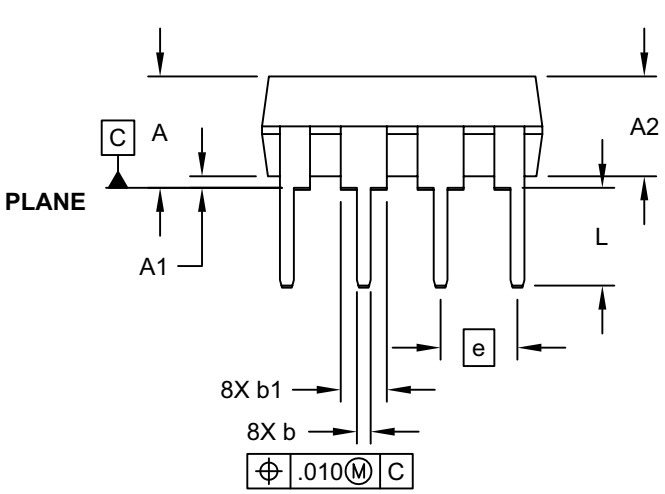
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

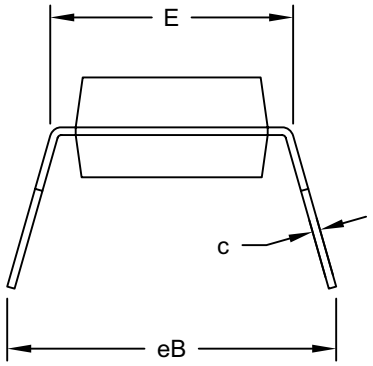


TOP VIEW





SIDE VIEW



END VIEW

Microchip Technology Drawing No. C04-018D Sheet 1 of 2

APPENDIX A: REVISION HISTORY

Revision C (August 2006)

Added 8-Pin DFN Pin Diagram; Revised Table 1-1; Reformatted all Registers; Revised Section 4.8 and added note; Section 5.3 (changed Figure reference to Figure 5-1); Tables 6-1 and 7-1 (removed shading from TRISGPIO (I/O Control Register); Sections 8.1-8.4 (changed Table reference to Table 12-2); Section 14.1 Revised and replaced Package Marking Information and drawings, Added Tables 14-1 & 14-2, Added DFN Package drawing.

Revision D (April 2007)

Revised section 12.1, 12.2, 12.3, Table 1-1, 12-1, 12-3, 12-4. Added Section 13.0. Replaced Package Drawings (Rev. AP); Removed instances of PICmicro® and replaced it with PIC®.

Revision E (October 2013)

Revised Figure 8-1 (deleted OSCCAL); Revised Packaging Legend.

Revision F (September 2014)

Added Table 12-6 (Thermal Considerations); Updated Register 4-1, Register 9-1 and Chapter 14 (Packaging Information); Other minor corrections.