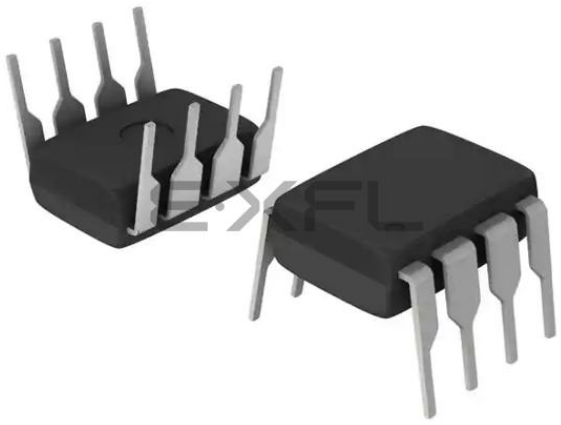

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 3 |
| Program Memory Size | 768B (512 x 12) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 24 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 8-DIP (0.300", 7.62mm) |
| Supplier Device Package | 8-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic10f206-e-p |

## 1.0 GENERAL DESCRIPTION

The PIC10F200/202/204/206 devices from Microchip Technology are low-cost, high-performance, 8-bit, fully-static, Flash-based CMOS microcontrollers. They employ a RISC architecture with only 33 single-word/ single-cycle instructions. All instructions are single cycle (1 μs) except for program branches, which take two cycles. The PIC10F200/202/204/206 devices deliver performance in an order of magnitude higher than their competitors in the same price category. The 12-bit wide instructions are highly symmetrical, resulting in a typical 2:1 code compression over other 8-bit microcontrollers in its class. The easy-to-use and easy to remember instruction set reduces development time significantly.

The PIC10F200/202/204/206 products are equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external Reset circuitry. INTRC Internal Oscillator mode is provided, thereby preserving the limited number of I/O available. Power-Saving Sleep mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The PIC10F200/202/204/206 devices are available in cost-effective Flash, which is suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in Flash programmable microcontrollers, while benefiting from the Flash programmable flexibility.

The PIC10F200/202/204/206 products are supported by a full-featured macro assembler, a software simulator, an in-circuit debugger, a 'C' compiler, a low-cost development programmer and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

### 1.1 Applications

The PIC10F200/202/204/206 devices fit in applications ranging from personal care appliances and security systems to low-power remote transmitters/receivers. The Flash technology makes customizing application programs (transmitter codes, appliance settings, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make these microcontrollers well suited for applications with space limitations. Low cost, low power, high performance, ease-of-use and I/O flexibility make the PIC10F200/202/204/206 devices very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, logic and PLDs in larger systems and coprocessor applications).

**TABLE 1-1: PIC10F200/202/204/206 DEVICES**

| | | PIC10F200 | PIC10F202 | PIC10F204 | PIC10F206 |
|---|---|---|---|---|---|
| Clock | Maximum Frequency of Operation (MHz) | 4 | 4 | 4 | 4 |
| Memory | Flash Program Memory | 256 | 512 | 256 | 512 |
| | Data Memory (bytes) | 16 | 24 | 16 | 24 |
| Peripherals | Timer Module(s) | TMR0 | TMR0 | TMR0 | TMR0 |
| | Wake-up from Sleep on Pin Change | Yes | Yes | Yes | Yes |
| | Comparators | 0 | 0 | 1 | 1 |
| Features | I/O Pins | 3 | 3 | 3 | 3 |
| | Input-Only Pins | 1 | 1 | 1 | 1 |
| | Internal Pull-ups | Yes | Yes | Yes | Yes |
| | In-Circuit Serial Programming™ | Yes | Yes | Yes | Yes |
| | Number of Instructions | 33 | 33 | 33 | 33 |
| | Packages | 6-pin SOT-23<br>8-pin PDIP, DFN | 6-pin SOT-23<br>8-pin PDIP, DFN | 6-pin SOT-23<br>8-pin PDIP, DFN | 6-pin SOT-23<br>8-pin PDIP, DFN |

The PIC10F200/202/204/206 devices have Power-on Reset, selectable Watchdog Timer, selectable code-protect, high I/O current capability and precision internal oscillator.
The PIC10F200/202/204/206 devices use serial programming with data pin GP0 and clock pin GP1.

**TABLE 3-2: PIC10F200/202/204/206 PINOUT DESCRIPTION**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| GP0/ICSPDAT/CIN+ | GP0 | TTL | CMOS | Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change. |
| | ICSPDAT | ST | CMOS | In-Circuit Serial Programming™ data pin. |
| | CIN+ | AN | — | Comparator input (PIC10F204/206 only). |
| GP1/ICSPCLK/CIN- | GP1 | TTL | CMOS | Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change. |
| | ICSPCLK | ST | CMOS | In-Circuit Serial Programming clock pin. |
| | CIN- | AN | — | Comparator input (PIC10F204/206 only). |
| GP2/T0CKI/COUT/ FOSC4 | GP2 | TTL | CMOS | Bidirectional I/O pin. |
| | T0CKI | ST | — | Clock input to TMR0. |
| | COUT | — | CMOS | Comparator output (PIC10F204/206 only). |
| | FOSC4 | — | CMOS | Oscillator/4 output. |
| GP3/$\overline{\text{MCLR}}$/$V_{PP}$ | GP3 | TTL | — | Input pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change. |
| | $\overline{\text{MCLR}}$ | ST | — | Master Clear (Reset). When configured as $\overline{\text{MCLR}}$, this pin is an active-low Reset to the device. Voltage on GP3/$\overline{\text{MCLR}}$/$V_{PP}$ must not exceed $V_{DD}$ during normal device operation or the device will enter Programming mode. Weak pull-up always on if configured as $\overline{\text{MCLR}}$. |
| | $V_{PP}$ | HV | — | Programming voltage input. |
| $V_{DD}$ | $V_{DD}$ | P | — | Positive supply for logic and I/O pins. |
| $V_{SS}$ | $V_{SS}$ | P | — | Ground reference for logic and I/O pins. |

**Legend:** I = Input, O = Output, I/O = Input/Output, P = Power, — = Not used, TTL = TTL input, ST = Schmitt Trigger input, AN = Analog input

## 3.1 Clocking Scheme/Instruction Cycle

The clock is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the PC is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-3 and Example 3-1.

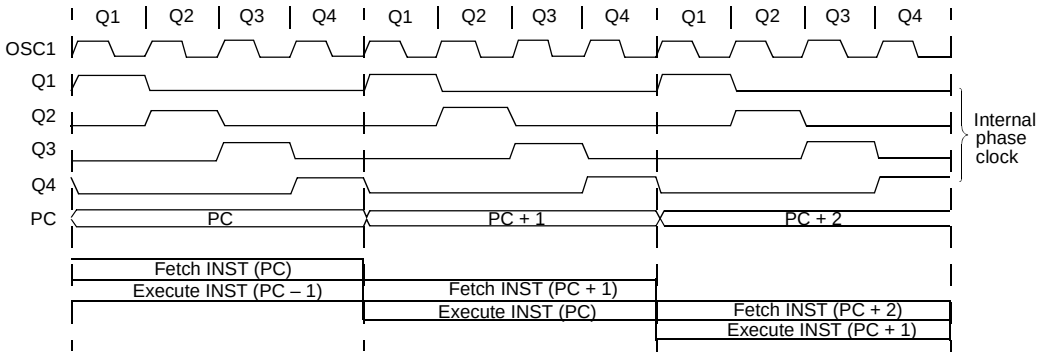
## 3.2 Instruction Flow/Pipelining

An instruction cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute take another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the PC to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the PC incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

**FIGURE 3-3: CLOCK/INSTRUCTION CYCLE**




**EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW**

```
1. MOVLW 03H
2. MOVWF GPIO
3. CALL  SUB_1
4. BSF   GPIO, BIT1
```

| | | | | | |
|---|---|---|---|---|---|
| Fetch 1 | Execute 1 | | | | |
| | Fetch 2 | Execute 2 | | | |
| | | Fetch 3 | Execute 3 | | |
| | | | Fetch 4 | Flush | |
| | | | | Fetch SUB_1 | Execute SUB_1 |

All instructions are single cycle, except for any program branches. These take two cycles, since the fetch instruction is “flushed” from the pipeline, while the new instruction is being fetched and then executed.

## 4.0 MEMORY ORGANIZATION

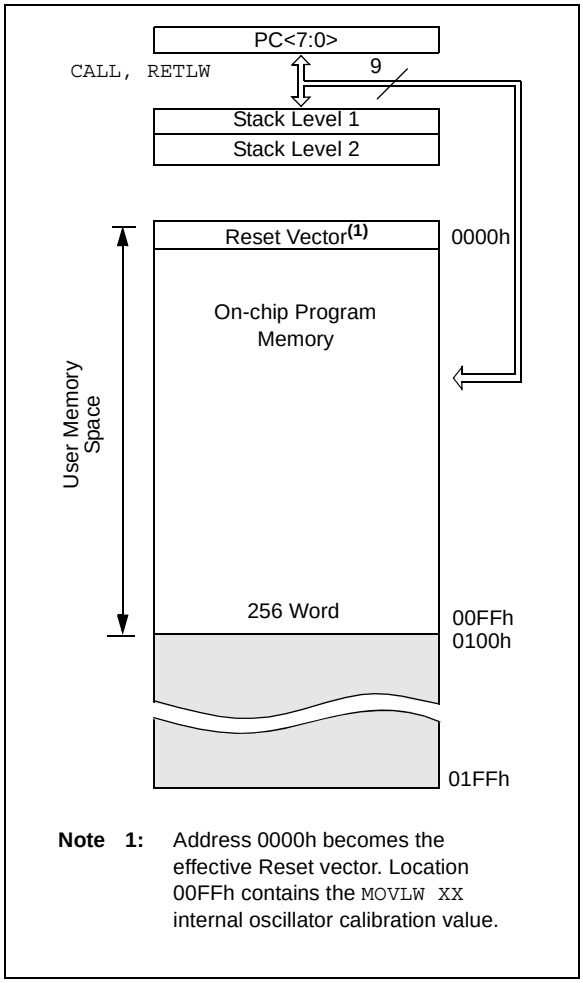
The PIC10F200/202/204/206 memories are organized into program memory and data memory. Data memory banks are accessed using the File Select Register (FSR).

### 4.1 Program Memory Organization for the PIC10F200/204

The PIC10F200/204 devices have a 9-bit Program Counter (PC) capable of addressing a 512 x 12 program memory space.

Only the first 256 x 12 (0000h-00FFh) for the PIC10F200/204 are physically implemented (see Figure 4-1). Accessing a location above these boundaries will cause a wraparound within the first 256 x 12 space (PIC10F200/204). The effective Reset vector is at 0000h (see Figure 4-1). Location 00FFh (PIC10F200/204) contains the internal clock oscillator calibration value. This value should never be overwritten.

**FIGURE 4-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC10F200/204**




**Note 1:** Address 0000h becomes the effective Reset vector. Location 00FFh contains the `MOVLW XX` internal oscillator calibration value.

**TABLE 5-2: SUMMARY OF PORT REGISTERS**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-On Reset | Value on All Other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N/A | TRISGPIO | — | — | — | — | I/O Control Register | | | | ---- 1111 | ---- 1111 |
| N/A | OPTION | $\overline{\text{GPWU}}$ | $\overline{\text{GPPU}}$ | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| 03h | STATUS | GPWUF | CWUF | — | $\overline{\text{TO}}$ | $\overline{\text{PD}}$ | Z | DC | C | 00-1 1xxx | qq-q quuu(1), (2) |
| 06h | GPIO | — | — | — | — | GP3 | GP2 | GP1 | GP0 | ---- xxxx | ---- uuuu |

**Legend:** Shaded cells are not used by PORT registers, read as '0', – = unimplemented, read as '0', x = unknown, u = unchanged, q = depends on condition.

**Note 1:** If Reset was due to wake-up on pin change, then bit 7 = 1. All other Resets will cause bit 7 = 0.

**2:** If Reset was due to wake-up on comparator change, then bit 6 = 1. All other Resets will cause bit 6 = 0.

## 5.4 I/O Programming Considerations

### 5.4.1 BIDIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and rewrite the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit 2 of GPIO will cause all eight bits of GPIO to be read into the CPU, bit 2 to be set and the GPIO value to be written to the output latches. If another bit of GPIO is used as a bidirectional I/O pin (say bit 0), and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit 0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential Read-Modify-Write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired OR", "wired AND"). The resulting high output currents may damage the chip.

**EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT**

```
;Initial GPIO Settings
;GPIO<3:2> Inputs
;GPIO<1:0> Outputs
;
;                 GPIO latch   GPIO pins
;                 ----------   ----------
 BCF    GPIO,  1 ;---- pp01    ---- pp11
 BCF    GPIO,  0 ;---- pp10    ---- pp11
 MOVLW  007h;
 TRIS   GPIO     ;---- pp10    ---- pp11
;
```

**Note 1:** The user may have expected the pin values to be ---- pp00. The 2nd BCF caused GP1 to be latched as the pin value (High).

### 5.4.2 SUCCESSIVE OPERATIONS ON I/O PORTS

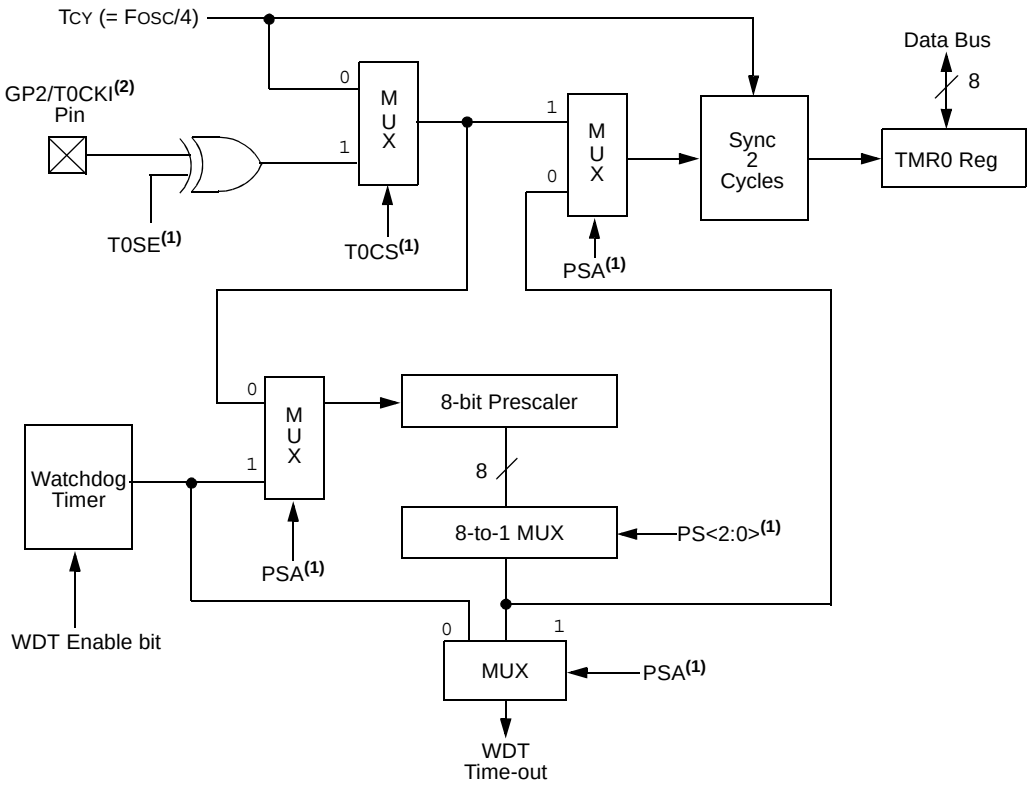
The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction causes that file to be read into the CPU. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

To change the prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A CLRWDT instruction should be executed before switching the prescaler.

**EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)**

```
CLRWDT              ;Clear WDT and
                    ;prescaler
MOVLW  'xxxx0xxx'   ;Select TMR0, new
                    ;prescale value and
                    ;clock source
OPTION
```

**FIGURE 6-5: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER**




**Note 1:** T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

**2:** T0CKI is shared with pin GP2 on the PIC10F200/202/204/206.

## 8.0 COMPARATOR MODULE

The comparator module contains one Analog comparator. The inputs to the comparator are multiplexed with GP0 and GP1 pins. The output of the comparator can be placed on GP2.

The CMCON0 register, shown in Register 8-1, controls the comparator operation. A block diagram of the comparator is shown in Figure 8-1.

**REGISTER 8-1: CMCON0 REGISTER**

| R-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| CMPOUT | $\overline{\text{COUTEN}}$ | POL | $\overline{\text{CMPT0CS}}$ | CMPON | CNREF | CPREF | $\overline{\text{CWU}}$ |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **CMPOUT:** Comparator Output bit
1 = $V_{IN}$+ > $V_{IN}$-
0 = $V_{IN}$+ < $V_{IN}$-

bit 6 **$\overline{\text{COUTEN}}$:** Comparator Output Enable bit(1, 2)
1 = Output of comparator is NOT placed on the COUT pin
0 = Output of comparator is placed in the COUT pin

bit 5 **POL:** Comparator Output Polarity bit(2)
1 = Output of comparator not inverted
0 = Output of comparator inverted

bit 4 **$\overline{\text{CMPT0CS}}$:** Comparator TMR0 Clock Source bit(2)
1 = TMR0 clock source selected by T0CS control bit
0 = Comparator output used as TMR0 clock source

bit 3 **CMPON:** Comparator Enable bit
1 = Comparator is on
0 = Comparator is off

bit 2 **CNREF:** Comparator Negative Reference Select bit(2)
1 = CIN- pin(3)
0 = Internal voltage reference

bit 1 **CPREF:** Comparator Positive Reference Select bit(2)
1 = CIN+ pin(3)
0 = CIN- pin(3)

bit 0 **$\overline{\text{CWU}}$:** Comparator Wake-up on Change Enable bit(2)
1 = Wake-up on comparator change is disabled
0 = Wake-up on comparator change is enabled.

**Note 1:** Overrides T0CS bit for TRIS control of GP2.
**2:** When the comparator is turned on, these control bits assert themselves. When the comparator is off, these bits have no effect on the device operation and the other control registers have precedence.
**3:** PIC10F204/206 only.

**FIGURE 8-3: ANALOG INPUT MODE**

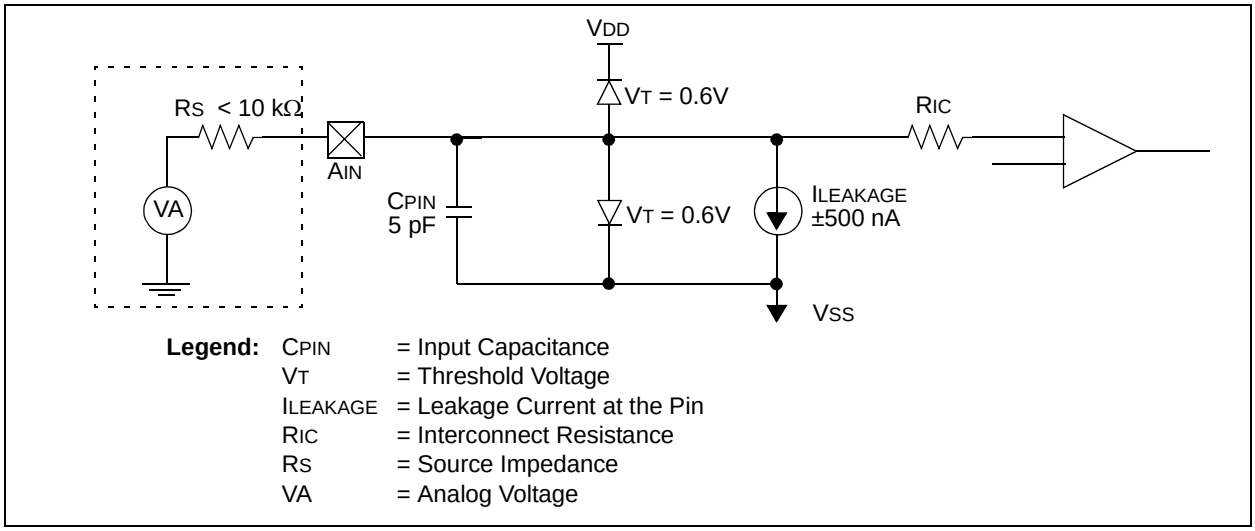



**TABLE 8-2: REGISTERS ASSOCIATED WITH COMPARATOR MODULE**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR | Value on All Other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 03h | STATUS | GPWUF | CWUF | — | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | 00-1 1xxx | qq0q quuu |
| 07h | CMCON0 | CMPOUT | $\overline{COUTEN}$ | POL | $\overline{CMPT0CS}$ | CMPON | CNREF | CPREF | $\overline{CWU}$ | 1111 1111 | uuuu uuuu |
| N/A | TRISGPIO | — | — | — | — | I/O Control Register | | | | ---- 1111 | ---- 1111 |

**Legend:** x = Unknown, u = Unchanged, – = Unimplemented, read as '0', q = Depends on condition.

**TABLE 9-2: RESET CONDITION FOR SPECIAL REGISTERS**

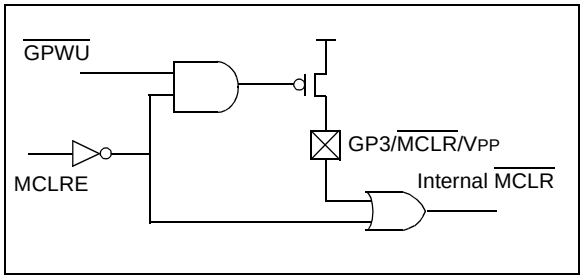
| — | STATUS Address: 03h | PCL Address: 02h |
|---|---|---|
| Power-on Reset | 00-1 1xxx | 1111 1111 |
| $\overline{MCLR}$ Reset during normal operation | 000u uuuu | 1111 1111 |
| $\overline{MCLR}$ Reset during Sleep | 0001 0uuu | 1111 1111 |
| WDT Reset during Sleep | 0000 0uuu | 1111 1111 |
| WDT Reset normal operation | 0000 uuuu | 1111 1111 |
| Wake-up from Sleep on pin change | 1001 0uuu | 1111 1111 |
| Wake-up from Sleep on comparator change | 0101 0uuu | 1111 1111 |

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, read as '0'.

### 9.3.1 $\overline{MCLR}$ ENABLE

This Configuration bit, when unprogrammed (left in the '1' state), enables the external $\overline{MCLR}$ function. When programmed, the $\overline{MCLR}$ function is tied to the internal $V_{DD}$ and the pin is assigned to be a I/O. See Figure 9-1.

**FIGURE 9-1: $\overline{MCLR}$ SELECT**




## 9.4 Power-on Reset (POR)

The PIC10F200/202/204/206 devices incorporate an on-chip Power-on Reset (POR) circuitry, which provides an internal chip Reset for most power-up situations.

The on-chip POR circuit holds the chip in Reset until $V_{DD}$ has reached a high enough level for proper operation. To take advantage of the internal POR, program the GP3/$\overline{MCLR}$/$V_{PP}$ pin as $\overline{MCLR}$ and tie through a resistor to $V_{DD}$, or program the pin as GP3. An internal weak pull-up resistor is implemented using a transistor (refer to Table 12-2 for the pull-up resistor ranges). This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for $V_{DD}$ is specified. See **Section 12.0 "Electrical Characteristics"** for details.

When the devices start normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the devices must be held in Reset until the operating parameters are met.

A simplified block diagram of the on-chip Power-on Reset circuit is shown in Figure 9-2.

The Power-on Reset circuit and the Device Reset Timer (see **Section 9.5 "Device Reset Timer (DRT)"**) circuit are closely related. On power-up, the Reset latch is set and the DRT is reset. The DRT timer begins counting once it detects $\overline{MCLR}$ to be high. After the time-out period, which is typically 18 ms, it will reset the Reset latch and thus end the on-chip Reset signal.

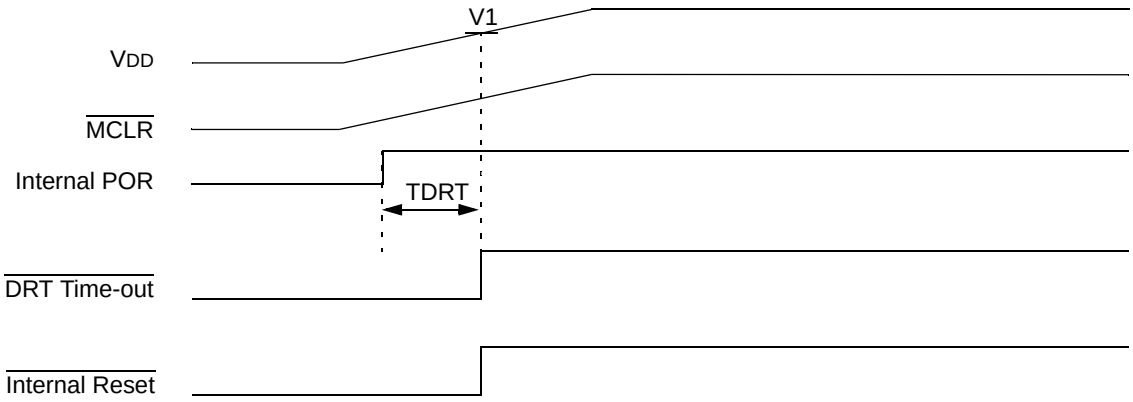
A power-up example where $\overline{MCLR}$ is held low is shown in Figure 9-3. $V_{DD}$ is allowed to rise and stabilize before bringing $\overline{MCLR}$ high. The chip will actually come out of Reset $T_{DRT}$ msec after $\overline{MCLR}$ goes high.

In Figure 9-4, the on-chip Power-on Reset feature is being used ($\overline{MCLR}$ and $V_{DD}$ are tied together or the pin is programmed to be GP3). The $V_{DD}$ is stable before the Start-up Timer times out and there is no problem in getting a proper Reset. However, Figure 9-5 depicts a problem situation where $V_{DD}$ rises too slowly. The time between when the DRT senses that $\overline{MCLR}$ is high and when $\overline{MCLR}$ and $V_{DD}$ actually reach their full value, is too long. In this situation, when the Start-up Timer times out, $V_{DD}$ has not reached the $V_{DD}$ (min) value and the chip may not function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 9-4).

| **Note:** | When the devices start normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met. |
|---|---|

For additional information, refer to Application Notes AN522 *"Power-up Considerations"*, (DS00522) and AN607 *"Power-up Trouble Shooting"*, (DS00000607).

**FIGURE 9-5: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO $V_{DD}$): SLOW $V_{DD}$ RISE TIME**




**Note:** When $V_{DD}$ rises slowly, the $T_{DRT}$ time-out expires long before $V_{DD}$ has reached its final value. In this example, the chip will reset properly if, and only if, V1 ≥ $V_{DD}$ min.

## 9.10 Program Verification/Code Protection

If the code protection bit has not been programmed, the on-chip program memory can be read out for verification purposes.

The first 64 locations and the last location (Reset vector) can be read, regardless of the code protection bit setting.

## 9.11 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify.

Use only the lower four bits of the ID locations and always program the upper eight bits as '0's.

## 9.12 In-Circuit Serial Programming™

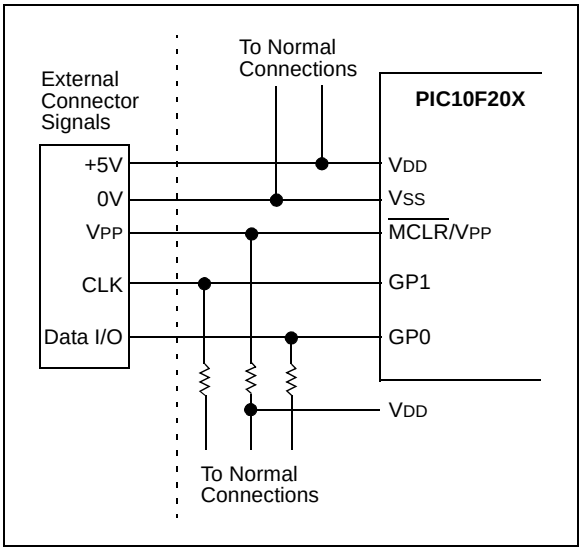
The PIC10F200/202/204/206 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware, to be programmed.

The devices are placed into a Program/Verify mode by holding the GP1 and GP0 pins low while raising the MCLR ($V_{PP}$) pin from $V_{IL}$ to $V_{IHH}$ (see programming specification). GP1 becomes the programming clock and GP0 becomes the programming data. Both GP1 and GP0 are Schmitt Trigger inputs in this mode.

After Reset, a 6-bit command is then supplied to the device. Depending on the command, 16 bits of program data are then supplied to or from the device, depending if the command was a Load or a Read. For complete details of serial programming, please refer to the PIC10F200/202/204/206 Programming Specifications.

A typical In-Circuit Serial Programming connection is shown in Figure 9-10.

**FIGURE 9-10: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING™ CONNECTION**



**RETLW** **Return with literal in W**

Syntax: [ *label* ] RETLW k

Operands: $0 \le k \le 255$

Operation: $k \rightarrow (W)$;
$TOS \rightarrow PC$

Status Affected: None

Description: The W register is loaded with the 8-bit literal ‘k’. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.

**RLF** **Rotate Left f through Carry**

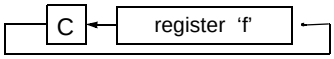
Syntax: [ *label* ] RLF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register ‘f’ are rotated one bit to the left through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.




**RRF** **Rotate Right f through Carry**

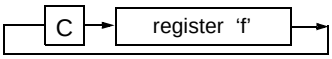
Syntax: [ *label* ] RRF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register ‘f’ are rotated one bit to the right through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.




**SLEEP** **Enter SLEEP Mode**

Syntax: [ *label* ] SLEEP

Operands: None

Operation: $00h \rightarrow WDT$;
$0 \rightarrow$ WDT prescaler;
$1 \rightarrow \overline{TO}$;
$0 \rightarrow \overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$, RBWUF

Description: Time-out Status bit ($\overline{TO}$) is set. The Power-down Status bit ($\overline{PD}$) is cleared.

RBWUF is unaffected.

The WDT and its prescaler are cleared.

The processor is put into Sleep mode with the oscillator stopped. See **Section 9.9 “Power-down Mode (Sleep)”** for more details.

**SUBWF** **Subtract W from f**

Syntax: [ *label* ] SUBWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(f) - (W) \rightarrow (dest)$

Status Affected: C, DC, Z

Description: Subtract (2’s complement method) the W register from register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.

**SWAPF** **Swap Nibbles in f**

Syntax: [ *label* ] SWAPF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(f<3:0>) \rightarrow (dest<7:4>)$;
$(f<7:4>) \rightarrow (dest<3:0>)$

Status Affected: None

Description: The upper and lower nibbles of register ‘f’ are exchanged. If ‘d’ is ‘0’, the result is placed in W register. If ‘d’ is ‘1’, the result is placed in register ‘f’.

## 11.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

## 11.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

## 11.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

## 11.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

## 12.1 DC Characteristics: PIC10F200/202/204/206 (Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +85°C (industrial) | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage** | 2.0 | | 5.5 | V | See Figure 12-1 |
| D002 | VDR | **RAM Data Retention Voltage(2)** | 1.5* | — | — | V | Device in Sleep mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | Vss | — | V | |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | |
| D010 | IDD | **Supply Current(3)** | | | | | |
| | | | —<br>— | 175<br>0.63 | 275<br>1.1 | µA<br>mA | VDD = 2.0V<br>VDD = 5.0V |
| D020 | IPD | **Power-down Current(4)** | | | | | |
| | | | —<br>— | 0.1<br>0.35 | 1.2<br>2.4 | µA<br>µA | VDD = 2.0V<br>VDD = 5.0V |
| D022 | IWDT | **WDT Current(5)** | | | | | |
| | | | —<br>— | 1.0<br>7 | 3<br>16 | µA<br>µA | VDD = 2.0V<br>VDD = 5.0V |
| D023 | ICMP | **Comparator Current(5)** | | | | | |
| | | | —<br>— | 12<br>44 | 23<br>80 | µA<br>µA | VDD = 2.0V<br>VDD = 5.0V |
| D024 | IVREF | **Internal Reference Current(5,6)** | | | | | |
| | | | — | 85<br>175 | 115<br>195 | µA<br>µA | VDD = 2.0V<br>VDD = 5.0V |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ.") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**2:** This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

**3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:
All I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in Sleep mode.

**4:** Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS.

**5:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled.

**6:** Measured with the comparator enabled.

## 12.2 DC Characteristics: PIC10F200/202/204/206 (Extended)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +125°C (extended) | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage** | 2.0 | | 5.5 | V | See Figure 12-1 |
| D002 | VDR | **RAM Data Retention Voltage(2)** | 1.5* | | — | V | Device in Sleep mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | Vss | — | V | |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | |
| D010 | IDD | **Supply Current(3)** | | | | | |
| | | | —<br>— | 175<br>0.63 | 275<br>1.1 | µA<br>mA | VDD = 2.0V<br>VDD = 5.0V |
| D020 | IPD | **Power-down Current(4)** | | | | | |
| | | | —<br>— | 0.1<br>0.35 | 9<br>15 | µA<br>µA | VDD = 2.0V<br>VDD = 5.0V |
| D022 | IWDT | **WDT Current(5)** | | | | | |
| | | | —<br>— | 1.0<br>7 | 18<br>22 | µA<br>µA | VDD = 2.0V<br>VDD = 5.0V |
| D023 | ICMP | **Comparator Current(5)** | | | | | |
| | | | —<br>— | 12<br>42 | 27<br>85 | µA<br>µA | VDD = 2.0V<br>VDD = 5.0V |
| D024 | VREF | **Internal Reference Current(5,6)** | | | | | |
| | | | — | 85<br>175 | 120<br>200 | µA<br>µA | VDD = 2.0V<br>VDD = 5.0V |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ.") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**2:** This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

**3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:
All I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in Sleep mode.

**4:** Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS.

**5:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled.

**6:** Measured with the Comparator enabled.

**TABLE 12-4: RESET, WATCHDOG TIMER AND DEVICE RESET TIMER – PIC10F200/202/204/206**

| AC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +85°C (industrial)<br>-40°C ≤ TA ≤ +125°C (extended)<br>Operating Voltage VDD range is described in Section 12.1 "DC Characteristics: PIC10F200/202/204/206 (Industrial)" | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| 30 | TMCL | $\overline{\text{MCLR}}$ Pulse Width (low) | 2*<br>5* | —<br>— | —<br>— | µs<br>µs | VDD = 5V, -40°C to +85°C<br>VDD = 5.0V |
| 31 | TWDT | Watchdog Timer Time-out Period (no prescaler) | 10<br>10 | 16<br>16 | 29<br>31 | ms<br>ms | VDD = 5.0V (industrial)<br>VDD = 5.0V (extended) |
| 32 | TDRT | Device Reset Timer Period (standard) | 10<br>10 | 16<br>16 | 29<br>31 | ms<br>ms | VDD = 5.0V (industrial)<br>VDD = 5.0V (extended) |
| 34 | TIOZ | I/O High-impedance from $\overline{\text{MCLR}}$ low | — | — | 2* | µs | |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ.") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 12-4: TIMER0 CLOCK TIMINGS – PIC10F200/202/204/206**

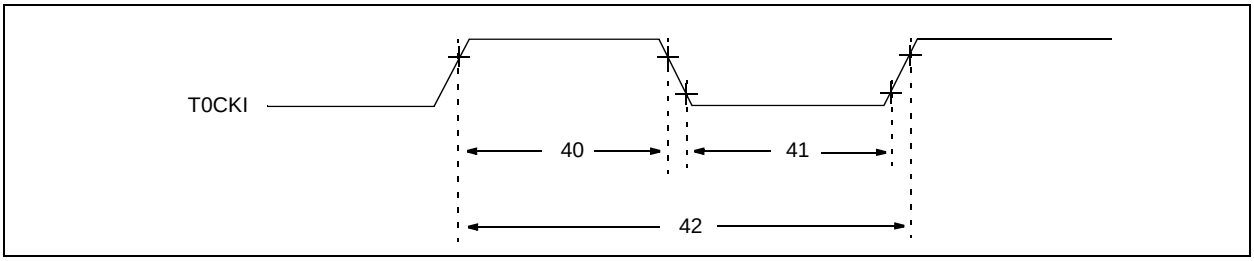



**TABLE 12-5: TIMER0 CLOCK REQUIREMENTS – PIC10F200/202/204/206**

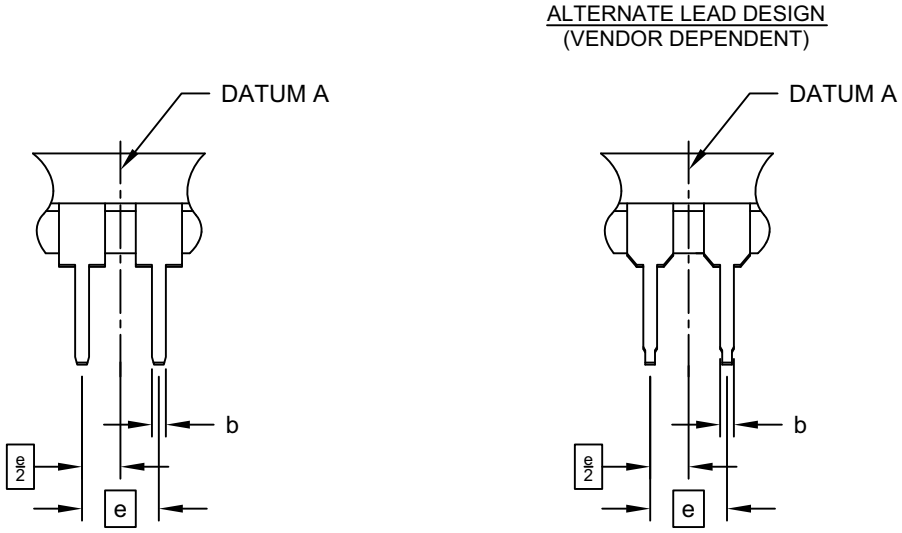
| AC CHARACTERISTICS | | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +85°C (industrial)<br>-40°C ≤ TA ≤ +125°C (extended)<br>Operating Voltage VDD range is described in<br>Section 12.1 "DC Characteristics: PIC10F200/202/204/206 (Industrial)". | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| 40 | Tt0H | T0CKI High Pulse Width | No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | | With Prescaler | 10* | — | — | ns | |
| 41 | Tt0L | T0CKI Low Pulse Width | No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | | With Prescaler | 10* | — | — | ns | |
| 42 | Tt0P | T0CKI Period | | 20 or $\frac{T_{CY} + 40^*}{N}$ | — | — | ns | Whichever is greater.<br>N = Prescale Value<br>(1, 2, 4,..., 256) |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ.") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

## 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | - | - | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | - | - |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | - | - | .430 |

Notes:

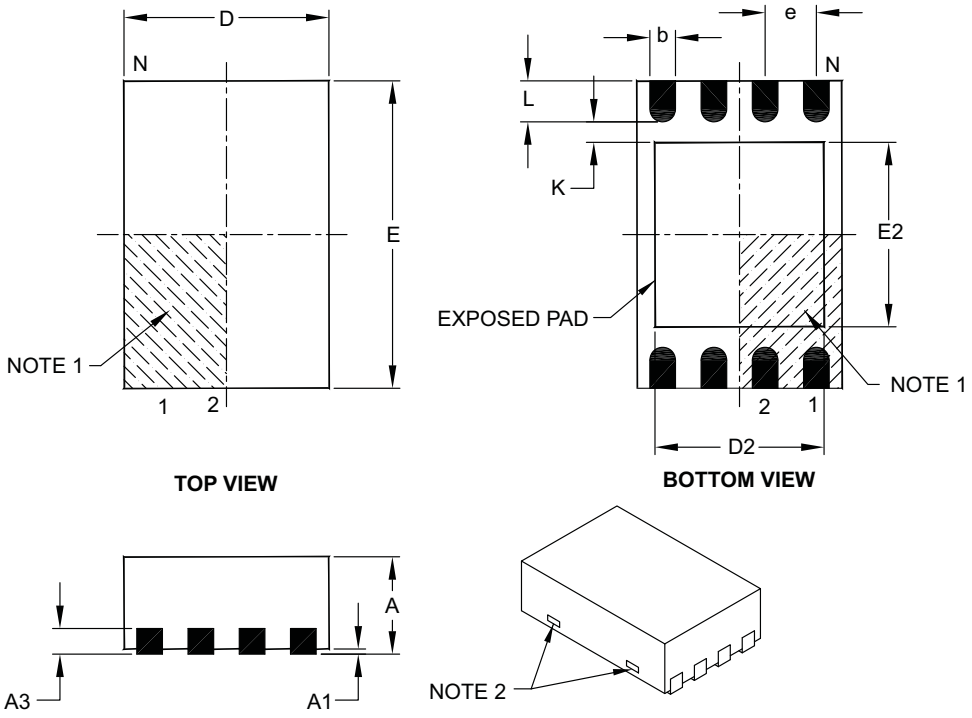
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-018D Sheet 2 of 2

### 8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 2.00 BSC | |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Length | D2 | 1.30 | – | 1.55 |
| Exposed Pad Width | E2 | 1.50 | – | 1.75 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C

## APPENDIX A: REVISION HISTORY

### Revision C (August 2006)

Added 8-Pin DFN Pin Diagram; Revised Table 1-1; Reformatted all Registers; Revised Section 4.8 and added note; Section 5.3 (changed Figure reference to Figure 5-1); Tables 6-1 and 7-1 (removed shading from TRISGPIO (I/O Control Register); Sections 8.1-8.4 (changed Table reference to Table 12-2); Section 14.1 Revised and replaced Package Marking Information and drawings, Added Tables 14-1 & 14-2, Added DFN Package drawing.

### Revision D (April 2007)

Revised section 12.1, 12.2, 12.3, Table 1-1, 12-1, 12-3, 12-4. Added Section 13.0. Replaced Package Drawings (Rev. AP); Removed instances of PICmicro® and replaced it with PIC®.

### Revision E (October 2013)

Revised Figure 8-1 (deleted OSCCAL); Revised Packaging Legend.

### Revision F (September 2014)

Added Table 12-6 (Thermal Considerations); Updated Register 4-1, Register 9-1 and Chapter 14 (Packaging Information); Other minor corrections.

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | [X](1) | - | X | /XX | XXX |
|---|---|---|---|---|---|
| Device | Tape and Reel Option | | Temperature Range | Package | Pattern |

| | |
|---|---|
| **Device:** | PIC10F200<br>PIC10F202<br>PIC10F204<br>PIC10F206<br>PIC10F200T (Tape & Reel)<br>PIC10F202T (Tape & Reel)<br>PIC10F204T (Tape & Reel)<br>PIC10F206T (Tape & Reel) |
| **Tape and Reel Option:** | Blank = Standard packaging (tube or tray)<br>T = Tape and Reel(1) |
| **Temperature Range:** | I = -40°C to +85°C (Industrial)<br>E = -40°C to +125°C (Extended) |
| **Package:** | P = 300 mil PDIP (Pb-free)<br>OT = SOT-23, 6-LD (Pb-free)<br>MC = DFN, 8-LD 2x3 (Pb-free) |
| **Pattern:** | QTP, SQTP, Code or Special Requirements (blank otherwise) |

**Examples:**

a) PIC10F202T - E/OT
Tape and Reel
Extended temperature
SOT-23 package (Pb-free)

b) PIC10F200 - I/P
Industrial temperature,
PDIP package (Pb-free)

c) PIC10F204 - I/MC
Industrial temperature
DFN package (Pb-free)

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.