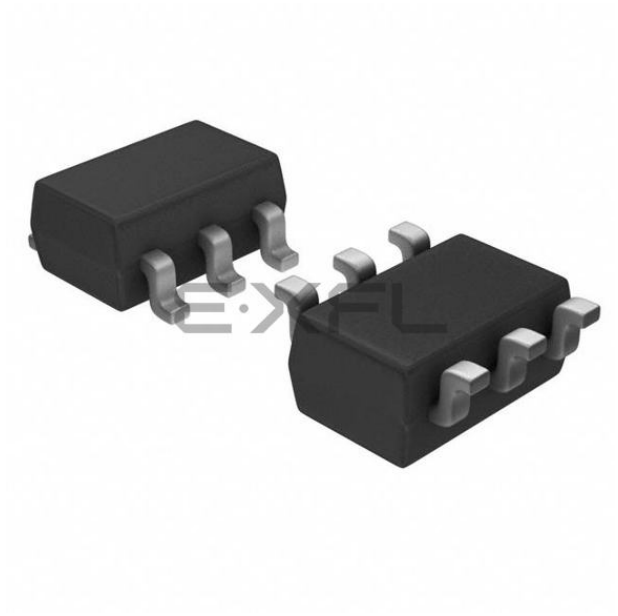

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	3
Program Memory Size	768B (512 x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	SOT-23-6
Supplier Device Package	SOT-23-6
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic10f206t-e-ot

4.5 OPTION Register

The OPTION register is a 8-bit wide, write-only register, which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the OPTION instruction, the contents of the W register will be transferred to the OPTION register. A Reset sets the OPTION<7:0> bits.

Note: If TRIS bit is set to '0', the wake-up on change and pull-up functions are disabled for that pin (i.e., note that TRIS overrides Option control of $\overline{GPPU}$ and $\overline{GPWU}$).

Note: If the T0CS bit is set to '1', it will override the TRIS function on the T0CKI pin.

REGISTER 4-2: OPTION REGISTER

W-1	W-1	W-1	W-1	W-1	W-1	W-1	W-1
$\overline{GPWU}$	$\overline{GPPU}$	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{GPWU}$:** Enable Wake-up on Pin Change bit (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 6 **$\overline{GPPU}$:** Enable Weak Pull-ups bit (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 5 **T0CS:** Timer0 Clock Source Select bit
1 = Transition on T0CKI pin (overrides TRIS on the T0CKI pin)
0 = Transition on internal instruction cycle clock, FOSC/4

bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on the T0CKI pin
0 = Increment on low-to-high transition on the T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

.

6.0 TIMER0 MODULE AND TMR0 REGISTER (PIC10F200/202)

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select:
  - Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

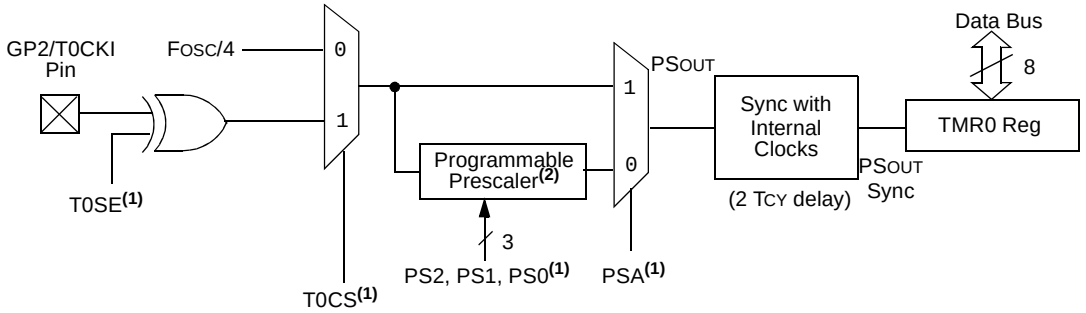
Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in **Section 6.1 "Using Timer0 with an External Clock (PIC10F200/202)"**.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit, PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, 1:256 are selectable. **Section 6.2 "Prescaler"** details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 6-1.

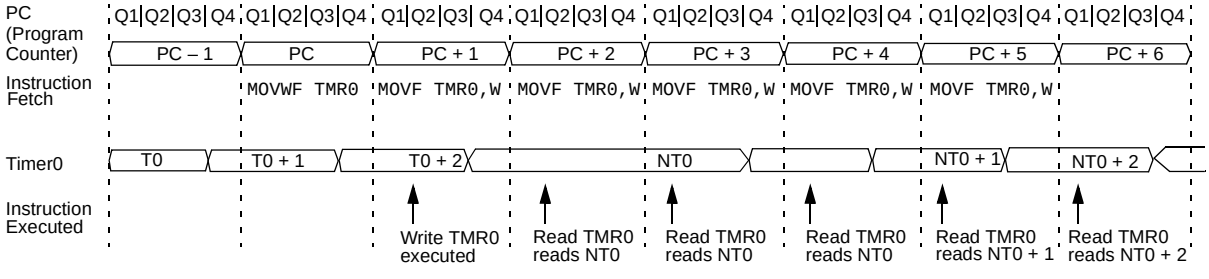
FIGURE 6-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.

2: The prescaler is shared with the Watchdog Timer (Figure 6-5).

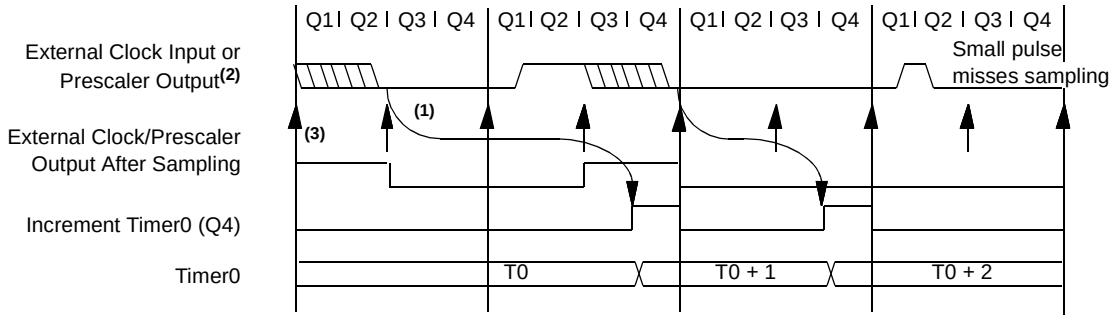
FIGURE 6-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE



7.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 7-4 shows the delay from the external clock edge to the timer incrementing.

FIGURE 7-4: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to Timer0 increment is 3 TOSC to 7 TOSC (Duration of Q = TOSC). Therefore, the error in measuring the interval between two edges on Timer0 input = ±4 TOSC max.

2: External clock if no prescaler selected; prescaler output otherwise.

3: The arrows indicate the points in time where sampling occurs.

7.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module or as a postscaler for the Watchdog Timer (WDT), respectively (see Figure 9-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet.

Note:	The prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT and vice versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x`, etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a Reset, the prescaler contains all '0's.

7.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on-the-fly" during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 7-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 7-1: CHANGING PRESCALER (TIMER0 → WDT)

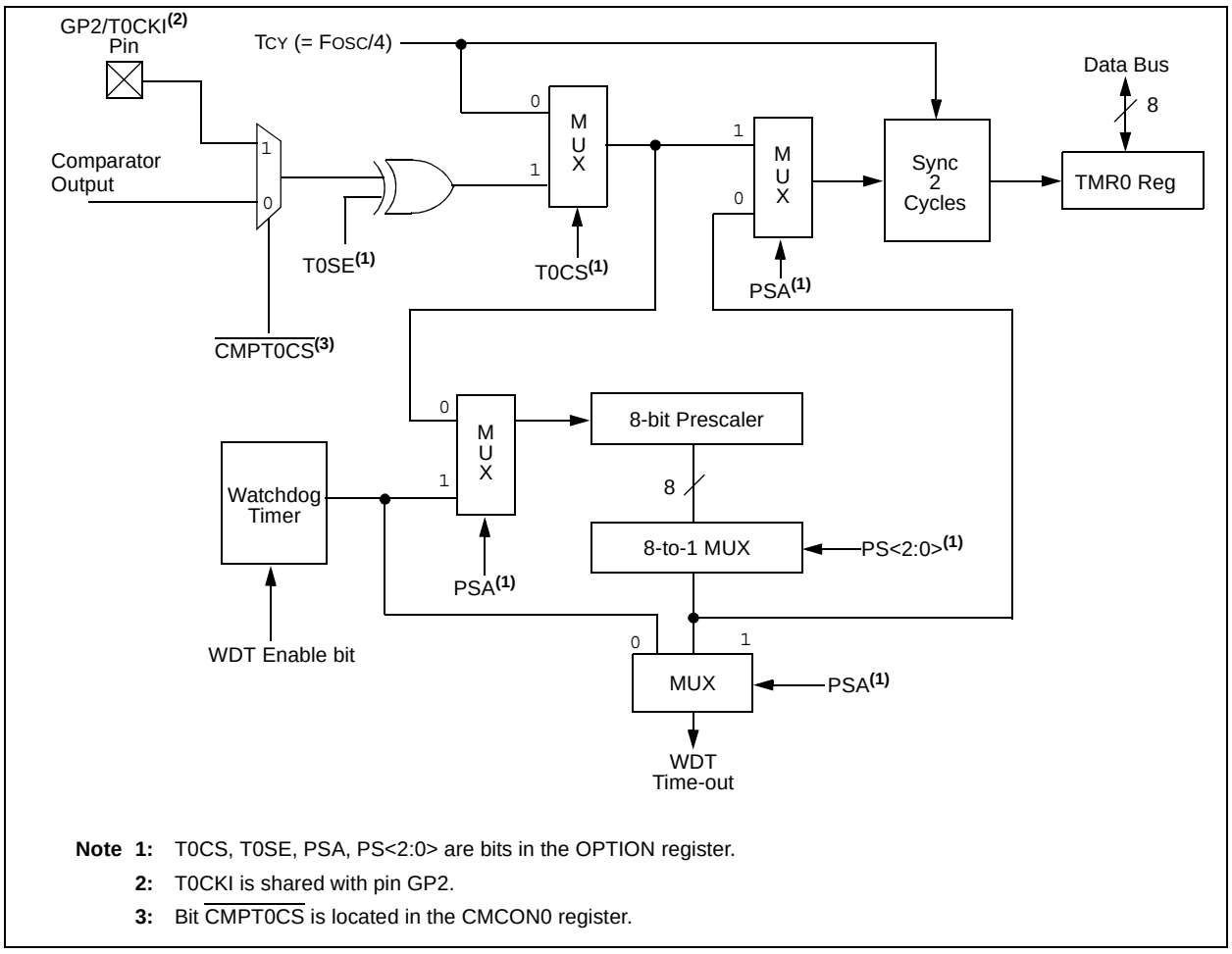
```
CLRWDT              ;Clear WDT
CLRF   TMR0         ;Clear TMR0 & Prescaler
MOVLW  '00xx1111'b  ;These 3 lines (5, 6, 7)
OPTION              ;are required only if
                    ;desired
CLRWDT              ;PS<2:0> are 000 or 001
MOVLW  '00xx1xxx'b  ;Set Postscaler to
OPTION              ;desired WDT rate
```

To change the prescaler from the WDT to the Timer0 module, use the sequence shown in Example 7.2. This sequence must be used even if the WDT is disabled. A `CLRWDT` instruction should be executed before switching the prescaler.

EXAMPLE 7-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT              ;Clear WDT and
                    ;prescaler
MOVLW  'xxxx0xxx'   ;Select TMR0, new
                    ;prescale value and
                    ;clock source
OPTION
```

FIGURE 7-5: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note 1: T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

2: T0CKI is shared with pin GP2.

3: Bit $\overline{\text{CMPT0CS}}$ is located in the CMCON0 register.

8.0 COMPARATOR MODULE

The comparator module contains one Analog comparator. The inputs to the comparator are multiplexed with GP0 and GP1 pins. The output of the comparator can be placed on GP2.

The CMCON0 register, shown in Register 8-1, controls the comparator operation. A block diagram of the comparator is shown in Figure 8-1.

REGISTER 8-1: CMCON0 REGISTER

R-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
CMPOUT	$\overline{\text{COUTEN}}$	POL	$\overline{\text{CMPT0CS}}$	CMPON	CNREF	CPREF	$\overline{\text{CWU}}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **CMPOUT:** Comparator Output bit
1 = $V_{IN}+ > V_{IN}-$
0 = $V_{IN}+ < V_{IN}-$

bit 6 **$\overline{\text{COUTEN}}$:** Comparator Output Enable bit(1, 2)
1 = Output of comparator is NOT placed on the COUT pin
0 = Output of comparator is placed in the COUT pin

bit 5 **POL:** Comparator Output Polarity bit(2)
1 = Output of comparator not inverted
0 = Output of comparator inverted

bit 4 **$\overline{\text{CMPT0CS}}$:** Comparator TMR0 Clock Source bit(2)
1 = TMR0 clock source selected by T0CS control bit
0 = Comparator output used as TMR0 clock source

bit 3 **CMPON:** Comparator Enable bit
1 = Comparator is on
0 = Comparator is off

bit 2 **CNREF:** Comparator Negative Reference Select bit(2)
1 = CIN- pin(3)
0 = Internal voltage reference

bit 1 **CPREF:** Comparator Positive Reference Select bit(2)
1 = CIN+ pin(3)
0 = CIN- pin(3)

bit 0 **$\overline{\text{CWU}}$:** Comparator Wake-up on Change Enable bit(2)
1 = Wake-up on comparator change is disabled
0 = Wake-up on comparator change is enabled.

Note 1: Overrides T0CS bit for TRIS control of GP2.

2: When the comparator is turned on, these control bits assert themselves. When the comparator is off, these bits have no effect on the device operation and the other control registers have precedence.

3: PIC10F204/206 only.

FIGURE 8-3: ANALOG INPUT MODE

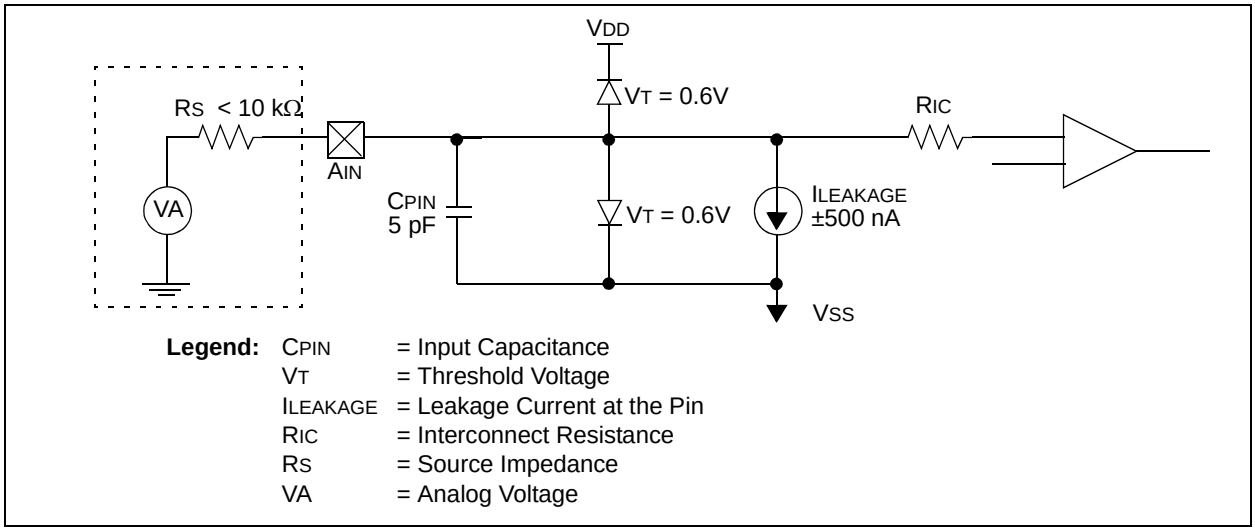


TABLE 8-2: REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other Resets
03h	STATUS	GPWUF	CWUF	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	00-1 1xxx	qq0q quuu
07h	CMCON0	CMPOUT	$\overline{COUTEN}$	POL	$\overline{CMPT0CS}$	CMPON	CNREF	CPREF	$\overline{CWU}$	1111 1111	uuuu uuuu
N/A	TRISGPIO	—	—	—	—	I/O Control Register				---- 1111	---- 1111

Legend: x = Unknown, u = Unchanged, – = Unimplemented, read as '0', q = Depends on condition.

FIGURE 9-2: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

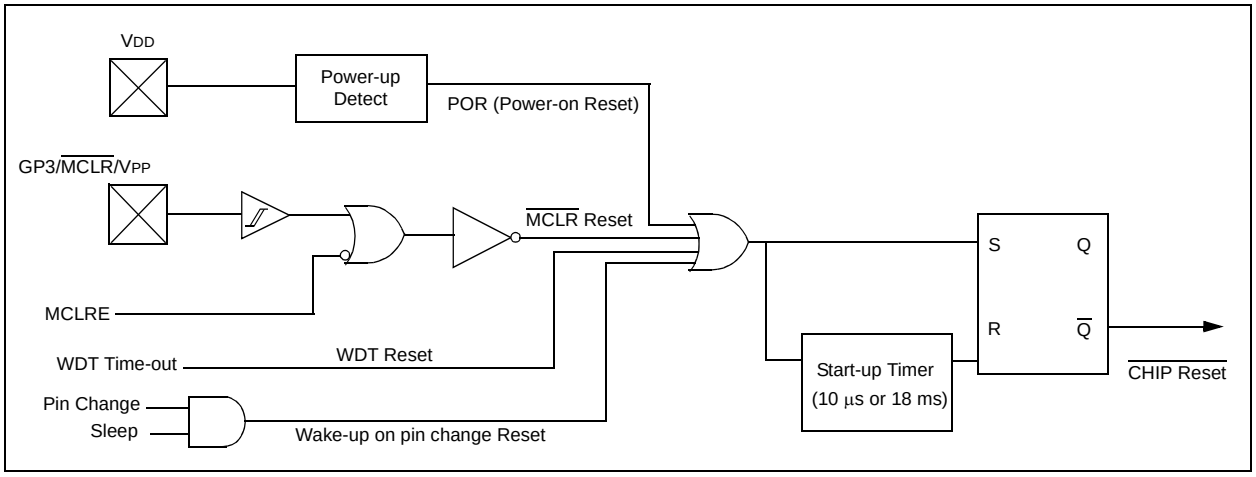


FIGURE 9-3: TIME-OUT SEQUENCE ON POWER-UP (MCLR PULLED LOW)

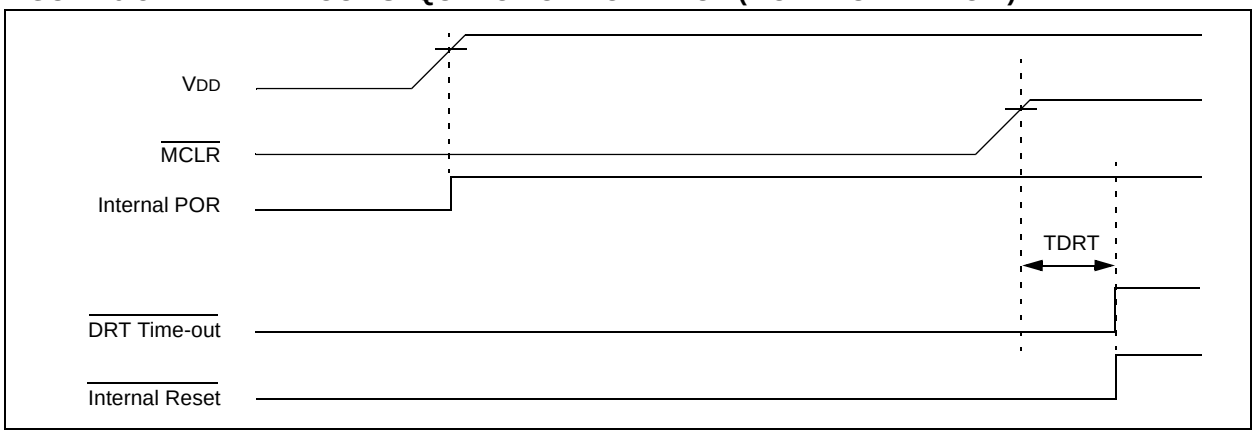


FIGURE 9-4: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): FAST VDD RISE TIME

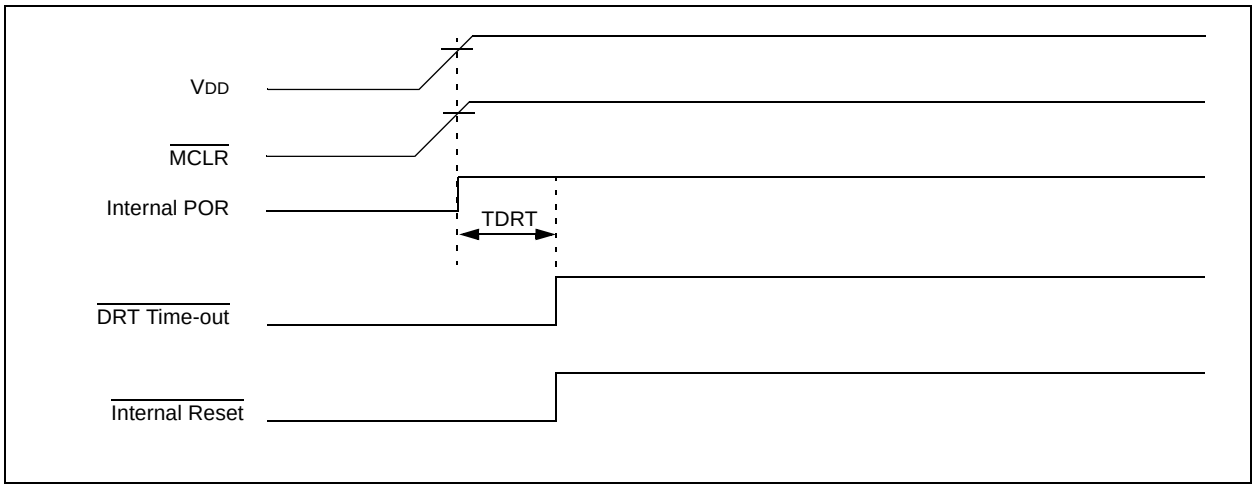
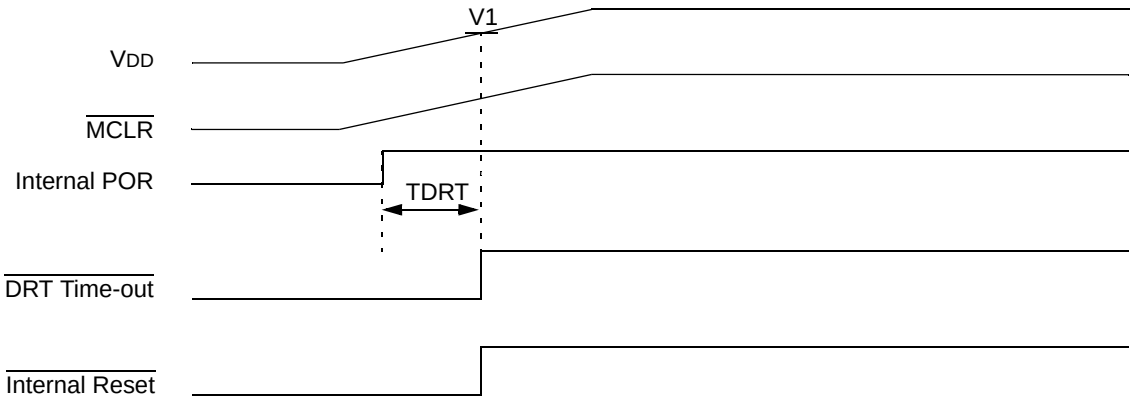


FIGURE 9-5: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO V_{DD}): SLOW V_{DD} RISE TIME



Note: When V_{DD} rises slowly, the T_{DRT} time-out expires long before V_{DD} has reached its final value. In this example, the chip will reset properly if, and only if, V1 ≥ V_{DD} min.

9.5 Device Reset Timer (DRT)

On the PIC10F200/202/204/206 devices, the DRT runs any time the device is powered-up.

The DRT operates on an internal oscillator. The processor is kept in Reset as long as the DRT is active. The DRT delay allows V_{DD} to rise above V_{DD} min. and for the oscillator to stabilize.

The on-chip DRT keeps the devices in a Reset condition for approximately 18 ms after $\overline{MCLR}$ has reached a logic high (V_{IH} $\overline{MCLR}$) level. Programming GP3/$\overline{MCLR}$/V_{PP} as $\overline{MCLR}$ and using an external RC network connected to the $\overline{MCLR}$ input is not required in most cases. This allows savings in cost-sensitive and/or space restricted applications, as well as allowing the use of the GP3/$\overline{MCLR}$/V_{PP} pin as a general purpose input.

The Device Reset Time delays will vary from chip-to-chip due to V_{DD}, temperature and process variation. See AC parameters for details.

Reset sources are POR, $\overline{MCLR}$, WDT time-out and wake-up on pin change. See **Section 9.9.2 "Wake-up from Sleep"**, Notes 1, 2 and 3.

TABLE 9-3: DRT PERIOD

Oscillator	POR Reset	Subsequent Resets
INTOSC	18 ms (typical)	10 μs (typical)

9.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator, which does not require any external components. This RC oscillator is separate from the internal 4 MHz oscillator. This means that the WDT will run even if the main processor clock has been stopped, for example, by execution of a SLEEP instruction. During normal operation or Sleep, a WDT Reset or wake-up Reset, generates a device Reset.

The $\overline{TO}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset.

The WDT can be permanently disabled by programming the configuration WDTE as a '0' (see **Section 9.1 "Configuration Bits"**). Refer to the PIC10F200/202/204/206 Programming Specifications to determine how to access the Configuration Word.

9.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, a time-out period of a nominal 2.3 seconds can be realized. These periods vary with temperature, V_{DD} and part-to-part process variations (see DC specs).

Under worst-case conditions (V_{DD} = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

9.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device Reset.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum Sleep time before a WDT wake-up Reset.

9.7 Time-out Sequence, Power-down and Wake-up from Sleep Status Bits (TO, PD, GPWUF, CWUF)

The $\overline{TO}$, $\overline{PD}$, GPWUF and CWUF bits in the STATUS register can be tested to determine if a Reset condition has been caused by a power-up condition, a $\overline{MCLR}$, Watchdog Timer (WDT) Reset, wake-up on comparator change or wake-up on pin change.

TABLE 9-5: $\overline{TO}$, $\overline{PD}$, GPWUF, CWUF STATUS AFTER RESET

CWUF	GPWUF	$\overline{TO}$	$\overline{PD}$	Reset Caused By
0	0	0	0	WDT wake-up from Sleep
0	0	0	u	WDT time-out (not from Sleep)
0	0	1	0	$\overline{MCLR}$ wake-up from Sleep
0	0	1	1	Power-up
0	0	u	u	$\overline{MCLR}$ not during Sleep
0	1	1	0	Wake-up from Sleep on pin change
1	0	1	0	Wake-up from Sleep on comparator change

Legend: u = unchanged, x = unknown, – = unimplemented bit, read as '0', q = value depends on condition.

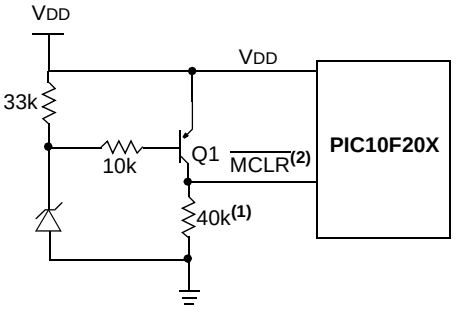
Note 1: The $\overline{TO}$, $\overline{PD}$, GPWUF and CWUF bits maintain their status (u) until a Reset occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{TO}$, $\overline{PD}$, GPWUF or CWUF Status bits.

9.8 Reset on Brown-out

A Brown-out Reset is a condition where device power (V_{DD}) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

To reset PIC10F200/202/204/206 devices when a Brown-out Reset occurs, external brown-out protection circuits may be built, as shown in Figure 9-7 and Figure 9-8.

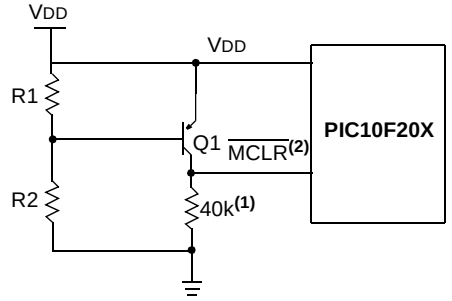
FIGURE 9-7: BROWN-OUT PROTECTION CIRCUIT 1



Note 1: This circuit will activate Reset when V_{DD} goes below Vz + 0.7V (where Vz = Zener voltage).

2: Pin must be confirmed as $\overline{MCLR}$.

FIGURE 9-8: BROWN-OUT PROTECTION CIRCUIT 2



Note 1: This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when V_{DD} is below a certain level such that:

$$V_{DD} \bullet \frac{R1}{R1 + R2} = 0.7V$$

2: Pin must be confirmed as $\overline{MCLR}$.

ADDWF	Add W and f
Syntax:	[*label*] ADDWF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(W) + (f) → (dest)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register and register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

ANDLW	AND literal with W
Syntax:	[*label*] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W).AND. (k) → (W)
Status Affected:	Z
Description:	The contents of the W register are AND'ed with the 8-bit literal 'k'. The result is placed in the W register.

ANDWF	AND W with f
Syntax:	[*label*] ANDWF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(W) .AND. (f) → (dest)
Status Affected:	Z
Description:	The contents of the W register are AND'ed with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

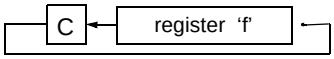
BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	$0 \le f \le 31$ $0 \le b \le 7$
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	Bit Set f
Syntax:	[*label*] BSF f,b
Operands:	$0 \le f \le 31$ $0 \le b \le 7$
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

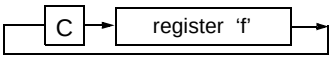
BTFSC	Bit Test f, Skip if Clear
Syntax:	[*label*] BTFSC f,b
Operands:	$0 \le f \le 31$ $0 \le b \le 7$
Operation:	skip if (f<b>) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', then the next instruction is skipped. If bit 'b' is '0', then the next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a 2-cycle instruction.

RETLW	Return with literal in W
Syntax:	[*label*] RETLW k
Operands:	$0 \le k \le 255$
Operation:	$k \rightarrow (W)$; $TOS \rightarrow PC$
Status Affected:	None
Description:	The W register is loaded with the 8-bit literal ‘k’. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.

RLF	Rotate Left f through Carry
Syntax:	[*label*] RLF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	See description below
Status Affected:	C
Description:	The contents of register ‘f’ are rotated one bit to the left through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.



RRF	Rotate Right f through Carry
Syntax:	[*label*] RRF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	See description below
Status Affected:	C
Description:	The contents of register ‘f’ are rotated one bit to the right through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.



SLEEP	Enter SLEEP Mode
Syntax:	[*label*] SLEEP
Operands:	None
Operation:	$00h \rightarrow WDT$; $0 \rightarrow$ WDT prescaler; $1 \rightarrow \overline{TO}$; $0 \rightarrow \overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$, RBWUF
Description:	Time-out Status bit ($\overline{TO}$) is set. The Power-down Status bit ($\overline{PD}$) is cleared. RBWUF is unaffected. The WDT and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped. See **Section 9.9 “Power-down Mode (Sleep)”** for more details.

SUBWF	Subtract W from f
Syntax:	[*label*] SUBWF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	$(f) - (W) \rightarrow (dest)$
Status Affected:	C, DC, Z
Description:	Subtract (2’s complement method) the W register from register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.

SWAPF	Swap Nibbles in f
Syntax:	[*label*] SWAPF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	$(f<3:0>) \rightarrow (dest<7:4>)$; $(f<7:4>) \rightarrow (dest<3:0>)$
Status Affected:	None
Description:	The upper and lower nibbles of register ‘f’ are exchanged. If ‘d’ is ‘0’, the result is placed in W register. If ‘d’ is ‘1’, the result is placed in register ‘f’.

12.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... 0 to +6.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} ..... 0 to +13.5V
Voltage on all other pins with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Total power dissipation(1) ..... 800 mW
Max. current out of V_{SS} pin ..... 80 mA
Max. current into V_{DD} pin ..... 80 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Max. output current sunk by any I/O pin ..... 25 mA
Max. output current sourced by any I/O pin ..... 25 mA
Max. output current sourced by I/O port ..... 75 mA
Max. output current sunk by I/O port ..... 75 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

†NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

12.2 DC Characteristics: PIC10F200/202/204/206 (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +125°C (extended)				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	2.0		5.5	V	See Figure 12-1
D002	VDR	**RAM Data Retention Voltage(2)**	1.5*		—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	Vss	—	V	
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	
D010	IDD	**Supply Current(3)**					
			— —	175 0.63	275 1.1	μA mA	VDD = 2.0V VDD = 5.0V
D020	IPD	**Power-down Current(4)**					
			— —	0.1 0.35	9 15	μA μA	VDD = 2.0V VDD = 5.0V
D022	IWDT	**WDT Current(5)**					
			— —	1.0 7	18 22	μA μA	VDD = 2.0V VDD = 5.0V
D023	ICMP	**Comparator Current(5)**					
			— —	12 42	27 85	μA μA	VDD = 2.0V VDD = 5.0V
D024	VREF	**Internal Reference Current(5,6)**					
			—	85 175	120 200	μA μA	VDD = 2.0V VDD = 5.0V

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ.") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: All I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in Sleep mode.

4: Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS.

5: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled.

6: Measured with the Comparator enabled.

12.3 DC Characteristics: PIC10F200/202/204/206 (Industrial, Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating temperature -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended) Operating voltage VDD range as described in DC specification				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O ports:					
D030		with TTL buffer	Vss	—	0.8	V	For all 4.5V ≤ VDD ≤ 5.5V
D030A			Vss	—	0.15 VDD	V	
D031		with Schmitt Trigger buffer	Vss	—	0.2 VDD	V	
D032		$\overline{MCLR}$, T0CKI	Vss	—	0.2 VDD	V	
	VIH	**Input High Voltage**					
		I/O ports:		—			
D040		with TTL buffer	2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.25 VDD + 0.8	—	VDD	V	Otherwise
D041		with Schmitt Trigger buffer	0.8VDD	—	VDD	V	For entire VDD range
D042		$\overline{MCLR}$, T0CKI	0.8VDD	—	VDD	V	
D070	IPUR	**GPIO weak pull-up current(3)**	50	250	400	µA	VDD = 5V, VPIN = VSS
	IIL	**Input Leakage Current(1, 2)**					
D060		I/O ports	—	±0.1	± 1	µA	Vss ≤ VPIN ≤ VDD, Pin at high-impedance
D061		GP3/$\overline{MCLR}$(3)	—	±0.7	± 5	µA	Vss ≤ VPIN ≤ VDD
		Output Low Voltage					
D080		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D080A			—	—	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
		Output High Voltage					
D090		I/O ports(2)	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D090A			VDD – 0.7	—	—	V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
		Capacitive Loading Specs on Output Pins					
D101		All I/O pins	—	—	50*	pF	

† Data in "Typ." column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

* These parameters are for design guidance only and are not tested.

Note 1: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

2: Negative current is defined as coming out of the pin.

3: This specification applies when GP3/$\overline{MCLR}$ is configured as an input with pull-up disabled. The leakage current of the $\overline{MCLR}$ circuit is higher than the standard I/O logic.

FIGURE 13-4: COMPARATOR IPD vs. VDD (COMPARATOR ENABLED)

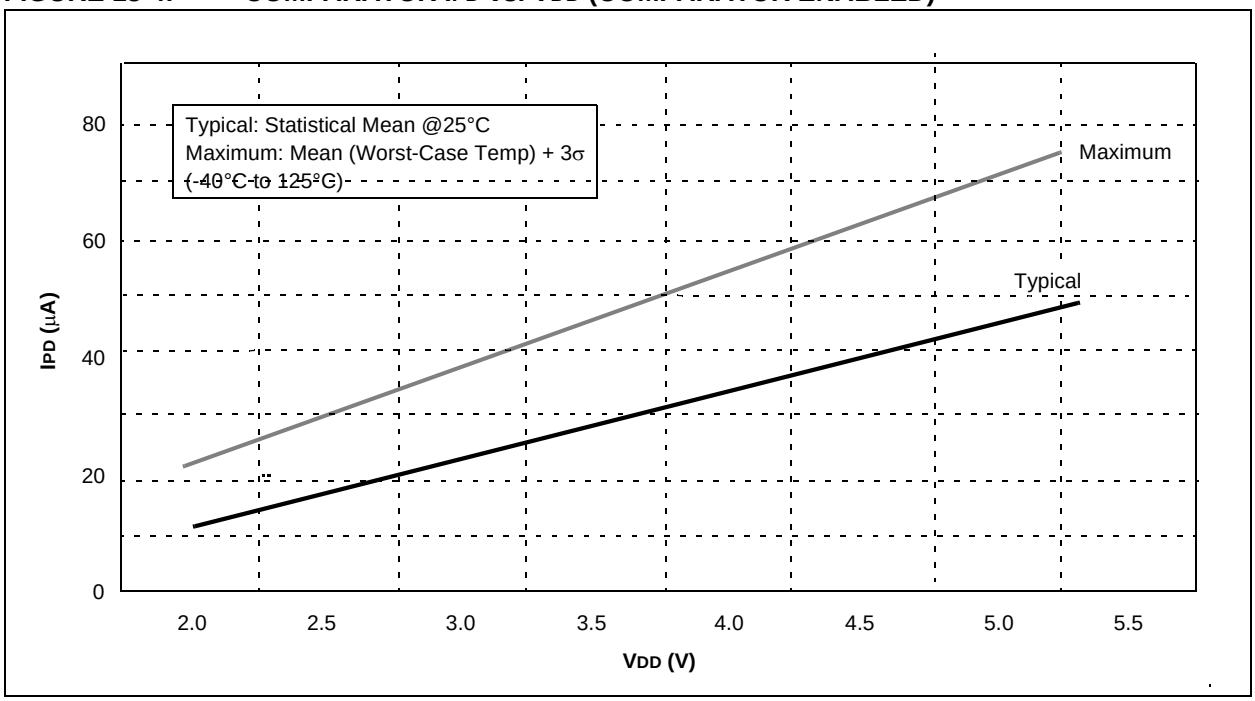


FIGURE 13-5: TYPICAL WDT IPD vs. VDD

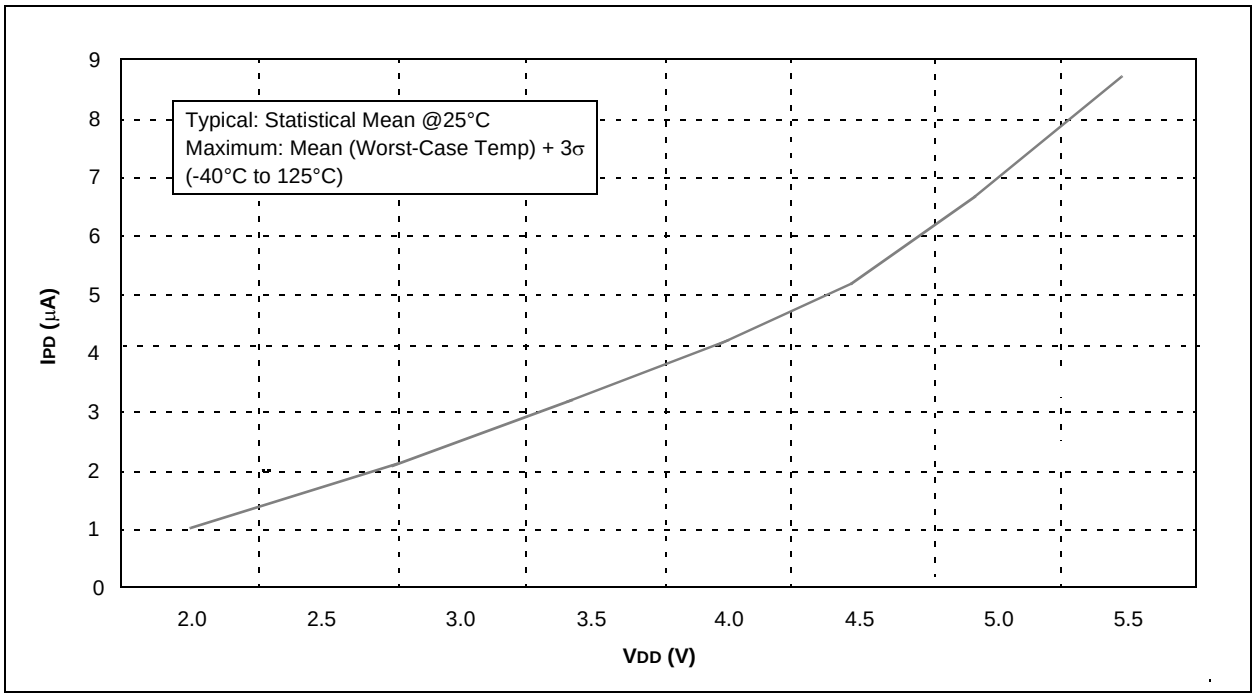


FIGURE 13-8: VOL vs. IOL OVER TEMPERATURE (VDD = 3.0V)

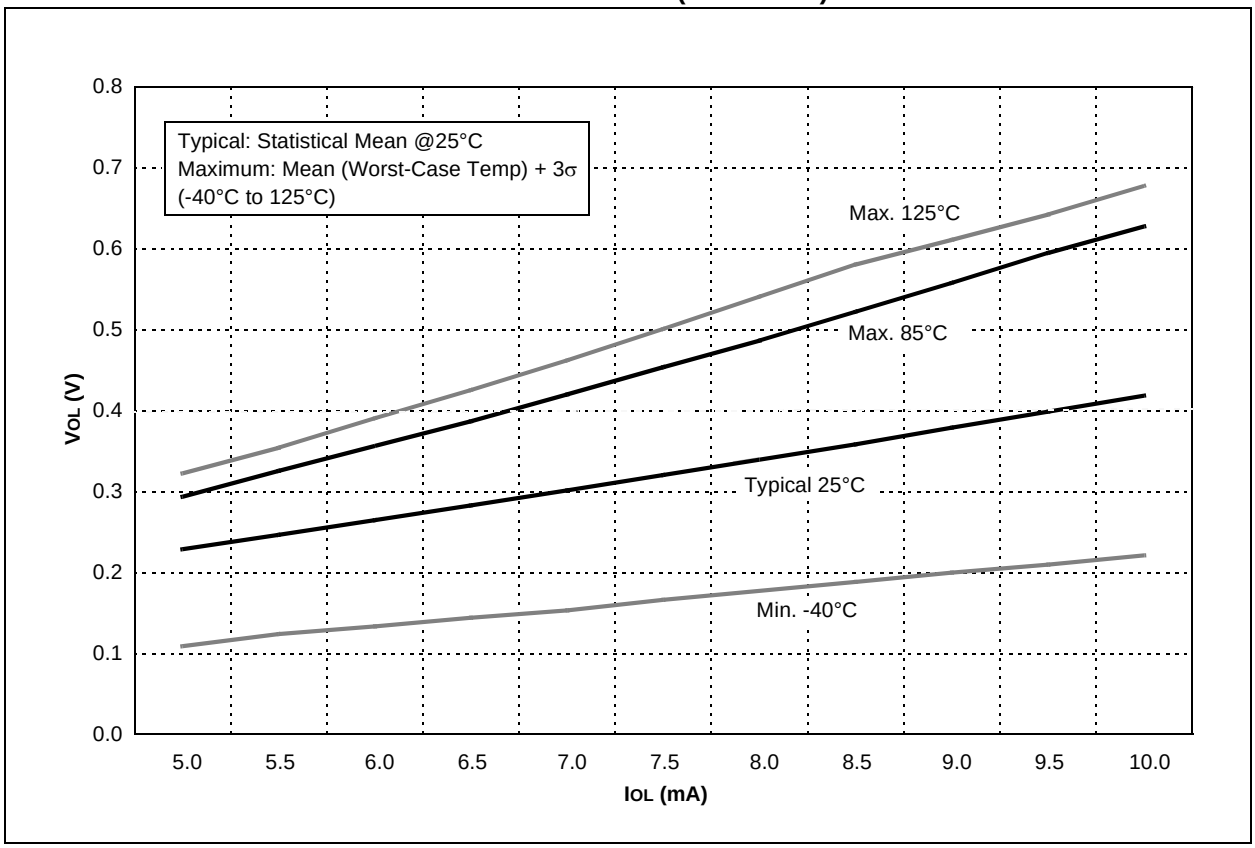


FIGURE 13-9: VOL vs. IOL OVER TEMPERATURE (VDD = 5.0V)

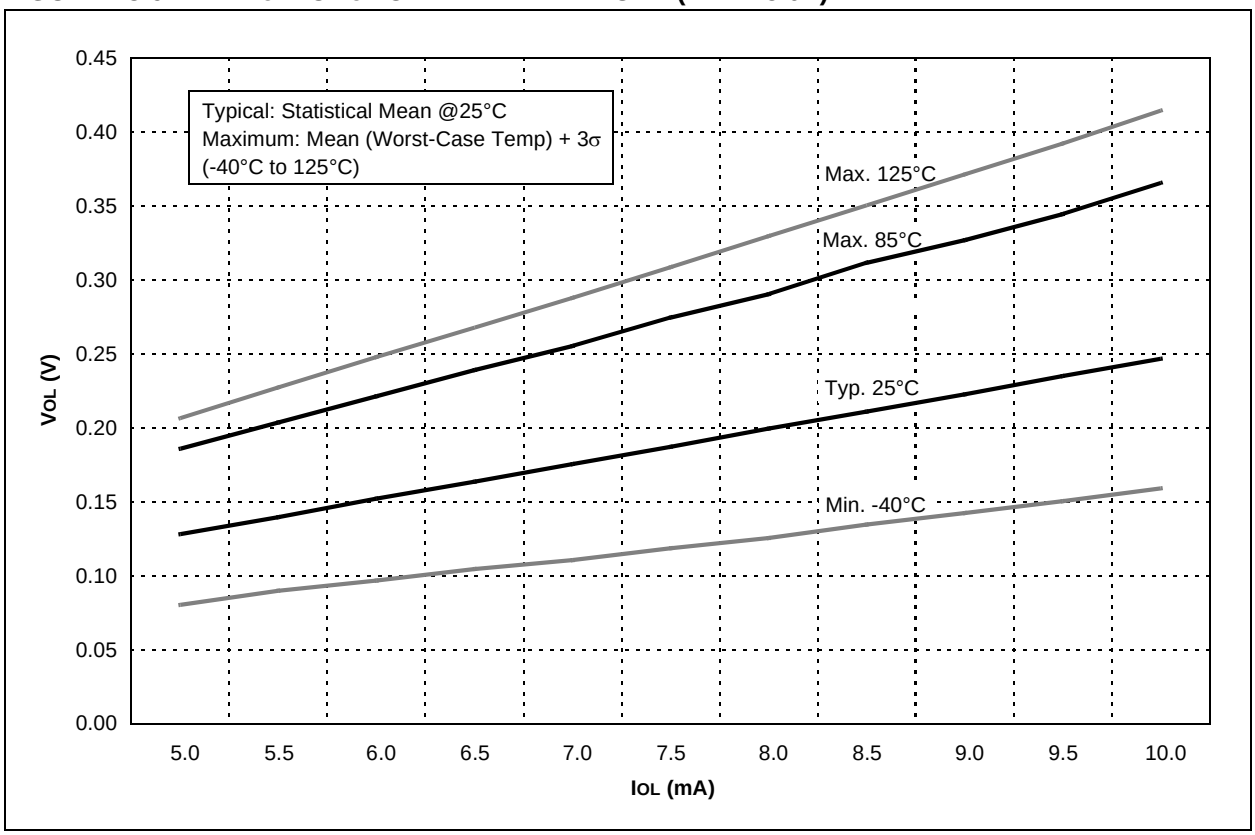


FIGURE 13-12: TTL INPUT THRESHOLD VIN VS. VDD

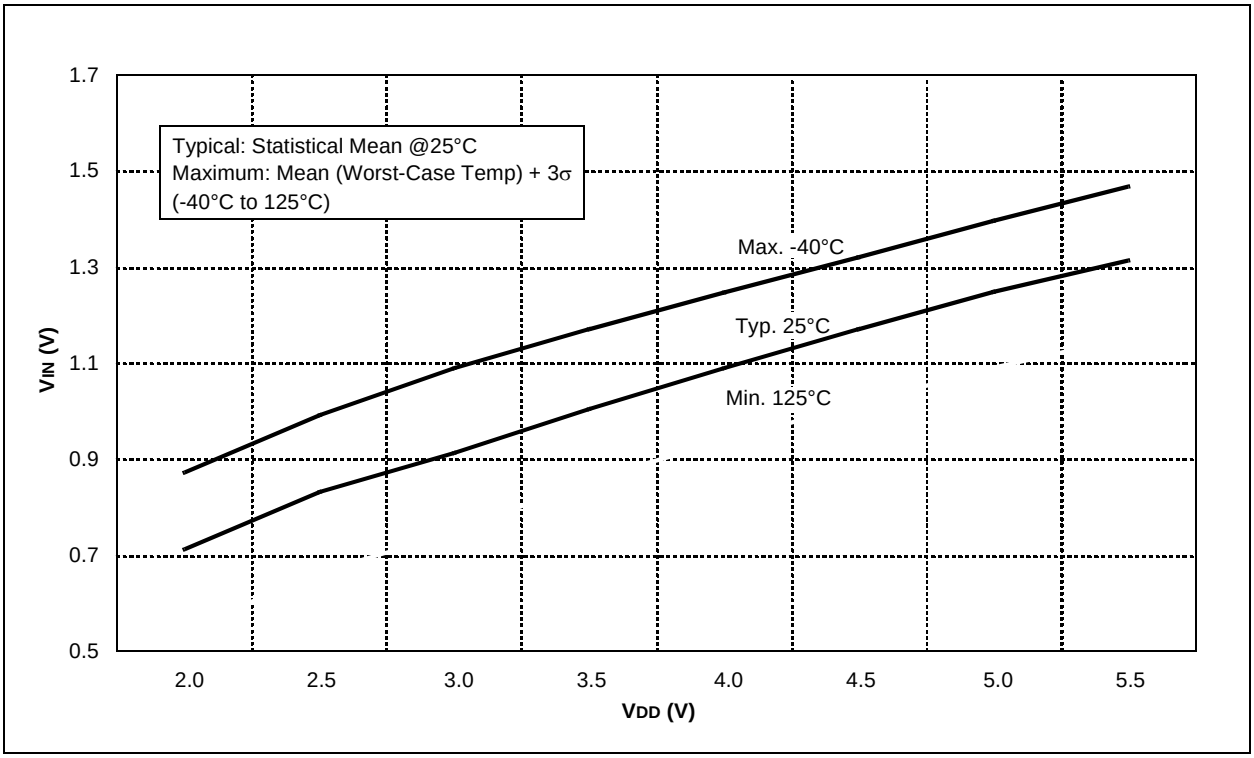
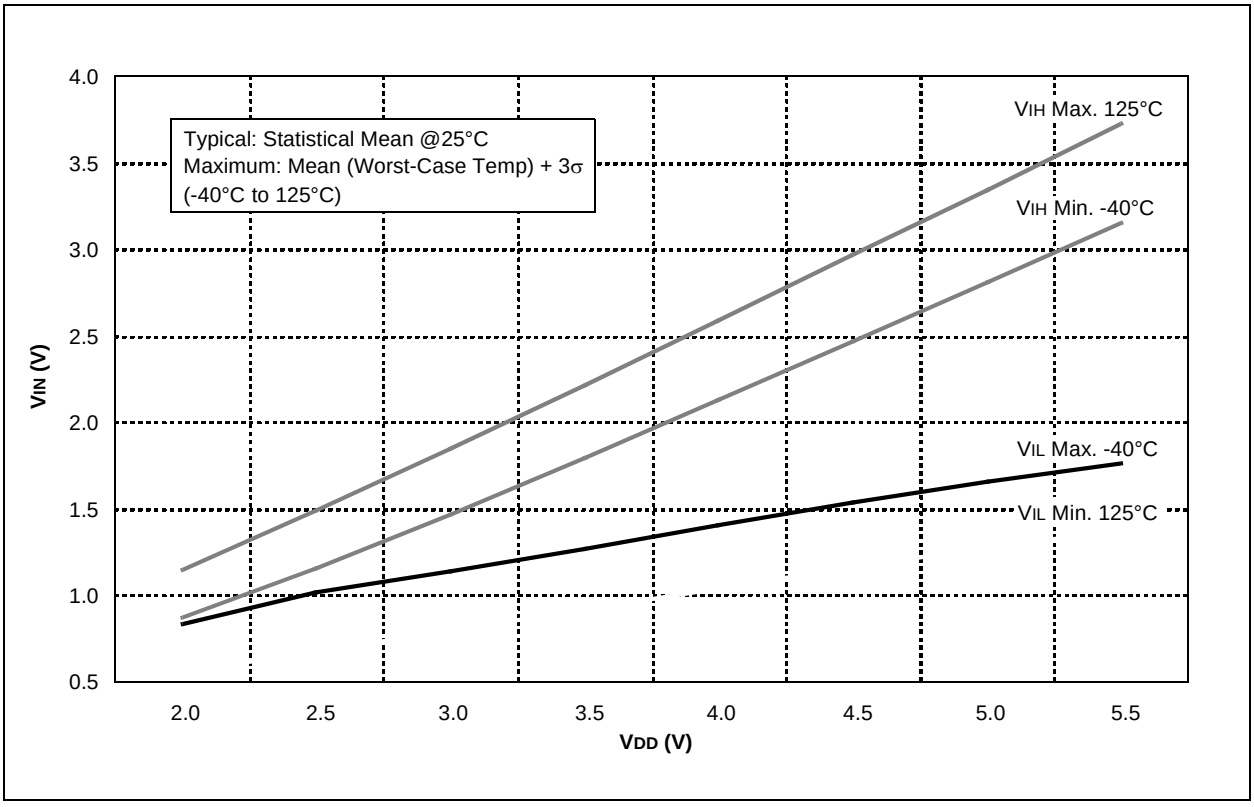
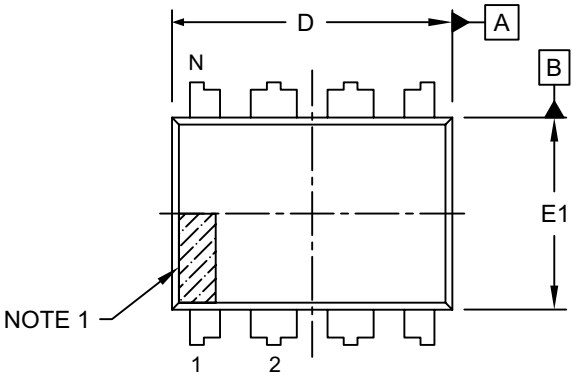


FIGURE 13-13: SCHMITT TRIGGER INPUT THRESHOLD VIN VS. VDD

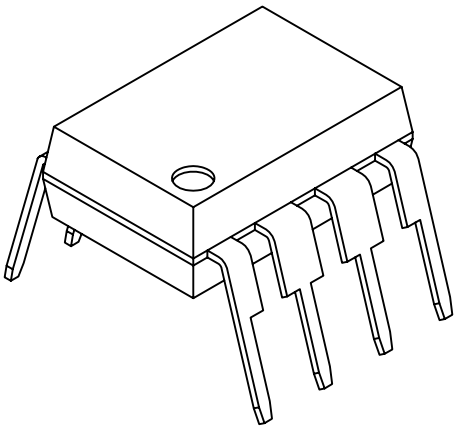


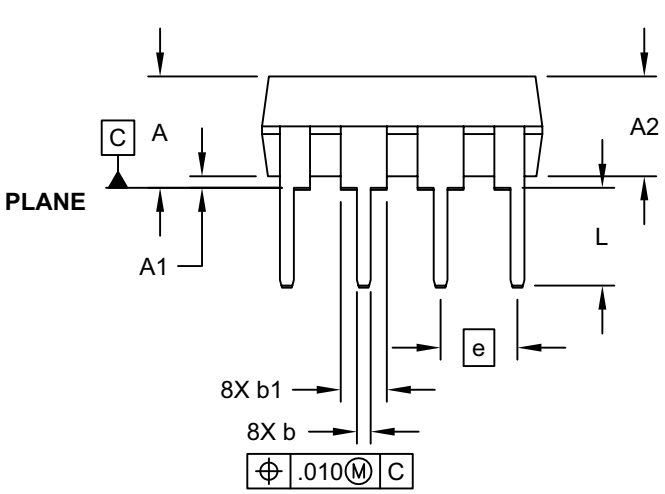
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

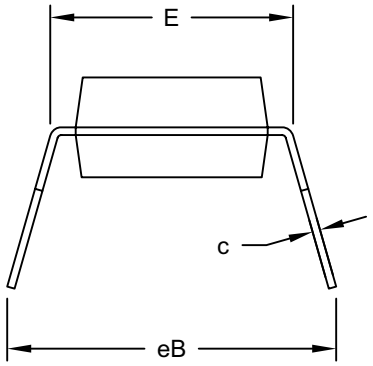


TOP VIEW





SIDE VIEW



END VIEW

Microchip Technology Drawing No. C04-018D Sheet 1 of 2

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