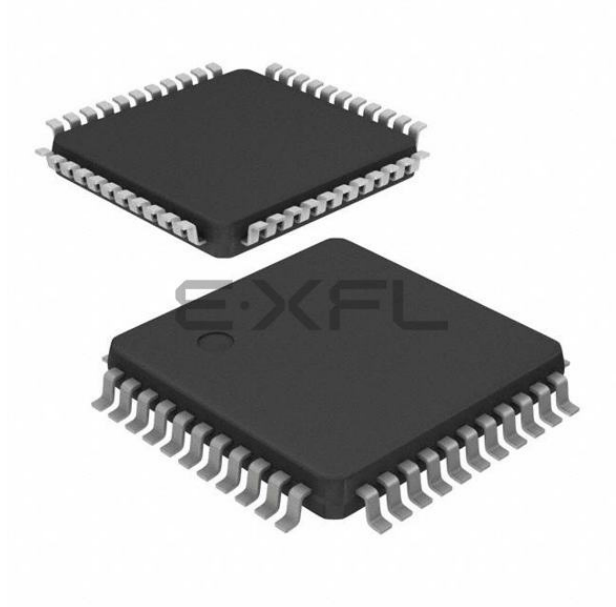

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87c52x2fbd-157

PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER DIP	PLCC	LQFP	TSSOP	TYPE	NAME AND FUNCTION
V_{SS}	20	22	16	9	I	**Ground:** 0 V reference.
V_{CC}	40	44	38	29	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0-0.7	39–32	43–36	37–30	28–21	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification and received code bytes during EPROM programming. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	40–44, 1–3	30–37	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 also receives the low-order address byte during program memory verification. Alternate functions for Port 1 include:
	1	2	40	30	I/O	**T2 (P1.0):** Timer/Counter 2 external count input/clockout (see Programmable Clock-Out)
	2	3	41	31	I	**T2EX (P1.1):** Timer/Counter 2 Reload/Capture/Direction control
P2.0–P2.7	21–28	24–31	18–25	10–17	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. Some Port 2 pins receive the high order address bits during EPROM programming and verification.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	1–6	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	10	11	5	1	I	**RxD (P3.0):** Serial input port
	11	13	7	2	O	**TxD (P3.1):** Serial output port
	12	14	8		I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt[1]
	13	15	9	3	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt
	14	16	10	4	I	**T0 (P3.4):** Timer 0 external input
	15	17	11		I	**T1 (P3.5):** Timer 1 external input[1]
	16	18	12	5	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe
	17	19	13	6	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe
RST	9	10	4	38	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE/$\overline{\text{PROG}}$	30	33	27	19	O	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (12-clock Mode) or 1/3 (6-clock Mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during EPROM programming. ALE can be disabled by setting SFR auxiliary.0. With this bit set, ALE will be active only during a MOVX instruction.

Table 4. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL}$2	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud rate generator
X	X	0	(off)

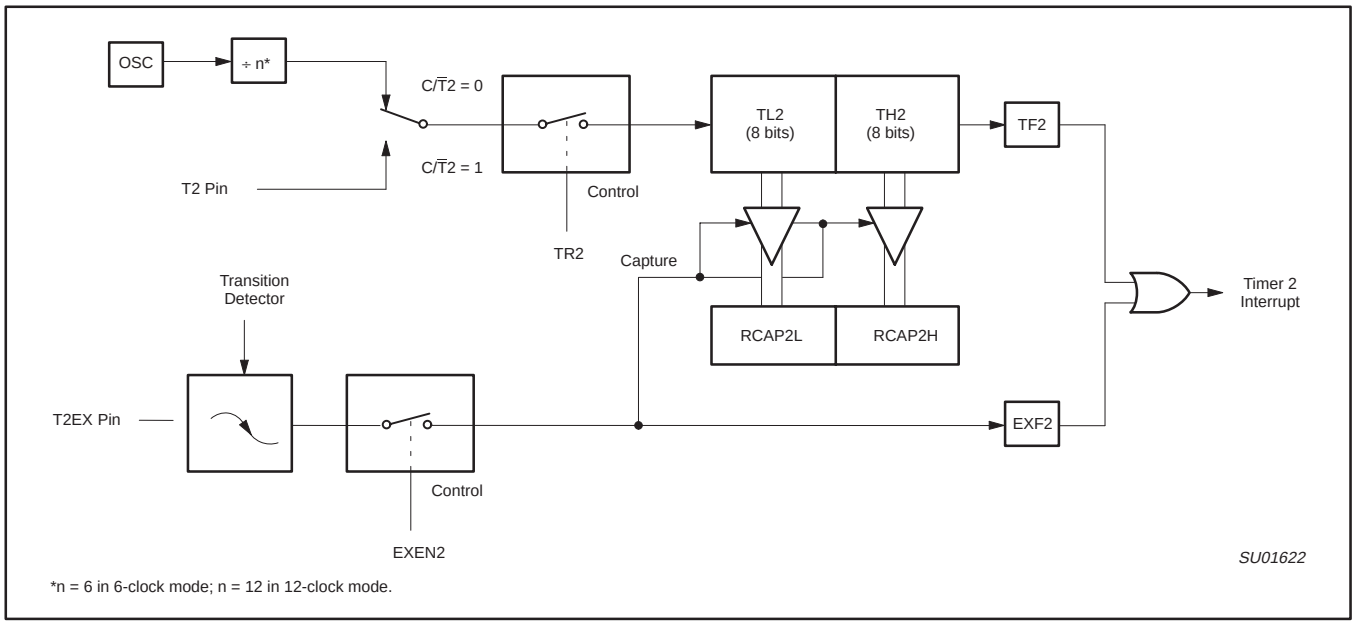
T2CON Address = C8H Reset Value = 00H
Bit Addressable

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T}$2	CP/$\overline{RL}$2

Symbol	Position	Name and Significance
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/$\overline{T}$2	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/12 in 12-clock mode or OSC/6 in 6-clock mode) 1 = External event counter (falling edge triggered).
CP/$\overline{RL}$2	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

SU01621

Figure 6. Timer/Counter 2 (T2CON) Control Register



*n = 6 in 6-clock mode; n = 12 in 12-clock mode.

Figure 7. Timer 2 in Capture Mode

T2MOD Address = 0C9H Reset Value = XXXX XX00B

Not Bit Addressable

7	6	5	4	3	2	1	0
—	—	—	—	—	—	T2OE	DCEN

Symbol	Position	Function
—		Not implemented, reserved for future use.*
T2OE	T2MOD.1	Timer 2 Output Enable bit.
DCEN	T2MOD.0	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

SU01519

Figure 8. Timer 2 Mode (T2MOD) Control Register

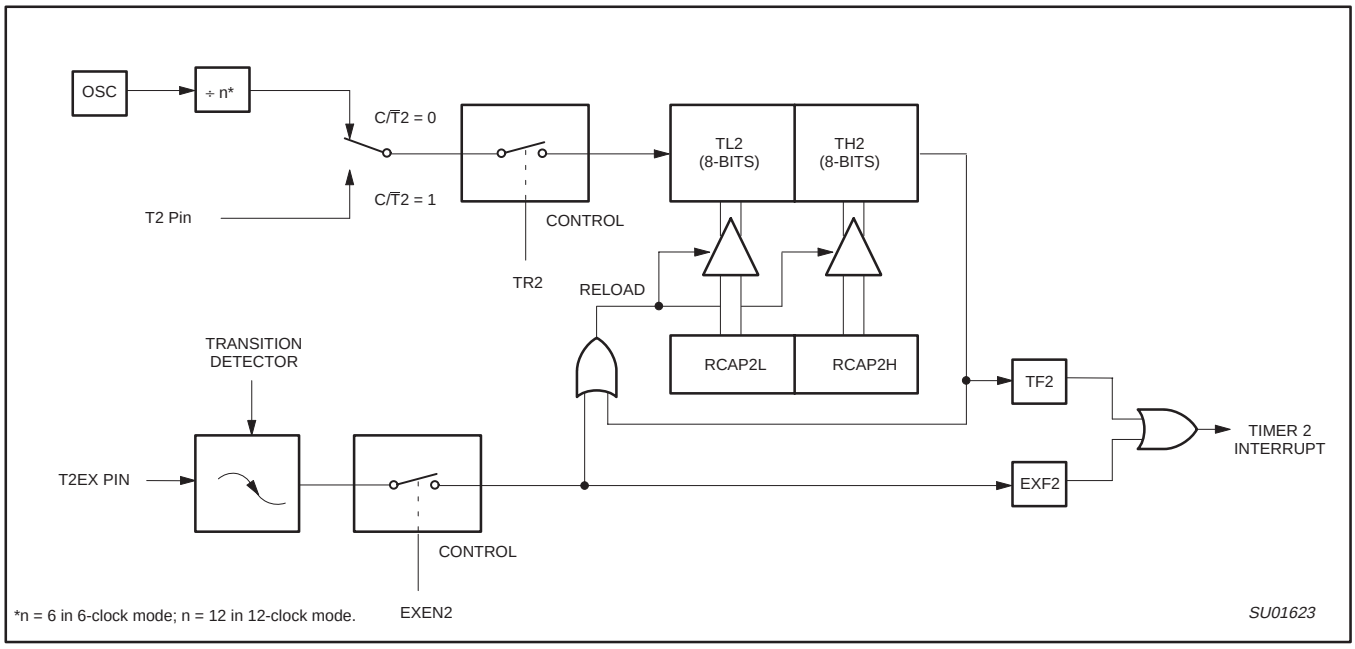


Figure 9. Timer 2 in Auto-Reload Mode (DCEN = 0)

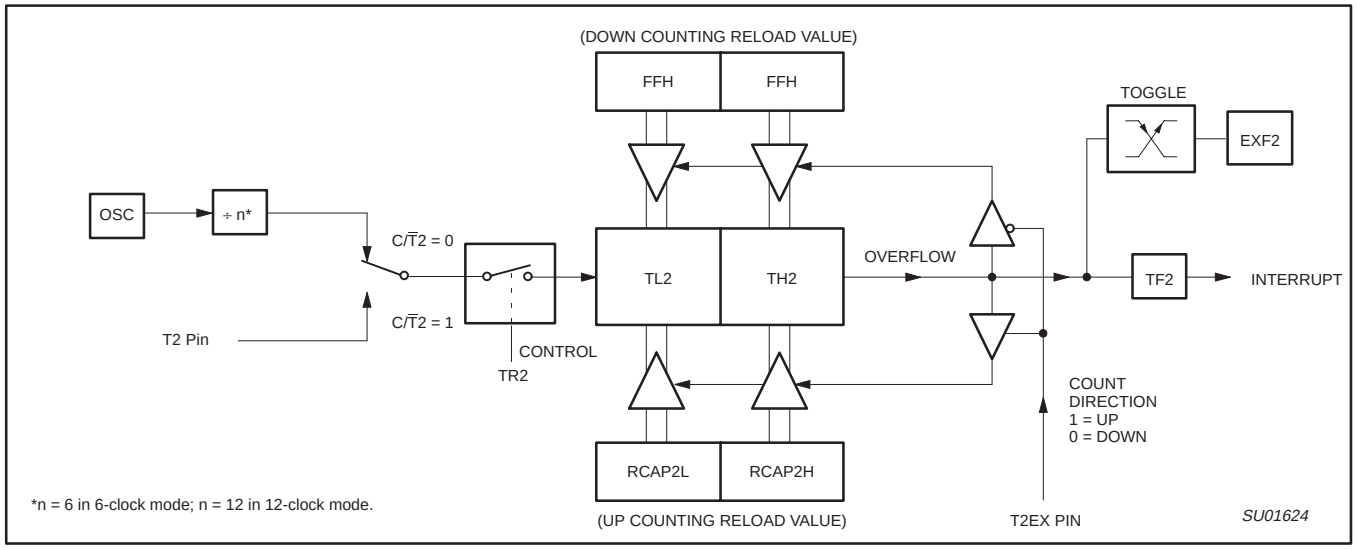


Figure 10. Timer 2 Auto Reload Mode (DCEN = 1)

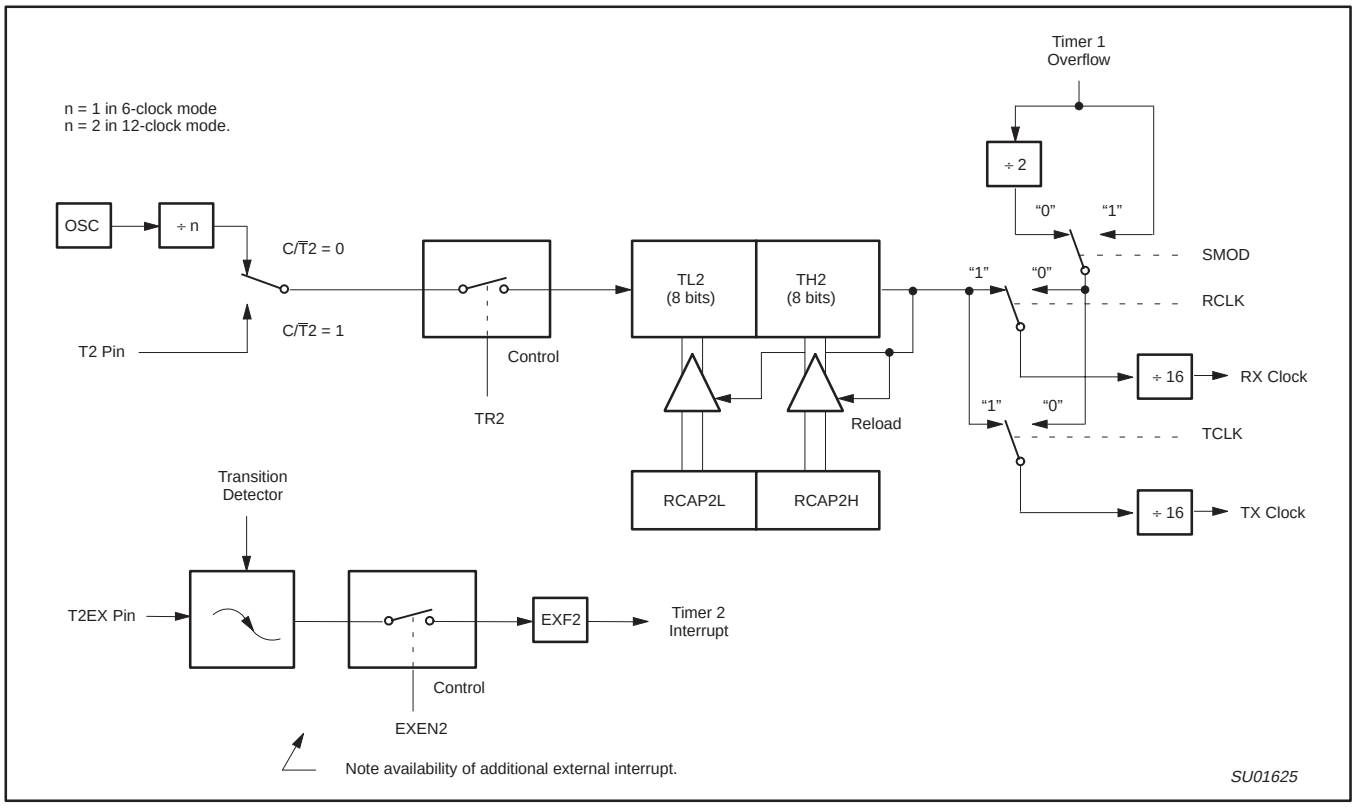


Figure 11. Timer 2 in Baud Rate Generator Mode

Baud Rate Generator Mode

Bits TCLK and/or RCLK in T2CON (Table 4) allow the serial port transmit and receive baud rates to be derived from either Timer 1 or Timer 2. When TCLK= 0, Timer 1 is used as the serial port transmit baud rate generator. When TCLK= 1, Timer 2 is used as the serial port transmit baud rate generator. RCLK has the same effect for the serial port receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates – one generated by Timer 1, the other by Timer 2.

Figure 11 shows the Timer 2 in baud rate generation mode. The baud rate generation mode is like the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in modes 1 and 3 are determined by Timer 2's overflow rate given below:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The timer can be configured for either "timer" or "counter" operation. In many applications, it is configured for "timer" operation (C/$\overline{T}$2=0). Timer operation is different for Timer 2 when it is being used as a baud rate generator.

Usually, as a timer it would increment every machine cycle (i.e., 1/6 the oscillator frequency in 6-clock mode or 1/12 the oscillator frequency in 12-clock mode). As a baud rate generator, it increments at the oscillator frequency in 6-clock mode or at 1/2 the oscillator frequency in 12-clock mode. Thus the baud rate formula is as follows:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Oscillator Frequency}}{[n \times [65536 - (\text{RCAP2H, RCAP2L})]]}$$

Where:

n = 16 in 6-clock mode, 32 in 12-clock mode.

(RCAP2H, RCAP2L)= The content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Timer 2 as a baud rate generator mode shown in Figure 11 is valid only if RCLK and/or TCLK = 1 in T2CON register. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Thus, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Also if the EXEN2 (T2 external enable flag) is set, a 1-to-0 transition in T2EX (Timer/counter 2 trigger input) will set EXF2 (T2 external flag) but will not cause a reload from (RCAP2H, RCAP2L) to (TH2,TL2). Therefore when Timer 2 is in use as a baud rate generator, T2EX can be used as an additional external interrupt, if needed.

When Timer 2 is in the baud rate generator mode, one should not try to read or write TH2 and TL2. As a baud rate generator, Timer 2 is incremented every state time (osc/2) or asynchronously from pin T2; under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Table 5 shows commonly used baud rates and how they can be obtained from Timer 2.

FULL-DUPLEX ENHANCED UART

Standard UART operation

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost.) The serial port receive and transmit registers are both accessed at Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

Mode 0: Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 the oscillator frequency in 12-clock mode or 1/6 the oscillator frequency in 6-clock mode.

Mode 1: 10 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register SCON. The baud rate is variable.

Mode 2: 11 bits are transmitted (through TxD) or received (through RxD): start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On Transmit, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency in 12-clock mode or 1/16 or 1/32 the oscillator frequency in 6-clock mode.

Mode 3: 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

Multiprocessor Communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. A way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that weren't being addressed leave their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

Serial Port Control Register

The serial port control and status register is the Special Function Register SCON, shown in Figure 12. This register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Baud Rates

The baud rate in Mode 0 is fixed: Mode 0 Baud Rate = Oscillator Frequency / 12 (12-clock mode) or / 6 (6-clock mode). The baud rate in Mode 2 depends on the value of bit SMOD in Special Function Register PCON. If SMOD = 0 (which is the value on reset), and the port pins in 12-clock mode, the baud rate is 1/64 the oscillator frequency. If SMOD = 1, the baud rate is 1/32 the oscillator frequency. In 6-clock mode, the baud rate is 1/32 or 1/16 the oscillator frequency, respectively.

Mode 2 Baud Rate =

$$\frac{2^{SMOD}}{n} \times (\text{Oscillator Frequency})$$

Where:

n = 64 in 12-clock mode, 32 in 6-clock mode

The baud rates in Modes 1 and 3 are determined by the Timer 1 or Timer 2 overflow rate.

Using Timer 1 to Generate Baud Rates

When Timer 1 is used as the baud rate generator (T2CON.RCLK = 0, T2CON.TCLK = 0), the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

Mode 1, 3 Baud Rate =

$$\frac{2^{SMOD}}{n} \times (\text{Timer 1 Overflow Rate})$$

Where:

n = 32 in 12-clock mode, 16 in 6-clock mode

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either "timer" or "counter" operation, and in any of its 3 running modes. In the most typical applications, it is configured for "timer" operation, in the auto-reload mode (high nibble of TMOD = 0010B). In that case the baud rate is given by the formula:

Mode 1, 3 Baud Rate =

$$\frac{2^{SMOD}}{n} \times \frac{\text{Oscillator Frequency}}{12 \times [256-(TH1)]}$$

Where:

n = 32 in 12-clock mode, 16 in 6-clock mode

One can achieve very low baud rates with Timer 1 by leaving the Timer 1 interrupt enabled, and configuring the Timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload. Figure 13 lists various commonly used baud rates and how they can be obtained from Timer 1.

Enhanced UART operation

In addition to the standard operation modes, the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 18). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 19.

Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the “Given” address or the “Broadcast” address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 20.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave’s address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are “don’t care”. The SADEN mask can be logically ANDed with the SADDR to create the “Given” address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0	SADDR	=	1100 0000
	SADEN	=	1111 1101
	Given	=	1100 00X0
Slave 1	SADDR	=	1100 0000
	SADEN	=	1111 1110
	Given	=	1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0	SADDR	=	1100 0000
	SADEN	=	1111 1001
	Given	=	1100 0XX0
Slave 1	SADDR	=	1110 0000
	SADEN	=	1111 1010
	Given	=	1110 0X0X
Slave 2	SADDR	=	1110 0000
	SADEN	=	1111 1100
	Given	=	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are trended as don’t-cares. In most cases, interpreting the don’t-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are leaded with 0s. This produces a given address of all “don’t cares” as well as a Broadcast address of all “don’t cares”. This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

SCON Address = 98H

Bit Addressable

Reset Value = 0000 0000B

7	6	5	4	3	2	1	0
SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

(SMOD0 = 0/1)*

Symbol	Position	Function
FE	SCON.7	Framing Error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit.*
SM0	SCON.7	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)
SM1	SCON.6	Serial Port Mode Bit 1

SM0	SM1	Mode	Description	Baud Rate**
0	0	0	shift register	f_{OSC}/12 (12-clk mode) or f_{OSC}/6 (6-clk mode)
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	f_{OSC}/64 or f_{OSC}/32 or f_{OSC}/16 (6-clock mode) or f_{OSC}/32 (12-clock mode)
1	1	3	9-bit UART	variable

SM2	SCON.5	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
REN	SCON.4	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	SCON.3	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
RB8	SCON.2	In modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	SCON.1	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	SCON.0	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

NOTES:
*SMOD0 is located at PCON.6.
**f_{OSC} = oscillator frequency

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Figure 18. SCON: Serial Port Control Register

Interrupt Priority Structure

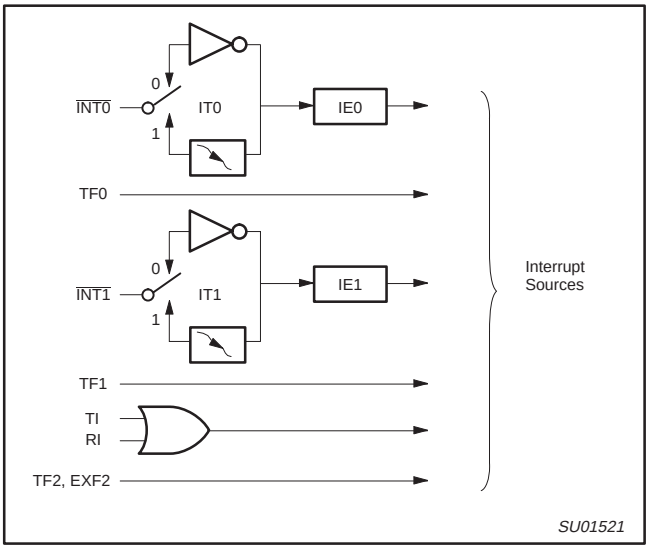


Figure 21. Interrupt Sources

Interrupts

The devices described in this data sheet provide six interrupt sources. These are shown in Figure 21. The External Interrupts $\overline{INT0}$ and $\overline{INT1}$ can each be either level-activated or transition-activated, depending on bits IT0 and IT1 in Register TCON. The flags that actually generate these interrupts are bits IE0 and IE1 in TCON. When an external interrupt is generated, the flag that generated it is cleared by the hardware when the service routine is vectored to only if the interrupt was transition-activated. If the interrupt was level-activated, then the external requesting source is what controls the request flag, rather than the on-chip hardware.

The Timer 0 and Timer 1 Interrupts are generated by TF0 and TF1, which are set by a rollover in their respective Timer/Counter registers (except see Timer 0 in Mode 3). When a timer interrupt is generated, the flag that generated it is cleared by the on-chip hardware when the service routine is vectored to.

The Serial Port Interrupt is generated by the logical OR of RI and TI. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine will normally have to determine whether it was RI or TI that generated the interrupt, and the bit will have to be cleared in software.

All of the bits that generate interrupts can be set or cleared by software, with the same result as though it had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be canceled in software.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE (Figure 22). IE also contains a global disable bit, $\overline{EA}$, which disables all interrupts at once.

Priority Level Structure

Each interrupt source can also be individually programmed to one of four priority levels by setting or clearing bits in Special Function Registers IP (Figure 23) and IPH (Figure 24). A lower-priority interrupt can itself be interrupted by a higher-priority interrupt, but not by another interrupt of the same level. A high-priority level 3 interrupt can't be interrupted by any other interrupt source.

If two request of different priority levels are received simultaneously, the request of higher priority level is serviced. If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as follows:

Source	Priority Within Level
1. IE0 (External Int 0)	(highest)
2. TF0 (Timer 0)	
3. IE1 (External Int 1)	
4. TF1 (Timer 1)	
5. RI+TI (UART)	
6. TF2, EXF2 (Timer 2)	(lowest)

Note that the "priority within level" structure is only used to resolve simultaneous requests of the same priority level.

The IP and IPH registers contain a number of unimplemented bits. User software should not write 1s to these positions, since they may be used in other 80C51 Family products.

How Interrupts Are Handled

The interrupt flags are sampled at S5P2 of every machine cycle. The samples are polled during the following machine cycle. If one of the flags was in a set condition at S5P2 of the preceding cycle, the polling cycle will find it and the interrupt system will generate an LCALL to the appropriate service routine, provided this hardware-generated LCALL is not blocked by any of the following conditions:

1. An interrupt of equal or higher priority level is already in progress.
2. The current (polling) cycle is not the final cycle in the execution of the instruction in progress.
3. The instruction in progress is RETI or any write to the IE or IP registers.

Any of these three conditions will block the generation of the LCALL to the interrupt service routine. Condition 2 ensures that the instruction in progress will be completed before vectoring to any service routine. Condition 3 ensures that if the instruction in progress is RETI or any access to IE or IP, then at least one more instruction will be executed before any interrupt is vectored to.

The polling cycle is repeated with each machine cycle, and the values polled are the values that were present at S5P2 of the previous machine cycle. Note that if an interrupt flag is active but not being responded to for one of the above conditions, if the flag is not still active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the fact that the interrupt flag was once active but not serviced is not remembered. Every polling cycle is new.

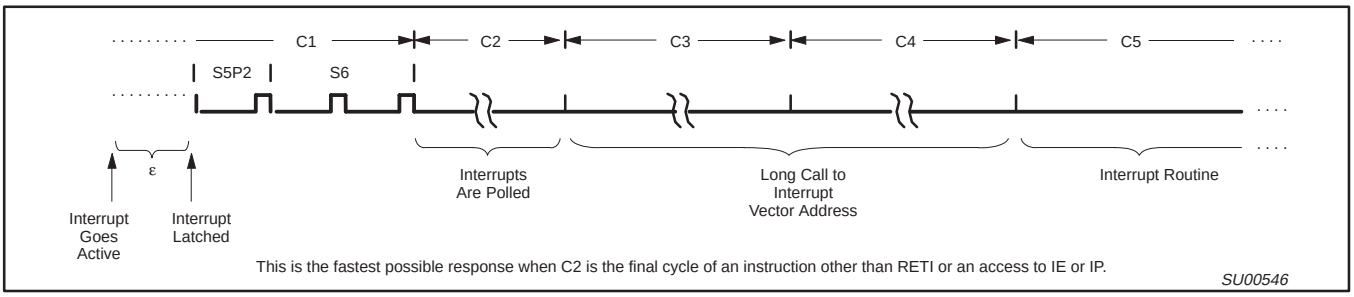


Figure 25. Interrupt Response Timing Diagram

The polling cycle/LCALL sequence is illustrated in Figure 25.

Note that if an interrupt of higher priority level goes active prior to S5P2 of the machine cycle labeled C3 in Figure 25, then in accordance with the above rules it will be vectored to during C5 and C6, without any instruction of the lower priority routine having been executed.

Thus the processor acknowledges an interrupt request by executing a hardware-generated LCALL to the appropriate servicing routine. In some cases it also clears the flag that generated the interrupt, and in other cases it doesn't. It never clears the Serial Port flag. This has to be done in the user's software. It clears an external interrupt flag (IE0 or IE1) only if it was transition-activated. The hardware-generated LCALL pushes the contents of the Program Counter on to the stack (but it does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt being vectored to, as shown in Table 8.

Execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that this interrupt routine is no longer in progress, then pops the top two bytes from the stack and reloads the Program Counter. Execution of the interrupted program continues from where it left off.

Note that a simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking an interrupt was still in progress, making future interrupts impossible.

External Interrupts

The external sources can be programmed to be level-activated or transition-activated by setting or clearing bit IT1 or IT0 in Register TCON. If ITx = 0, external interrupt x is triggered by a detected low at the $\overline{\text{INT}}$x pin. If ITx = 1, external interrupt x is edge triggered. In this mode if successive samples of the $\overline{\text{INT}}$x pin show a high in one cycle and a low in the next cycle, interrupt request flag IEx in TCON is set. Flag bit IEx then requests the interrupt.

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 12 oscillator periods to ensure sampling. If the external interrupt is transition-activated, the external source has to hold the request pin high for at least one cycle, and then hold it low for at least one cycle. This is done to ensure that the transition is seen so that interrupt request flag IEx will be set. IEx will be automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source has to hold the request active until the requested interrupt is actually generated. Then it has to deactivate the request before the interrupt service routine is completed, or else another interrupt will be generated.

Response Time

The $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ levels are inverted and latched into IE0 and IE1 at S5P2 of every machine cycle. The values are not actually polled by the circuitry until the next machine cycle. If a request is active and conditions are right for it to be acknowledged, a hardware subroutine call to the requested service routine will be the next instruction to be executed. The call itself takes two cycles. Thus, a minimum of three complete machine cycles elapse between activation of an external interrupt request and the beginning of execution of the first instruction of the service routine. Figure 25 shows interrupt response timings.

A longer response time would result if the request is blocked by one of the 3 previously listed conditions. If an interrupt of equal or higher priority level is already in progress, the additional wait time obviously depends on the nature of the other interrupt's service routine. If the instruction in progress is not in its final cycle, the additional wait time cannot be more the 3 cycles, since the longest instructions (MUL and DIV) are only 4 cycles long, and if the instruction in progress is RETI or an access to IE or IP, the additional wait time cannot be more than 5 cycles (a maximum of one more cycle to complete the instruction in progress, plus 4 cycles to complete the next instruction if the instruction is MUL or DIV).

Thus, in a single-interrupt system, the response time is always more than 3 cycles and less than 9 cycles.

As previously mentioned, the derivatives described in this data sheet have a four-level interrupt structure. The corresponding registers are IE, IP and IPH. (See Figures 22, 23, and 24.) The IPH (Interrupt Priority High) register makes the four-level interrupt structure possible.

The function of the IPH SFR is simple and when combined with the IP SFR determines the priority of each interrupt. The priority of each interrupt is determined as shown in the following table:

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPH.x	IP.x	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

Table 8. Interrupt Table

SOURCE	POLLING PRIORITY	REQUEST BITS	HARDWARE CLEAR?	VECTOR ADDRESS
External interrupt 0	1	IE0	N (L)[1] Y (T)[2]	03H
Timer 0	2	TF0	Y	0BH
External interrupt 1	3	IE1	N (L) Y (T)	13H
Timer 1	4	TF1	Y	1BH
UART	5	RI, TI	N	23H
Timer 2	6	TF2, EXF2	N	2BH

NOTES:
1. L = Level activated
2. T = Transition activated

Reduced EMI

All port pins have slew rate controlled outputs. This is to limit noise generated by quickly switching output signals. The slew rate is factory set to approximately 10 ns rise and fall times.

Reduced EMI Mode

The AO bit (AUXR.0) in the AUXR register when set disables the ALE output.

AUXR (8EH)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	AO

AUXR.0 AO Turns off ALE output.

Dual DPTR

The dual DPTR structure (see Figure 26) enables a way to specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 that allows the program code to switch between them.

- New Register Name: AUXR1#
- SFR Address: A2H
- Reset Value: xxx000x0B

AUXR1 (A2H)

7	6	5	4	3	2	1	0
–	–	–	LPEP	WUPD	0	–	DPS

Where:
DPS = AUXR1/bit0 = Switches between DPTR0 and DPTR1.

Select Reg	DPS
DPTR0	0
DPTR1	1

The DPS bit status should be saved by software when switching between DPTR0 and DPTR1.

Note that bit 2 is not writable and is always read as a zero. This allows the DPS bit to be quickly toggled simply by executing an INC DPTR instruction without affecting the WUPD or LPEP bits.

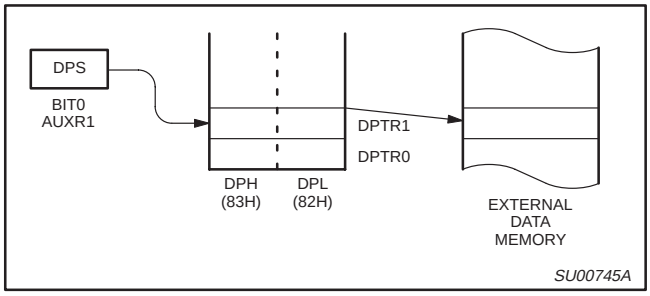


Figure 26.

DPTR Instructions

The instructions that refer to DPTR refer to the data pointer that is currently selected using the AUXR1/bit 0 register. The six instructions that use the DPTR are as follows:

INC DPTR	Increments the data pointer by 1
MOV DPTR, #data16	Loads the DPTR with a 16-bit constant
MOV A, @ A+DPTR	Move code byte relative to DPTR to ACC
MOVX A, @ DPTR	Move external RAM (16-bit address) to ACC
MOVX @ DPTR , A	Move ACC to external RAM (16-bit address)
JMP @ A + DPTR	Jump indirect relative to DPTR

The data pointer can be accessed on a byte-by-byte basis by specifying the low or high byte in an instruction which accesses the SFRs. See application note AN458 for more details.

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or –40 to +85	°C
Storage temperature range	–65 to +150	°C
Voltage on $\overline{EA}/V_{PP}$ pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS}	–0.5 to +6.5	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or –40°C to +85°C

SYMBOL	FIGURE	PARAMETER	OPERATING MODE	POWER SUPPLY VOLTAGE	CLOCK FREQUENCY RANGE		UNIT
					MIN	MAX	
$1/t_{CLCL}$	31	Oscillator frequency	6-clock	5 V ± 10%	0	30	MHz
			6-clock	2.7 V to 5.5 V	0	16	MHz
			12-clock	5 V ± 10%	0	33	MHz
			12-clock	2.7 V to 5.5 V	0	16	MHz

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0 °C to +70 °C or –40 °C to +85 °C; **V_{CC} = 2.7 V to 5.5 V**; V_{SS} = 0 V (16 MHz max. CPU clock)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
V_{IL}	Input low voltage[11]	4.0 V < V_{CC} < 5.5 V	–0.5		0.2 V_{CC}–0.1	V
		2.7 V < V_{CC} < 4.0 V	–0.5		0.7 V_{CC}	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, $\overline{EA}$)	–	0.2 V_{CC}+0.9		V_{CC}+0.5	V
V_{IH1}	Input high voltage, XTAL1, RST[11]	–	0.7 V_{CC}		V_{CC}+0.5	V
V_{OL}	Output low voltage, ports 1, 2, [8]	V_{CC} = 2.7 V; I_{OL} = 1.6 mA[2]	–		0.4	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$[8, 7]	V_{CC} = 2.7 V; I_{OL} = 3.2 mA[2]	–		0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 [3]	V_{CC} = 2.7 V; I_{OH} = –20 μA	V_{CC} – 0.7		–	V
		V_{CC} = 4.5 V; I_{OH} = –30 μA	V_{CC} – 0.7		–	V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE[9], $\overline{PSEN}$[3]	V_{CC} = 2.7 V; I_{OH} = –3.2 mA	V_{CC} – 0.7		–	V
I_{IL}	Logical 0 input current, ports 1, 2, 3	V_{IN} = 0.4 V	–1		–50	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3[6]	V_{IN} = 2.0 V; See note 4	–		–650	μA
I_{LI}	Input leakage current, port 0	0.45 < V_{IN} < V_{CC} – 0.3	–		±10	μA
I_{CC}	Power supply current (see Figure 34 and Source Code):					
	Active mode @ 16 MHz					μA
	Idle mode @ 16 MHz					μA
	Power-down mode or clock stopped (see Figure 30 for conditions) [12]	T_{amb} = 0 °C to 70 °C		2	30	μA
		T_{amb} = –40 °C to +85 °C		3	50	μA
V_{RAM}	RAM keep-alive voltage	–	1.2			V
R_{RST}	Internal reset pull-down resistor	–	40		225	kΩ
C_{IO}	Pin capacitance[10] (except $\overline{EA}$)	–	–		15	pF

NOTES:

1. Typical ratings are not guaranteed. Values listed are based on tests conducted on limited number of samples at room temperature.
2. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.
3. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the V_{CC}–0.7 specification when the address bits are stabilizing.
4. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V.
5. See Figures 36 through 39 for I_{CC} test conditions and Figure 34 for I_{CC} vs. Frequency
   12-clock mode characteristics:
   Active mode (operating): I_{CC} = 1.0 mA + 0.9 mA × FREQ.[MHz]
   Active mode (reset): I_{CC} = 7.0 mA + 0.5 mA x FREQ.[MHz]
   Idle mode: I_{CC} = 1.0 mA + 0.18 mA x FREQ.[MHz]
6. This value applies to T_{amb} = 0 °C to +70 °C. For T_{amb} = –40 °C to +85 °C, I_{TL} = –750 μA.
7. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.
8. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15 mA (*NOTE: This is 85 °C specification.)
   Maximum I_{OL} per 8-bit port: 26 mA
   Maximum total I_{OL} for all outputs: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
9. ALE is tested to V_{OH1}, except when ALE is off then V_{OH} is the voltage specification.
10. Pin capacitance is characterized but not tested. Pin capacitance is less than 25 pF. Pin capacitance of ceramic package is less than 15 pF (except $\overline{EA}$ is 25 pF).
11. To improve noise rejection a nominal 100 ns glitch rejection circuitry has been added to the RST pin, and a nominal 15 ns glitch rejection circuitry has been added to the $\overline{INT0}$ and $\overline{INT1}$ pins. Previous devices provided only an inherent 5 ns of glitch rejection.
12. Power down mode for 3 V range: Commercial Temperature Range – typ: 0.5 μA, max. 20 μA; Industrial Temperature Range – typ. 1.0 μA, max. 30 μA;

AC ELECTRICAL CHARACTERISTICS (12-CLOCK MODE, 2.7 V TO 5.5 V OPERATION)

T_{amb} = 0 °C to +70 °C or –40 °C to +85 °C ; V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0 V[1,2,3,4]

Symbol	Figure	Parameter	Limits		16 MHz Clock		Unit
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	31	Oscillator frequency	0	16	–	–	MHz
t_{LHLL}	27	ALE pulse width	$2t_{CLCL}$–10	–	115	–	ns
t_{AVLL}	27	Address valid to ALE low	t_{CLCL} –15	–	47.5	–	ns
t_{LLAX}	27	Address hold after ALE low	t_{CLCL} –25	–	37.5	–	ns
t_{LLIV}	27	ALE low to valid instruction in	–	4 t_{CLCL} –55	–	195	ns
t_{LLPL}	27	ALE low to $\overline{PSEN}$ low	t_{CLCL} –15	–	47.5	–	ns
t_{PLPH}	27	$\overline{PSEN}$ pulse width	3 t_{CLCL} –15	–	172.5	–	ns
t_{PLIV}	27	$\overline{PSEN}$ low to valid instruction in	–	3 t_{CLCL} –55	–	132.5	ns
t_{PXIX}	27	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}	27	Input instruction float after $\overline{PSEN}$	–	t_{CLCL} –10	–	52.5	ns
t_{AVIV}	27	Address to valid instruction in	–	5 t_{CLCL} –50	–	262.5	ns
t_{PLAZ}	27	$\overline{PSEN}$ low to address float	–	10	–	10	ns
Data Memory							
t_{RLRH}	28	$\overline{RD}$ pulse width	6 t_{CLCL} –25	–	350	–	ns
t_{WLWH}	29	$\overline{WR}$ pulse width	6 t_{CLCL} –25	–	350	–	ns
t_{RLDV}	28	$\overline{RD}$ low to valid data in	–	5 t_{CLCL} –50	–	262.5	ns
t_{RHDX}	28	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	28	Data float after $\overline{RD}$	–	2 t_{CLCL} –20	–	105	ns
t_{LLDV}	28	ALE low to valid data in	–	8 t_{CLCL} –55	–	445	ns
t_{AVDV}	28	Address to valid data in	–	9 t_{CLCL} –50	–	512.5	ns
t_{LLWL}	28, 29	ALE low to $\overline{RD}$ or $\overline{WR}$ low	3 t_{CLCL} –20	3 t_{CLCL} +20	167.5	207.5	ns
t_{AVWL}	28, 29	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	4 t_{CLCL} –20	–	230	–	ns
t_{QVWX}	29	Data valid to $\overline{WR}$ transition	t_{CLCL} –30	–	32.5	–	ns
t_{WHQX}	29	Data hold after $\overline{WR}$	t_{CLCL} –20	–	42.5	–	ns
t_{QVWH}	29	Data valid to $\overline{WR}$ high	7 t_{CLCL} –10	–	427.5	–	ns
t_{RLAZ}	28	$\overline{RD}$ low to address float	–	0	–	0	ns
t_{WHLH}	28, 29	$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{CLCL} –15	t_{CLCL} +15	47.5	77.5	ns
External Clock							
t_{CHCX}	31	High time	0.32 t_{CLCL}	$t_{CLCL} - t_{CLCX}$	–	–	ns
t_{CLCX}	31	Low time	0.32 t_{CLCL}	$t_{CLCL} - t_{CHCX}$	–	–	ns
t_{CLCH}	31	Rise time	–	5	–	–	ns
t_{CHCL}	31	Fall time	–	5	–	–	ns
Shift register							
t_{XLXL}	30	Serial port clock cycle time	12 t_{CLCL}	–	750	–	ns
t_{QVXH}	30	Output data setup to clock rising edge	10 t_{CLCL} –25	–	600	–	ns
t_{XHQX}	30	Output data hold after clock rising edge	2 t_{CLCL} –15	–	110	–	ns
t_{XHDX}	30	Input data hold after clock rising edge	0	–	0	–	ns
t_{XHDV}	30	Clock rising edge to input data valid	–	10 t_{CLCL} –133	–	492	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all outputs = 80 pF
3. Interfacing the microcontroller to devices with float time up to 45 ns is permitted. This limited bus contention will not cause damage to port 0 drivers.
4. Parts are guaranteed by design to operate down to 0 Hz.

AC ELECTRICAL CHARACTERISTICS (6-CLOCK MODE, 2.7 V TO 5.5 V OPERATION)

T_{amb} = 0 °C to +70 °C or –40 °C to +85 °C ; V_{CC}=2.7 V to 5.5 V, V_{SS} = 0 V[1,2,3,4,5]

Symbol	Figure	Parameter	Limits		16 MHz Clock		Unit
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	31	Oscillator frequency	0	16	–	–	MHz
t_{LHLL}	27	ALE pulse width	t_{CLCL}–10	–	52.5	–	ns
t_{AVLL}	27	Address valid to ALE low	0.5 t_{CLCL} –15	–	16.25	–	ns
t_{LLAX}	27	Address hold after ALE low	0.5 t_{CLCL} –25	–	6.25	–	ns
t_{LLIV}	27	ALE low to valid instruction in	–	2 t_{CLCL} –55	–	70	ns
t_{LLPL}	27	ALE low to $\overline{PSEN}$ low	0.5 t_{CLCL} –15	–	16.25	–	ns
t_{PLPH}	27	$\overline{PSEN}$ pulse width	1.5 t_{CLCL} –15	–	78.75	–	ns
t_{PLIV}	27	$\overline{PSEN}$ low to valid instruction in	–	1.5 t_{CLCL} –55	–	38.75	ns
t_{PXIX}	27	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}	27	Input instruction float after $\overline{PSEN}$	–	0.5 t_{CLCL} –10	–	21.25	ns
t_{AVIV}	27	Address to valid instruction in	–	2.5 t_{CLCL} –50	–	101.25	ns
t_{PLAZ}	27	$\overline{PSEN}$ low to address float	–	10	–	10	ns
Data Memory							
t_{RLRH}	28	$\overline{RD}$ pulse width	3 t_{CLCL} –25	–	162.5	–	ns
t_{WLWH}	29	$\overline{WR}$ pulse width	3 t_{CLCL} –25	–	162.5	–	ns
t_{RLDV}	28	$\overline{RD}$ low to valid data in	–	2.5 t_{CLCL} –50	–	106.25	ns
t_{RHDX}	28	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	28	Data float after $\overline{RD}$	–	t_{CLCL} –20	–	42.5	ns
t_{LLDV}	28	ALE low to valid data in	–	4 t_{CLCL} –55	–	195	ns
t_{AVDV}	28	Address to valid data in	–	4.5 t_{CLCL} –50	–	231.25	ns
t_{LLWL}	28, 29	ALE low to $\overline{RD}$ or $\overline{WR}$ low	1.5 t_{CLCL} –20	1.5 t_{CLCL} +20	73.75	113.75	ns
t_{AVWL}	28, 29	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	2 t_{CLCL} –20	–	105	–	ns
t_{QVWX}	29	Data valid to $\overline{WR}$ transition	0.5 t_{CLCL} –30	–	1.25	–	ns
t_{WHQX}	29	Data hold after $\overline{WR}$	0.5 t_{CLCL} –20	–	11.25	–	ns
t_{QVWH}	29	Data valid to $\overline{WR}$ high	3.5 t_{CLCL} –10	–	208.75	–	ns
t_{RLAZ}	28	$\overline{RD}$ low to address float	–	0	–	0	ns
t_{WHLH}	28, 29	$\overline{RD}$ or $\overline{WR}$ high to ALE high	0.5 t_{CLCL} –15	0.5 t_{CLCL} +15	16.25	46.25	ns
External Clock							
t_{CHCX}	31	High time	0.4 t_{CLCL}	$t_{CLCL} - t_{CLCX}$	–	–	ns
t_{CLCX}	31	Low time	0.4 t_{CLCL}	$t_{CLCL} - t_{CHCX}$	–	–	ns
t_{CLCH}	31	Rise time	–	5	–	–	ns
t_{CHCL}	31	Fall time	–	5	–	–	ns
Shift register							
t_{XLXL}	30	Serial port clock cycle time	6 t_{CLCL}	–	375	–	ns
t_{QVXH}	30	Output data setup to clock rising edge	5 t_{CLCL} –25	–	287.5	–	ns
t_{XHQX}	30	Output data hold after clock rising edge	t_{CLCL} –15	–	47.5	–	ns
t_{XHDX}	30	Input data hold after clock rising edge	0	–	0	–	ns
t_{XHDV}	30	Clock rising edge to input data valid	–	5 t_{CLCL} –133	–	179.5	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$=100 pF, load capacitance for all outputs = 80 pF
3. Interfacing the microcontroller to devices with float time up to 45ns is permitted. This limited bus contention will not cause damage to port 0 drivers.
4. Parts are guaranteed by design to operate down to 0 Hz.
5. Data shown in the table are the best mathematical models for the set of measured values obtained in tests. If a particular parameter calculated at a customer specified frequency has a negative value, it should be considered equal to zero.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE
P – $\overline{\text{PSEN}}$
Q – Output data
R – $\overline{\text{RD}}$ signal
t – Time
V – Valid
W – $\overline{\text{WR}}$ signal
X – No longer a valid logic level
Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
t_{LLPL} =Time for ALE low to $\overline{\text{PSEN}}$ low.

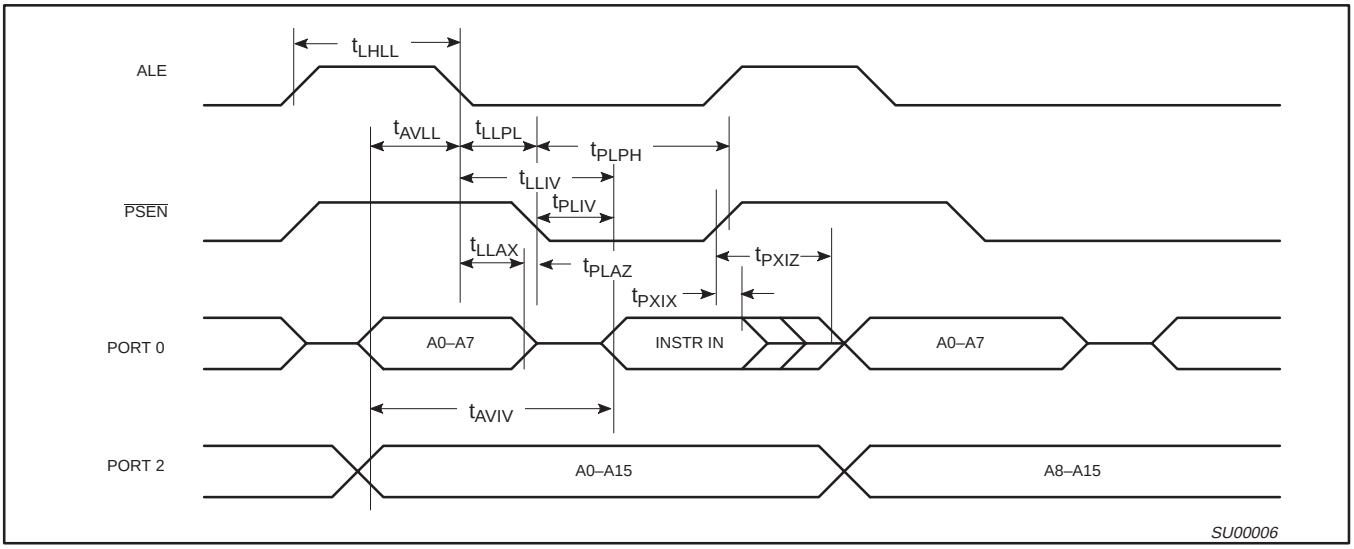


Figure 27. External Program Memory Read Cycle

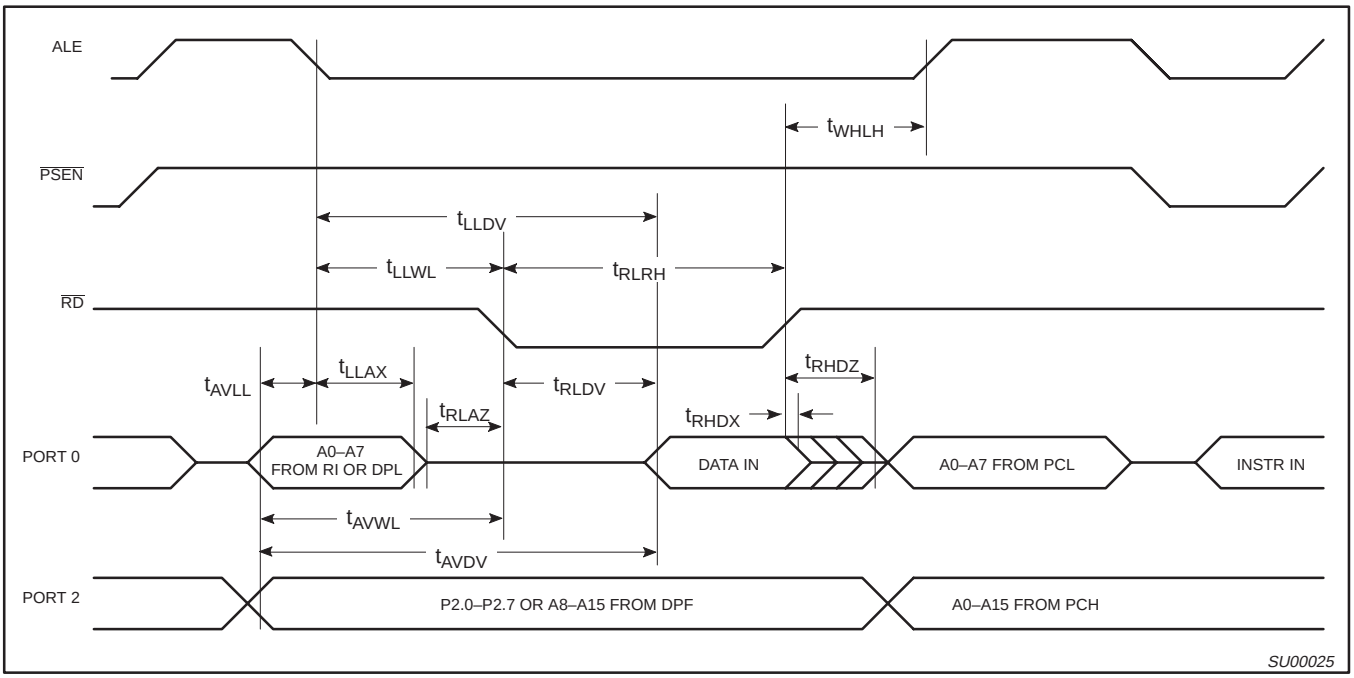


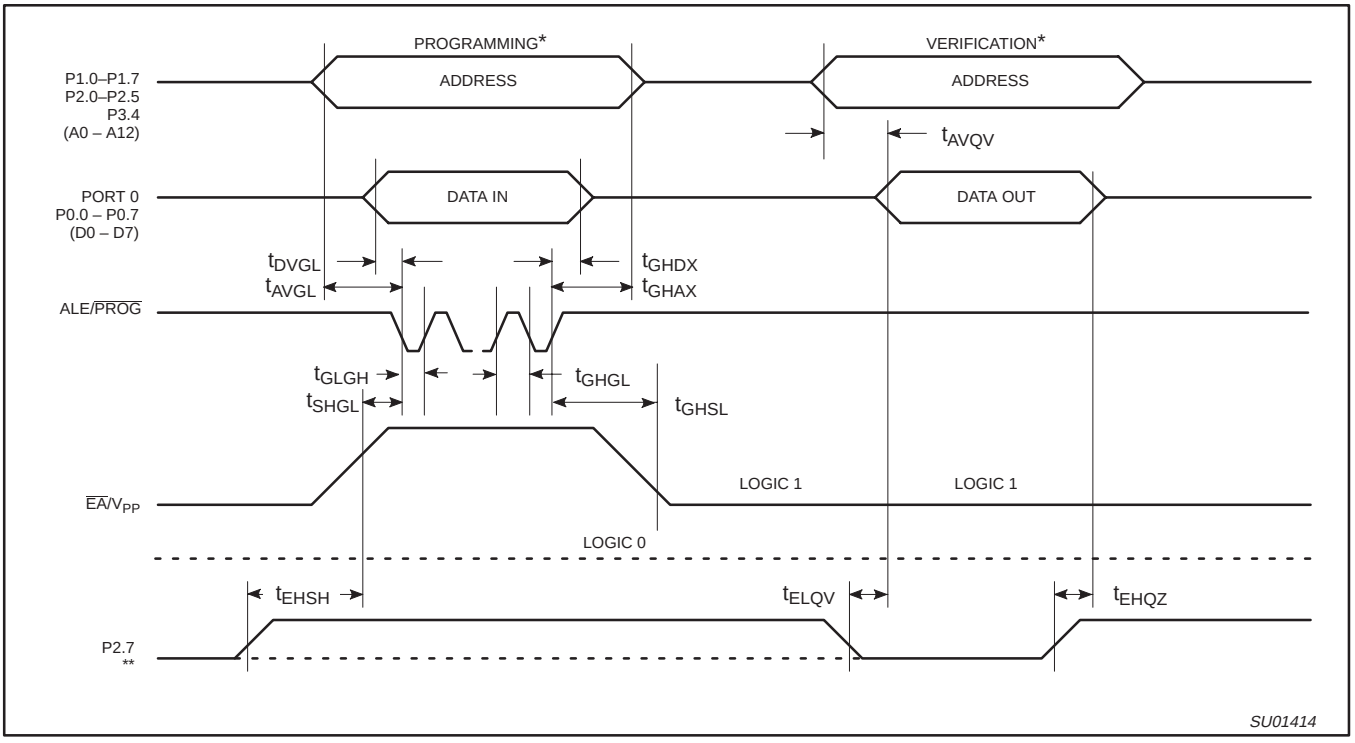
Figure 28. External Data Memory Read Cycle

PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_{amb} = 21 °C to +27 °C, V_{CC} = 5 V±10%, V_{SS} = 0 V (See Figure 43)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50 [1]	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHAX}	Address hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHDX}	Data hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to $\overline{PROG}$ low	10		µs
t_{GHSL}	V_{PP} hold after $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ width	90	110	µs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELQZ}	$\overline{ENABLE}$ low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHGL}	$\overline{PROG}$ high to $\overline{PROG}$ low	10		µs

NOTE:
1. Not tested.



NOTES:

* FOR PROGRAMMING CONFIGURATION SEE FIGURE 40.
FOR VERIFICATION CONDITIONS SEE FIGURE 42.

** SEE TABLE 9.

Figure 43. Programming and Verification

80C54X2 ROM CODE SUBMISSION

When submitting a ROM code for the 80C54X2, the following must be specified:

1. 16 kbyte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 3FFFH	DATA	7:0	User ROM Data
4000H to 403FH	KEY	7:0	ROM Encryption Key FFH = no encryption
4040H	SEC	0	ROM Security Bit 1 0 = enable security 1 = disable security
4040H	SEC	1	ROM Security Bit 2 0 = enable security 1 = disable security

Security Bit 1: When programmed, this bit has two effects on masked ROM parts:

1. External MOVC is disabled, and
2. $\overline{EA}$ is latched on Reset.

Security Bit 2: When programmed, this bit inhibits Verify User ROM.

NOTE: Security Bit 2 cannot be enabled unless Security Bit 1 is enabled.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box, and send to Philips along with the code:

Security Bit #1: ☐ Enabled ☐ Disabled

Security Bit #2: ☐ Enabled ☐ Disabled

Encryption: ☐ No ☐ Yes If Yes, must send key file.

REVISION HISTORY

Rev	Date	Description
_6	20030124	**Product data (9397 750 10995); ECN 853-2337 29260 of 06 December 2002** Modifications: • Added TSSOP38 package details
_5	20020912	**Product data (9397 750 10361); ECN 853-2337 28906 of 12 September 2002**
_4	20020612	**Product data (9397 750 09969); ECN 853-2337 28427 of 12 June 2002**
_3	20020422	**Product data (9397 750 09779); ECN 853-2337 28059 of 22 April 2002**
_2	20020219	**Preliminary data (9397 750 09467)**
_1	20010924	**Preliminary data (9397 750 08895); initial release**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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