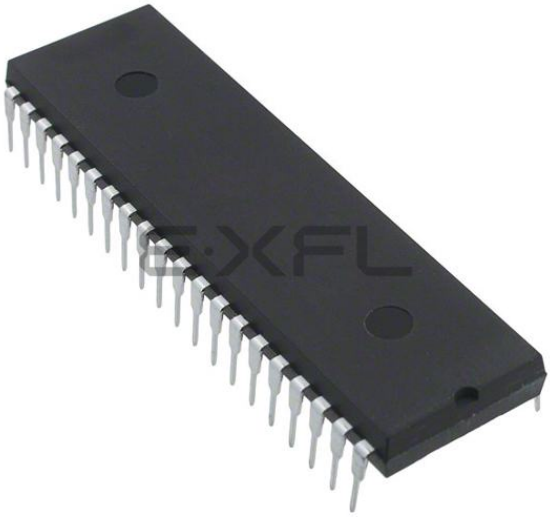

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87c58x2bn-112

DESCRIPTION

The Philips microcontrollers described in this data sheet are high-performance static 80C51 designs incorporating Philips' high-density CMOS technology with operation from 2.7 V to 5.5 V. They support both 6-clock and 12-clock operation.

The P8xC31X2/51X2 and P8xC32X2/52X2/54X2/58X2 contain 128 byte RAM and 256 byte RAM respectively, 32 I/O lines, three 16-bit counter/timers, a six-source, four-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the devices are low power static designs which offer a wide range of operating frequencies down to zero. Two software selectable modes of power reduction — idle mode and power-down mode — are available. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative. Since the design is static, the clock can be stopped without loss of user data. Then the execution can be resumed from the point the clock was stopped.

SELECTION TABLE

For applications requiring more ROM and RAM, as well as more on-chip peripherals, see the P89C66x and P89C51Rx2 data sheets.

Type	Memory				Timers				Serial Interfaces				ADC bits/ch.	I/O Pins	Interrupts (External)	Program Security	Default Clock Rate	Optional Clock Rate	Max. Freq. at 6-clk / 12-clk (MHz)	Freq. Range at 3V (MHz)	Freq. Range at 5V (MHz)
	RAM	ROM	OTP	Flash	# of Timers	PWM	PCA	WD	UART	I^2C	CAN	SPI									
P87C58X2	256B	–	32K	–	3	–	–	–	✓	–	–	–	–	32	6 (2)	✓	12–clk	6-clk	30/33	0–16	0–30/33
P80C58X2	256B	32K	–	–	3	–	–	–	✓	–	–	–	–	32	6 (2)	✓	12–clk	6-clk	30/33	0–16	0–30/33
P87C54X2	256B	–	16K	–	3	–	–	–	✓	–	–	–	–	32	6 (2)	✓	12–clk	6-clk	30/33	0–16	0–30/33
P80C54X2	256B	16K	–	–	3	–	–	–	✓	–	–	–	–	32	6 (2)	✓	12–clk	6-clk	30/33	0–16	0–30/33
P87C52X2	256B	–	8K	–	3	–	–	–	✓	–	–	–	–	32	6 (2)	✓	12–clk	6-clk	30/33	0–16	0–30/33
P80C52X2	256B	8K	–	–	3	–	–	–	✓	–	–	–	–	32	6 (2)	✓	12–clk	6-clk	30/33	0–16	0–30/33
P87C51X2	128B	–	4K	–	3	–	–	–	✓	–	–	–	–	32	6 (2)	✓	12–clk	6-clk	30/33	0–16	0–30/33
P80C51X2	128B	4K	–	–	3	–	–	–	✓	–	–	–	–	32	6 (2)	✓	12–clk	6-clk	30/33	0–16	0–30/33
P80C32X2	256B	–	–	–	3	–	–	–	✓	–	–	–	–	32	6 (2)	–	12–clk	6-clk	30/33	0–16	0–30/33
P80C31X2	128B	–	–	–	3	–	–	–	✓	–	–	–	–	32	6 (2)	–	12–clk	6-clk	30/33	0–16	0–30/33

NOTE:

1. I^2C = Inter-Integrated Circuit Bus; CAN = Controller Area Network; SPI = Serial Peripheral Interface; PCA = Programmable Counter Array; ADC = Analog-to-Digital Converter; PWM = Pulse Width Modulation

P80C31/32X2 ORDERING INFORMATION (ROMLESS)

Type number	Package			Temperature Range (°C)
	Name	Description	Version	
P80C31X2BA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2	0 to +70
P80C31X2BN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	0 to +70
P80C32X2BA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2	0 to +70
P80C32X2BN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	0 to +70
P80C32X2BBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	0 to +70
P80C32X2FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2	–40 to +85
P80C32X2FN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	–40 to +85

P87C51X2 ORDERING INFORMATION (4 KBYTE OTP)

Type number	Package			Temperature Range (°C)
	Name	Description	Version	
P87C51X2BA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2	0 to +70
P87C51X2BN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	0 to +70
P87C51X2BBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	0 to +70
P87C51X2FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2	–40 to +85
P87C51X2FBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	–40 to +85

P87C52X2 ORDERING INFORMATION (8 KBYTE OTP)

Type number	Package			Temperature Range (°C)
	Name	Description	Version	
P87C52X2BA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2	0 to +70
P87C52X2BN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	0 to +70
P87C52X2BBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	0 to +70
P87C52X2FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2	–40 to +85
P87C52X2FN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	–40 to +85
P87C52X2FBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	–40 to +85

P87C54X2 ORDERING INFORMATION (16 KBYTE OTP)

Type number	Package			Temperature Range (°C)
	Name	Description	Version	
P87C54X2BA	PLCC44	plastic lead chip carrier; 44 leads	SOT187-2	0 to +70
P87C54X2BN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	0 to +70
P87C54X2BBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	0 to +70
P87C54X2BDH	TSSOP38	plastic thin shrink small outline package; 38 leads; body width 4.4 mm; lead pitch 0.5 mm	SOT510-1	0 to +70
P87C54X2FA	PLCC44	plastic lead chip carrier; 44 leads	SOT187-2	–40 to +85
P87C54X2FBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	–40 to +85

P87C58X2 ORDERING INFORMATION (32 KBYTE OTP)

Type number	Package			Temperature Range (°C)
	Name	Description	Version	
P87C58X2BA	PLCC44	plastic lead chip carrier; 44 leads	SOT187-2	0 to +70
P87C58X2BN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	0 to +70
P87C58X2BBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	0 to +70
P87C58X2FA	PLCC44	plastic lead chip carrier; 44 leads	SOT187-2	–40 to +85
P87C58X2FBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	–40 to +85
P87C58X2FN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	–40 to +85

All OTP parts listed here are also available as ROM parts (80C5xX2). Please contact your Philips representative if you would like to order a ROM part.

PART NUMBER DERIVATION

Memory	Temperature Range	Package
P87C51X2 7 = OTP 0 = ROM or ROMless 5 = ROM/OTP 3 = ROMless 1 = 128 BYTES RAM 4 KBYTES ROM/OTP 2 = 256 BYTES RAM 8 KBYTES ROM/OTP 4 = 256 BYTES RAM 16 KBYTES ROM/OTP 8 = 256 BYTES RAM 32 KBYTES ROM/OTP X2 = 6-clock mode available	B = 0 °C TO +70 °C F = –40 °C TO +85 °C	A = PLCC N = DIP BD = LQFP DH = TSSOP

The following table illustrates the correlation between operating mode, power supply and maximum external clock frequency:

Operating Mode	Power Supply	Maximum Clock Frequency
6-clock	5 V ± 10%	30 MHz
6-clock	2.7 V to 5.5 V	16 MHz
12-clock	5 V ± 10%	33 MHz
12-clock	2.7 V to 5.5 V	16 MHz

PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER DIP	PLCC	LQFP	TSSOP	TYPE	NAME AND FUNCTION
V_{SS}	20	22	16	9	I	**Ground:** 0 V reference.
V_{CC}	40	44	38	29	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0-0.7	39–32	43–36	37–30	28–21	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification and received code bytes during EPROM programming. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	40–44, 1–3	30–37	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 also receives the low-order address byte during program memory verification. Alternate functions for Port 1 include:
	1	2	40	30	I/O	**T2 (P1.0):** Timer/Counter 2 external count input/clockout (see Programmable Clock-Out)
	2	3	41	31	I	**T2EX (P1.1):** Timer/Counter 2 Reload/Capture/Direction control
P2.0–P2.7	21–28	24–31	18–25	10–17	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. Some Port 2 pins receive the high order address bits during EPROM programming and verification.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	1–6	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	10	11	5	1	I	**RxD (P3.0):** Serial input port
	11	13	7	2	O	**TxD (P3.1):** Serial output port
	12	14	8		I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt[1]
	13	15	9	3	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt
	14	16	10	4	I	**T0 (P3.4):** Timer 0 external input
	15	17	11		I	**T1 (P3.5):** Timer 1 external input[1]
	16	18	12	5	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe
	17	19	13	6	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe
RST	9	10	4	38	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE/$\overline{\text{PROG}}$	30	33	27	19	O	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (12-clock Mode) or 1/3 (6-clock Mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during EPROM programming. ALE can be disabled by setting SFR auxiliary.0. With this bit set, ALE will be active only during a MOVX instruction.

Table 1. Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB							LSB	RESET VALUE
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
AUXR#	Auxiliary	8EH	–	–	–	–	–	–	–	AO	xxxxxxx0B
AUXR1#	Auxiliary 1	A2H	–	–	–	LPEP[2]	WUPD	0	–	DPS	xxx000x0B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
CKCON	Clock Control Register	8FH	–	–	–	–	–	–	–	X2	xxx00000B
DPTR:	Data Pointer (2 bytes)										
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*	Interrupt Enable	A8H	$\overline{EA}$	–	ET2	ES	ET1	EX1	ET0	EX0	0x000000B
			BF	BE	BD	BC	BB	BA	B9	B8	
IP*	Interrupt Priority	B8H	–	–	PT2	PS	PT1	PX1	PT0	PX0	xx000000B
IPH#	Interrupt Priority High	B7H	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	xx000000B
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	–	–	–	–	–	–	T2EX	T2	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TxD	RxD	FFH
PCON#[1]	Power Control	87H	SMOD1	SMOD0	–	POF	GF1	GF0	PD	IDL	00xx0000B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	000000x0B
RACAP2H#	Timer 2 Capture High	CBH									00H
RACAP2L#	Timer 2 Capture Low	CAH									00H
SADDR#	Slave Address	A9H									00H
SADEN#	Slave Address Mask	B9H									00H
SBUF	Serial Data Buffer	99H									xxxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SP	Stack Pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON*	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T}$2	CP/$\overline{RL}$2	00H
T2MOD#	Timer 2 Mode Control	C9H	–	–	–	–	–	–	T2OE	DCEN	xxxxxx00B
TH0	Timer High 0	8CH									00H
TH1	Timer High 1	8DH									00H
TH2#	Timer High 2	CDH									00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low 1	8BH									00H
TL2#	Timer Low 2	CCH									00H
TMOD	Timer Mode	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	00H

NOTE:
Unused register bits that are not defined should not be set by the user's program. If violated, the device could function incorrectly.
* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.
– Reserved bits.
1. Reset value depends on reset source.
2. LPEP – Low Power EPROM operation (OTP only)

TMOD Address = 89H Reset Value = 00H

Not Bit Addressable

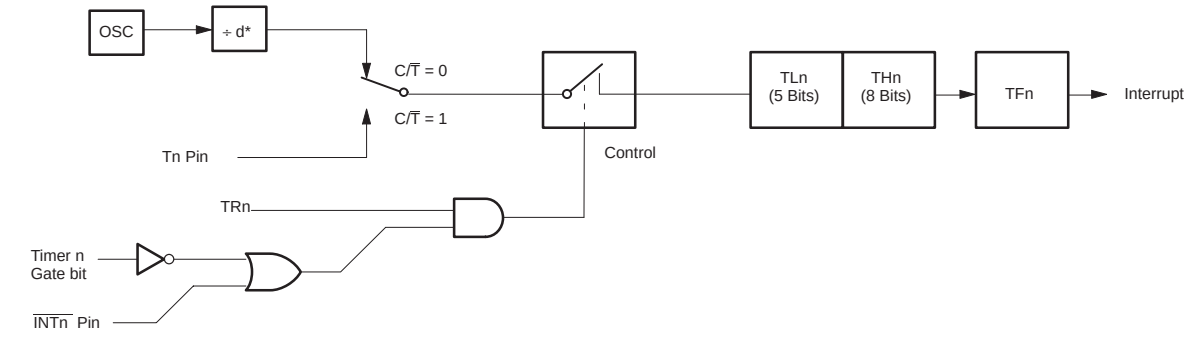
7	6	5	4	3	2	1	0
GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
TIMER 1				**TIMER 0**			

BIT	SYMBOL	FUNCTION
TMOD.3/ TMOD.7	GATE	Gating control when set. Timer/Counter "n" is enabled only while "$\overline{INTn}$" pin is high and "TRn" control pin is set. when cleared Timer "n" is enabled whenever "TRn" control bit is set.
TMOD.2/ TMOD.6	C/$\overline{T}$	Timer or Counter Selector cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from "Tn" input pin).

M1	M0	OPERATING
0	0	8048 Timer: "TLn" serves as 5-bit prescaler.
0	1	16-bit Timer/Counter: "THn" and "TLn" are cascaded; there is no prescaler.
1	0	8-bit auto-reload Timer/Counter: "THn" holds a value which is to be reloaded into "TLn" each time it overflows.
1	1	(Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	(Timer 1) Timer/Counter 1 stopped.

SU01580

Figure 1. Timer/Counter 0/1 Mode Control (TMOD) Register



*d = 6 in 6-clock mode; d = 12 in 12-clock mode.

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Figure 2. Timer/Counter 0/1 Mode 0: 13-Bit Timer/Counter

Table 4. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL}$2	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud rate generator
X	X	0	(off)

T2CON Address = C8H Reset Value = 00H
Bit Addressable

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T}$2	CP/$\overline{RL}$2

Symbol	Position	Name and Significance
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/$\overline{T}$2	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/12 in 12-clock mode or OSC/6 in 6-clock mode) 1 = External event counter (falling edge triggered).
CP/$\overline{RL}$2	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

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Figure 6. Timer/Counter 2 (T2CON) Control Register

Table 5. Timer 2 Generated Commonly Used Baud Rates

Baud Rate		Osc Freq	Timer 2	
12-clk mode	6-clk mode		RCAP2H	RCAP2L
375 K	750 K	12 MHz	FF	FF
9.6 K	19.2 K	12 MHz	FF	D9
4.8 K	9.6 K	12 MHz	FF	B2
2.4 K	4.8 K	12 MHz	FF	64
1.2 K	2.4 K	12 MHz	FE	C8
300	600	12 MHz	FB	1E
110	220	12 MHz	F2	AF
300	600	6 MHz	FD	8F
110	220	6 MHz	F9	57

Summary Of Baud Rate Equations

Timer 2 is in baud rate generating mode. If Timer 2 is being clocked through pin T2(P1.0) the baud rate is:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

If Timer 2 is being clocked internally, the baud rate is:

$$\text{Baud Rate} = \frac{f_{OSC}}{[n \times [65536 - (RCAP2H, RCAP2L)]]}$$

Where:

n = 16 in 6-clock mode, 32 in 12-clock mode.

f_{OSC}= Oscillator Frequency

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

$$RCAP2H, RCAP2L = 65536 - \left(\frac{f_{OSC}}{n \times \text{Baud Rate}}\right)$$

Timer/Counter 2 Set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the timer on. See Table 6 for set-up of Timer 2 as a timer. Also see Table 7 for set-up of Timer 2 as a counter.

Table 6. Timer 2 as a Timer

MODE	T2CON	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit Auto-Reload	00H	08H
16-bit Capture	01H	09H
Baud rate generator receive and transmit same baud rate	34H	36H
Receive only	24H	26H
Transmit only	14H	16H

Table 7. Timer 2 as a Counter

MODE	TMOD	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit	02H	0AH
Auto-Reload	03H	0BH

NOTES:
1. Capture/reload occurs only on timer/counter overflow.
2. Capture/reload occurs on timer/counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generator mode.

FULL-DUPLEX ENHANCED UART

Standard UART operation

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost.) The serial port receive and transmit registers are both accessed at Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

Mode 0: Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 the oscillator frequency in 12-clock mode or 1/6 the oscillator frequency in 6-clock mode.

Mode 1: 10 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register SCON. The baud rate is variable.

Mode 2: 11 bits are transmitted (through TxD) or received (through RxD): start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On Transmit, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency in 12-clock mode or 1/16 or 1/32 the oscillator frequency in 6-clock mode.

Mode 3: 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

Multiprocessor Communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. A way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that weren't being addressed leave their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

Serial Port Control Register

The serial port control and status register is the Special Function Register SCON, shown in Figure 12. This register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Baud Rates

The baud rate in Mode 0 is fixed: Mode 0 Baud Rate = Oscillator Frequency / 12 (12-clock mode) or / 6 (6-clock mode). The baud rate in Mode 2 depends on the value of bit SMOD in Special Function Register PCON. If SMOD = 0 (which is the value on reset), and the port pins in 12-clock mode, the baud rate is 1/64 the oscillator frequency. If SMOD = 1, the baud rate is 1/32 the oscillator frequency. In 6-clock mode, the baud rate is 1/32 or 1/16 the oscillator frequency, respectively.

Mode 2 Baud Rate =

$$\frac{2^{SMOD}}{n} \times (\text{Oscillator Frequency})$$

Where:

n = 64 in 12-clock mode, 32 in 6-clock mode

The baud rates in Modes 1 and 3 are determined by the Timer 1 or Timer 2 overflow rate.

Using Timer 1 to Generate Baud Rates

When Timer 1 is used as the baud rate generator (T2CON.RCLK = 0, T2CON.TCLK = 0), the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

Mode 1, 3 Baud Rate =

$$\frac{2^{SMOD}}{n} \times (\text{Timer 1 Overflow Rate})$$

Where:

n = 32 in 12-clock mode, 16 in 6-clock mode

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either "timer" or "counter" operation, and in any of its 3 running modes. In the most typical applications, it is configured for "timer" operation, in the auto-reload mode (high nibble of TMOD = 0010B). In that case the baud rate is given by the formula:

Mode 1, 3 Baud Rate =

$$\frac{2^{SMOD}}{n} \times \frac{\text{Oscillator Frequency}}{12 \times [256-(TH1)]}$$

Where:

n = 32 in 12-clock mode, 16 in 6-clock mode

One can achieve very low baud rates with Timer 1 by leaving the Timer 1 interrupt enabled, and configuring the Timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload. Figure 13 lists various commonly used baud rates and how they can be obtained from Timer 1.

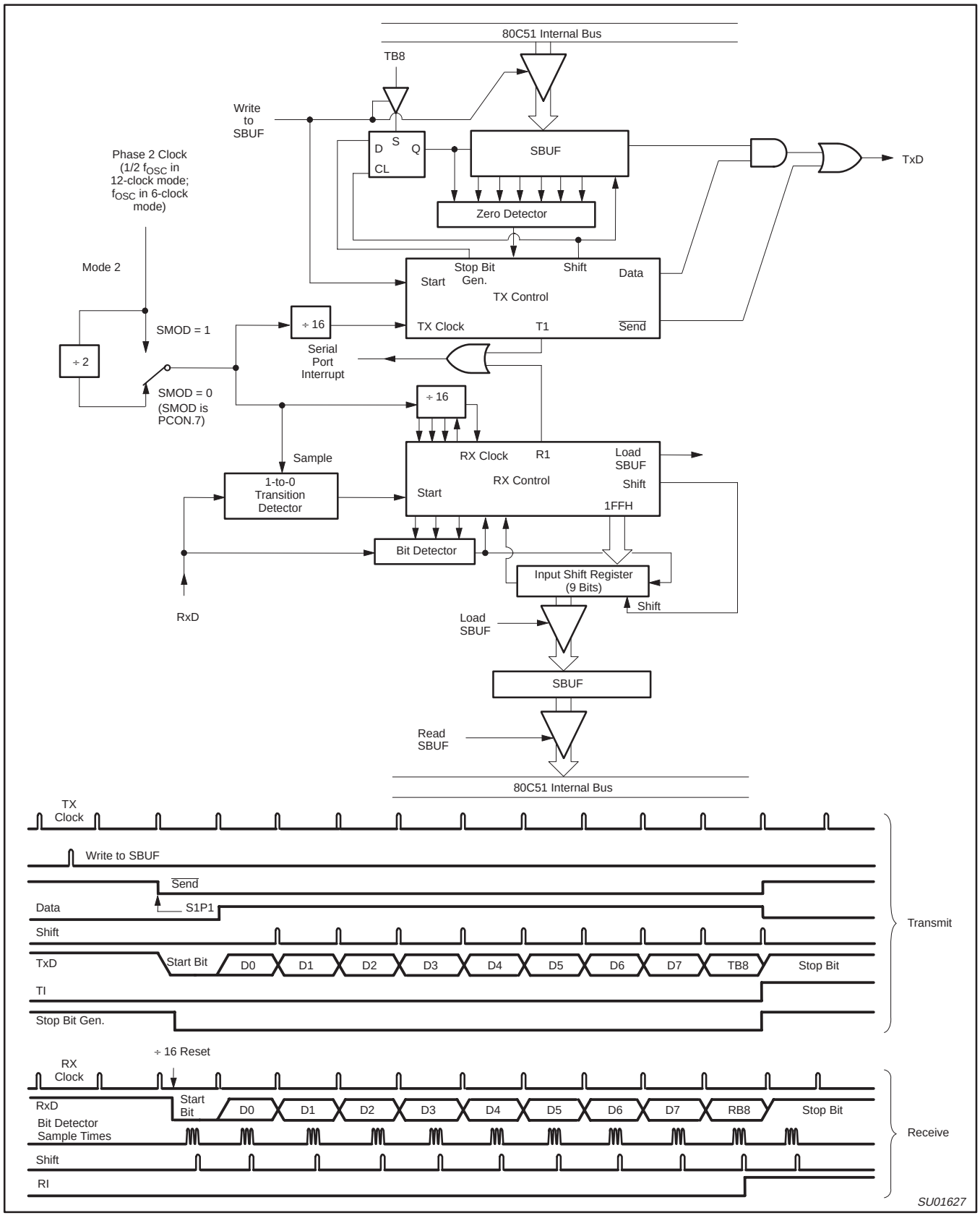


Figure 16. Serial Port Mode 2

SCON Address = 98H

Bit Addressable

Reset Value = 0000 0000B

7	6	5	4	3	2	1	0
SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

(SMOD0 = 0/1)*

Symbol	Position	Function
FE	SCON.7	Framing Error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit.*
SM0	SCON.7	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)
SM1	SCON.6	Serial Port Mode Bit 1

SM0	SM1	Mode	Description	Baud Rate**
0	0	0	shift register	f_{OSC}/12 (12-clk mode) or f_{OSC}/6 (6-clk mode)
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	f_{OSC}/64 or f_{OSC}/32 or f_{OSC}/16 (6-clock mode) or f_{OSC}/32 (12-clock mode)
1	1	3	9-bit UART	variable

SM2	SCON.5	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
REN	SCON.4	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	SCON.3	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
RB8	SCON.2	In modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	SCON.1	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	SCON.0	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

NOTES:
*SMOD0 is located at PCON.6.
**f_{OSC} = oscillator frequency

SU01628

Figure 18. SCON: Serial Port Control Register

IE Address = 0A8H Reset Value = 0X000000B

Bit Addressable

7	6	5	4	3	2	1	0
EA	—	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables it.

BIT	SYMBOL	FUNCTION
IE.7	EA	Global disable bit. If EA = 0, all interrupts are disabled. If EA = 1, each interrupt can be individually enabled or disabled by setting or clearing its enable bit.
IE.6	—	Not implemented. Reserved for future use.
IE.5	ET2	Timer 2 interrupt enable bit.
IE.4	ES	Serial Port interrupt enable bit.
IE.3	ET1	Timer 1 interrupt enable bit.
IE.2	EX1	External interrupt 1 enable bit.
IE.1	ET0	Timer 0 interrupt enable bit.
IE.0	EX0	External interrupt 0 enable bit.

SU01522

Figure 22. Interrupt Enable (IE) Register

IP Address = 0B8H Reset Value = xx000000B

Bit Addressable

7	6	5	4	3	2	1	0
—	—	PT2	PS	PT1	PX1	PT0	PX0

Priority Bit = 1 assigns higher priority
Priority Bit = 0 assigns lower priority

BIT	SYMBOL	FUNCTION
IP.7	—	Not implemented, reserved for future use.
IP.6	—	Not implemented, reserved for future use.
IP.5	PT2	Timer 2 interrupt priority bit.
IP.4	PS	Serial Port interrupt priority bit.
IP.3	PT1	Timer 1 interrupt priority bit.
IP.2	PX1	External interrupt 1 priority bit.
IP.1	PT0	Timer 0 interrupt priority bit.
IP.0	PX0	External interrupt 0 priority bit.

SU01523

Figure 23. Interrupt Priority (IP) Register

IPH Address = B7H Reset Value = xx000000B

Bit Addressable

7	6	5	4	3	2	1	0
—	—	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Priority Bit = 1 assigns higher priority
Priority Bit = 0 assigns lower priority

BIT	SYMBOL	FUNCTION
IPH.7	—	Not implemented, reserved for future use.
IPH.6	—	Not implemented, reserved for future use.
IPH.5	PT2H	Timer 2 interrupt priority bit high.
IPH.4	PSH	Serial Port interrupt priority bit high.
IPH.3	PT1H	Timer 1 interrupt priority bit high.
IPH.2	PX1H	External interrupt 1 priority bit high.
IPH.1	PT0H	Timer 0 interrupt priority bit high.
IPH.0	PX0H	External interrupt 0 priority bit high.

SU01524

Figure 24. Interrupt Priority HIGH (IPH) Register

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0 °C to +70 °C or –40 °C to +85 °C; **V_{CC} = 2.7 V to 5.5 V**; V_{SS} = 0 V (16 MHz max. CPU clock)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
V_{IL}	Input low voltage[11]	4.0 V < V_{CC} < 5.5 V	–0.5		0.2 V_{CC}–0.1	V
		2.7 V < V_{CC} < 4.0 V	–0.5		0.7 V_{CC}	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, $\overline{EA}$)	–	0.2 V_{CC}+0.9		V_{CC}+0.5	V
V_{IH1}	Input high voltage, XTAL1, RST[11]	–	0.7 V_{CC}		V_{CC}+0.5	V
V_{OL}	Output low voltage, ports 1, 2, [8]	V_{CC} = 2.7 V; I_{OL} = 1.6 mA[2]	–		0.4	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$[8, 7]	V_{CC} = 2.7 V; I_{OL} = 3.2 mA[2]	–		0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 [3]	V_{CC} = 2.7 V; I_{OH} = –20 μA	V_{CC} – 0.7		–	V
		V_{CC} = 4.5 V; I_{OH} = –30 μA	V_{CC} – 0.7		–	V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE[9], $\overline{PSEN}$[3]	V_{CC} = 2.7 V; I_{OH} = –3.2 mA	V_{CC} – 0.7		–	V
I_{IL}	Logical 0 input current, ports 1, 2, 3	V_{IN} = 0.4 V	–1		–50	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3[6]	V_{IN} = 2.0 V; See note 4	–		–650	μA
I_{LI}	Input leakage current, port 0	0.45 < V_{IN} < V_{CC} – 0.3	–		±10	μA
I_{CC}	Power supply current (see Figure 34 and Source Code):					
	Active mode @ 16 MHz					μA
	Idle mode @ 16 MHz					μA
	Power-down mode or clock stopped (see Figure 30 for conditions) [12]	T_{amb} = 0 °C to 70 °C		2	30	μA
		T_{amb} = –40 °C to +85 °C		3	50	μA
V_{RAM}	RAM keep-alive voltage	–	1.2			V
R_{RST}	Internal reset pull-down resistor	–	40		225	kΩ
C_{IO}	Pin capacitance[10] (except $\overline{EA}$)	–	–		15	pF

NOTES:

1. Typical ratings are not guaranteed. Values listed are based on tests conducted on limited number of samples at room temperature.
2. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.
3. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the V_{CC}–0.7 specification when the address bits are stabilizing.
4. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V.
5. See Figures 36 through 39 for I_{CC} test conditions and Figure 34 for I_{CC} vs. Frequency
   12-clock mode characteristics:
   Active mode (operating): I_{CC} = 1.0 mA + 0.9 mA × FREQ.[MHz]
   Active mode (reset): I_{CC} = 7.0 mA + 0.5 mA x FREQ.[MHz]
   Idle mode: I_{CC} = 1.0 mA + 0.18 mA x FREQ.[MHz]
6. This value applies to T_{amb} = 0 °C to +70 °C. For T_{amb} = –40 °C to +85 °C, I_{TL} = –750 μA.
7. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.
8. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15 mA (*NOTE: This is 85 °C specification.)
   Maximum I_{OL} per 8-bit port: 26 mA
   Maximum total I_{OL} for all outputs: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
9. ALE is tested to V_{OH1}, except when ALE is off then V_{OH} is the voltage specification.
10. Pin capacitance is characterized but not tested. Pin capacitance is less than 25 pF. Pin capacitance of ceramic package is less than 15 pF (except $\overline{EA}$ is 25 pF).
11. To improve noise rejection a nominal 100 ns glitch rejection circuitry has been added to the RST pin, and a nominal 15 ns glitch rejection circuitry has been added to the $\overline{INT0}$ and $\overline{INT1}$ pins. Previous devices provided only an inherent 5 ns of glitch rejection.
12. Power down mode for 3 V range: Commercial Temperature Range – typ: 0.5 μA, max. 20 μA; Industrial Temperature Range – typ. 1.0 μA, max. 30 μA;

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0 °C to +70 °C or –40 °C to +85 °C; **V_{CC} = 5 V ±10%**; V_{SS} = 0 V (30/33 MHz max. CPU clock)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
V_{IL}	Input low voltage[11]	4.5 V < V_{CC} < 5.5 V	–0.5		0.2 V_{CC}–0.1	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, $\overline{EA}$)	–	0.2 V_{CC}+0.9		V_{CC}+0.5	V
V_{IH1}	Input high voltage, XTAL1, RST[11]	–	0.7 V_{CC}		V_{CC}+0.5	V
V_{OL}	Output low voltage, ports 1, 2, 3 [8]	V_{CC} = 4.5 V; I_{OL} = 1.6 mA[2]	–		0.4	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$ [7, 8]	V_{CC} = 4.5 V; I_{OL} = 3.2 mA[2]	–		0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 [3]	V_{CC} = 4.5 V; I_{OH} = –30 µA	V_{CC} – 0.7		–	V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE[9], $\overline{PSEN}$[3]	V_{CC} = 4.5 V; I_{OH} = –3.2 mA	V_{CC} – 0.7		–	V
I_{IL}	Logical 0 input current, ports 1, 2, 3	V_{IN} = 0.4 V	–1		–50	µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3[6]	V_{IN} = 2.0 V; See note 4	–		–650	µA
I_{LI}	Input leakage current, port 0	0.45 < V_{IN} < V_{CC} – 0.3	–		±10	µA
I_{CC}	Power supply current (see Figure 34):					
	Active mode (see Note 5)					
	Idle mode (see Note 5)					
	Power-down mode or clock stopped (see Figure 39 for conditions)	T_{amb} = 0 °C to 70 °C		2	30	µA
		T_{amb} = –40 °C to +85 °C		3	50	µA
V_{RAM}	RAM keep-alive voltage	–	1.2			V
R_{RST}	Internal reset pull-down resistor	–	40		225	kΩ
C_{IO}	Pin capacitance[10] (except $\overline{EA}$)	–	–		15	pF

NOTES:

1. Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.
2. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.
3. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the V_{CC}–0.7 specification when the address bits are stabilizing.
4. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V.
5. See Figures 36 through 39 for I_{CC} test conditions and Figure 34 for I_{CC} vs. Frequency.
   12-clock mode characteristics:
   Active mode (operating): $I_{CC(MAX)}$ = 1.0 mA + 0.9 mA × FREQ.[MHz]
   Active mode (reset): $I_{CC(MAX)}$ = 7.0 mA + 0.5 mA x FREQ.[MHz]
   Idle mode: $I_{CC(MAX)}$ = 1.0 mA + 0.18 mA × FREQ.[MHz]
6. This value applies to T_{amb} = 0°C to +70°C. For T_{amb} = –40°C to +85°C, I_{TL} = –750 µA.
7. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.
8. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15 mA (*NOTE: This is 85 °C specification.)
   Maximum I_{OL} per 8-bit port: 26 mA
   Maximum total I_{OL} for all outputs: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
9. ALE is tested to V_{OH1}, except when ALE is off then V_{OH} is the voltage specification.
10. Pin capacitance is characterized but not tested. Pin capacitance is less than 25 pF. Pin capacitance of ceramic package is less than 15 pF (except $\overline{EA}$ is 25 pF).
11. To improve noise rejection a nominal 100 ns glitch rejection circuitry has been added to the RST pin, and a nominal 15 ns glitch rejection circuitry has been added to the $\overline{INT0}$ and $\overline{INT1}$ pins. Previous devices provided only an inherent 5 ns of glitch rejection.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE
P – $\overline{\text{PSEN}}$
Q – Output data
R – $\overline{\text{RD}}$ signal
t – Time
V – Valid
W – $\overline{\text{WR}}$ signal
X – No longer a valid logic level
Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
t_{LLPL} =Time for ALE low to $\overline{\text{PSEN}}$ low.

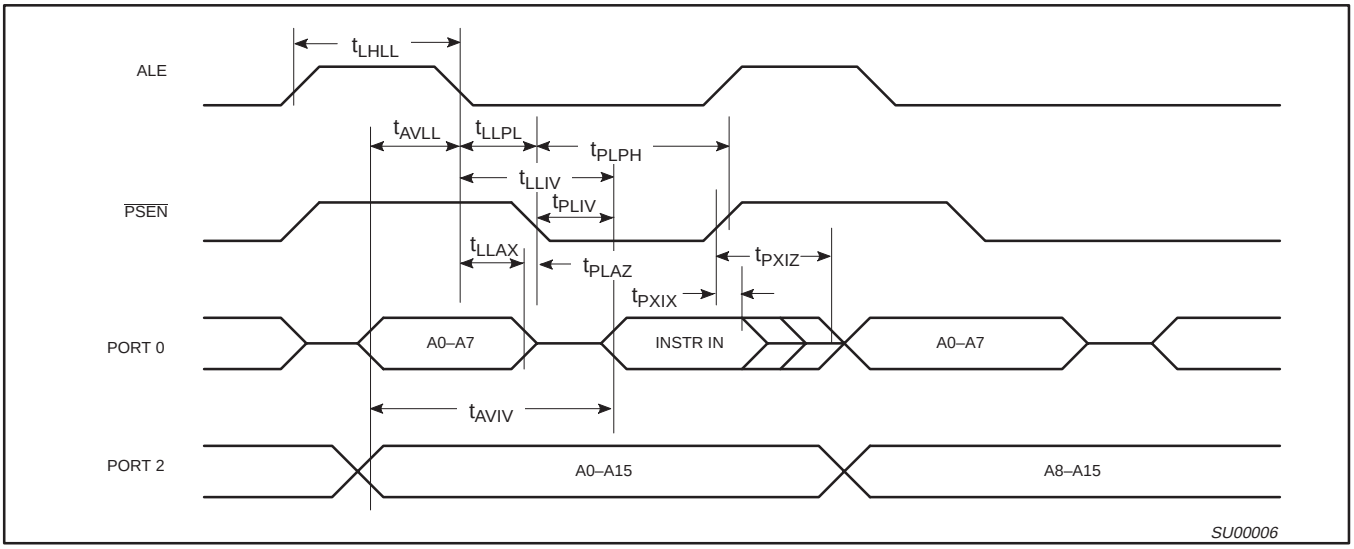


Figure 27. External Program Memory Read Cycle

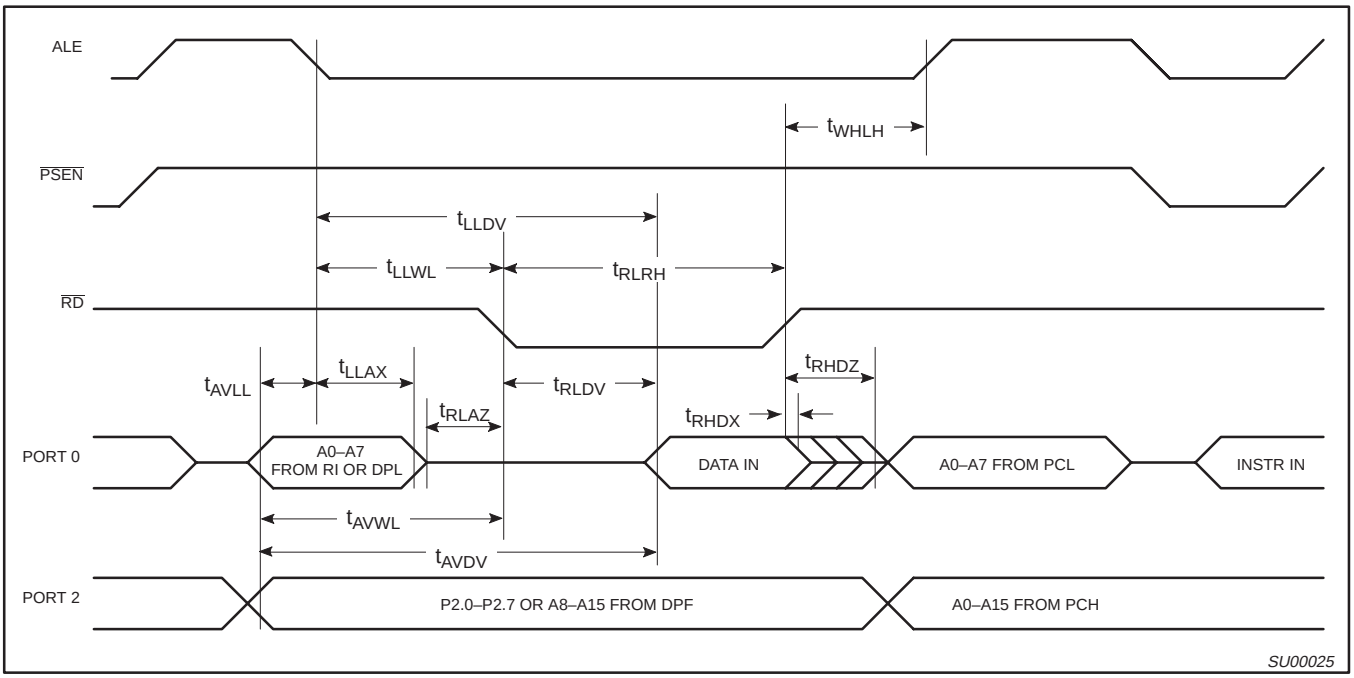


Figure 28. External Data Memory Read Cycle

EPROM CHARACTERISTICS

The OTP devices described in this data sheet can be programmed by using a modified Improved Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses.

The family contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as being manufactured by Philips.

Table 9 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 40 and 41. Figure 42 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 40. Note that the device is running with a 4 to 6 MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 40. The code byte to be programmed into that location is applied to port 0. RST, $\overline{PSEN}$ and pins of ports 2 and 3 specified in Table 9 are held at the 'Program Code Data' levels indicated in Table 9. The ALE/$\overline{PROG}$ is pulsed low 5 times as shown in Figure 41.

To program the encryption table, repeat the 5 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the 5 pulse programming sequence using the 'Pgm Security Bit' levels. After one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bits can still be programmed.

Note that the $\overline{EA}$/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If security bits 2 and 3 have not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 42. The other pins are held at the 'Verify Code Data' levels indicated in Table 9. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the 64 byte encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature bytes

The signature bytes are read by the same procedure as a normal verification of locations 030h and 031h, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030h) = 15h; indicates manufacturer (Philips)
(031h) = 92h/97h/BBh/BDh; indicates P87C51X2/52X2/54X2/58X2.

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 9, and which satisfies the timing specifications, is suitable.

Security Bits

With none of the security bits programmed the code in the program memory can be verified. If the encryption table is programmed, the code will be encrypted when verified. When only security bit 1 (see Table 10) is programmed, MOVC instructions executed from external program memory are disabled from fetching code bytes from the internal memory, $\overline{EA}$ is latched on Reset and all further programming of the EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled. When all three security bits are programmed, all of the conditions above apply and all external program memory execution is disabled.

Encryption Array

64 bytes of encryption array are initially unprogrammed (all 1s).

™Trademark phrase of Intel Corporation.

Table 9. EPROM Programming Modes

MODE	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.7	P2.6	P3.7	P3.6	P3.3
Read signature	1	0	1	1	0	0	0	0	X
Program code data	1	0	0*	V_{PP}	1	0	1	1	X
Verify code data	1	0	1	1	0	0	1	1	X
Pgm encryption table	1	0	0*	V_{PP}	1	0	1	0	X
Pgm security bit 1	1	0	0*	V_{PP}	1	1	1	1	X
Pgm security bit 2	1	0	0*	V_{PP}	1	1	0	0	X
Pgm security bit 3	1	0	0*	V_{PP}	0	1	0	1	X
Program to 6-clock mode	1	0	0*	V_{PP}	0	0	1	0	0
Verify 6-clock[4]	1	0	1	1	e	0	0	1	1
Verify security bits[5]	1	0	1	1	e	0	1	0	X

NOTES:
1. '0' = Valid low for that pin, '1' = valid high for that pin.
2. V_{PP} = 12.75 V ±0.25 V.
3. V_{CC} = 5 V±10% during programming and verification.
4. Bit is output on P0.4 (1 = 12x, 0 = 6x).
5. Security bit one is output on P0.7.
   Security bit two is output on P0.6.
   Security bit three is output on P0.3.

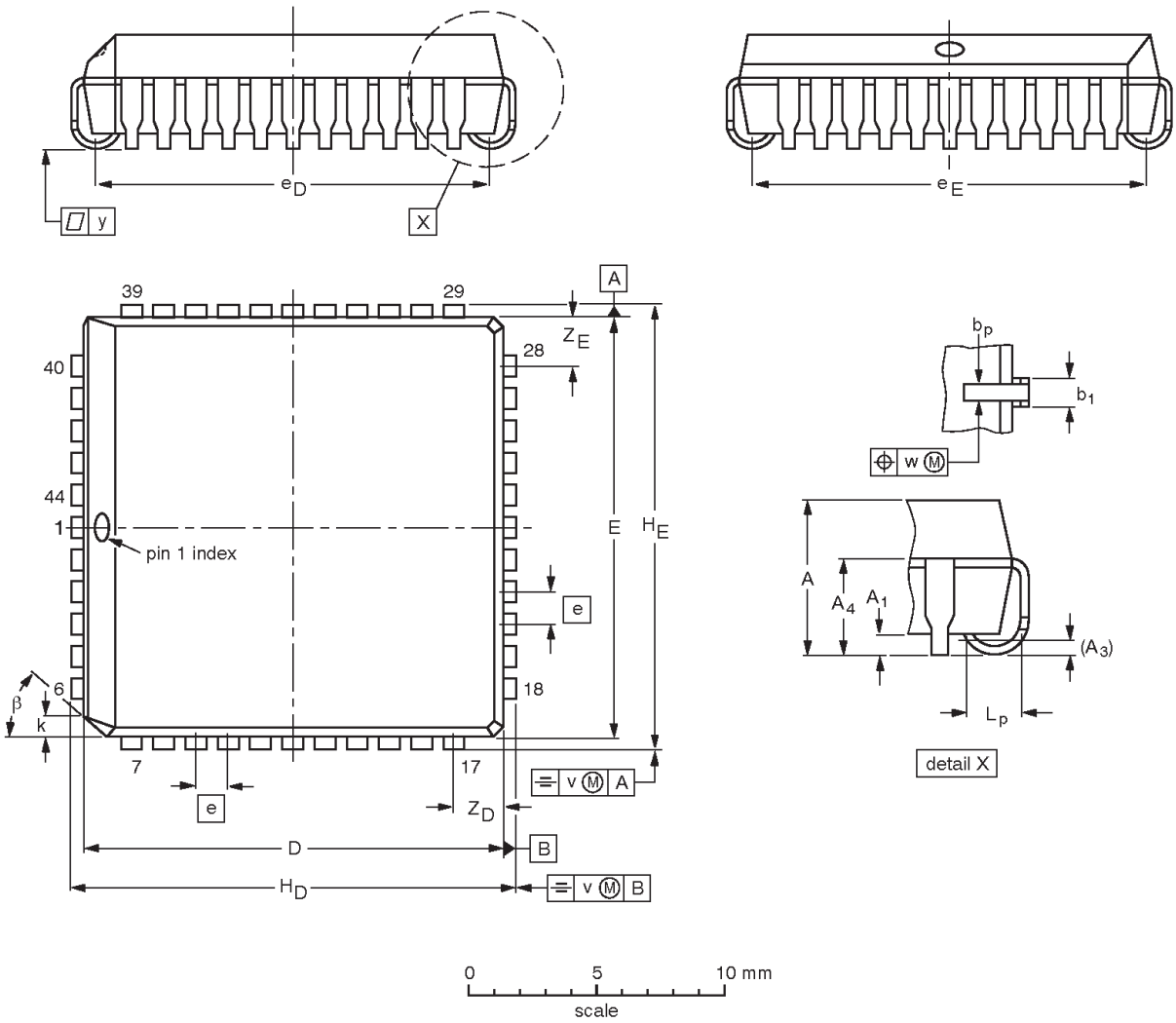
* ALE/$\overline{PROG}$ receives 5 programming pulses for code data (also for user array; 5 pulses for encryption or security bits) while V_{PP} is held at 12.75 V. Each programming pulse is low for 100 µs (±10 µs) and high for a minimum of 10 µs.

Table 10. Program Security Bits for EPROM Devices

PROGRAM LOCK BITS[1, 2]				PROTECTION DESCRIPTION
	SB1	SB2	SB3	
1	U	U	U	No Program Security features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, external execution is disabled. Internal data RAM is not accessible.

NOTES:
1. P – programmed. U – unprogrammed.
2. Any other combination of the security bits is not defined.

PLCC44: plastic leaded chip carrier; 44 leads SOT187-2



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

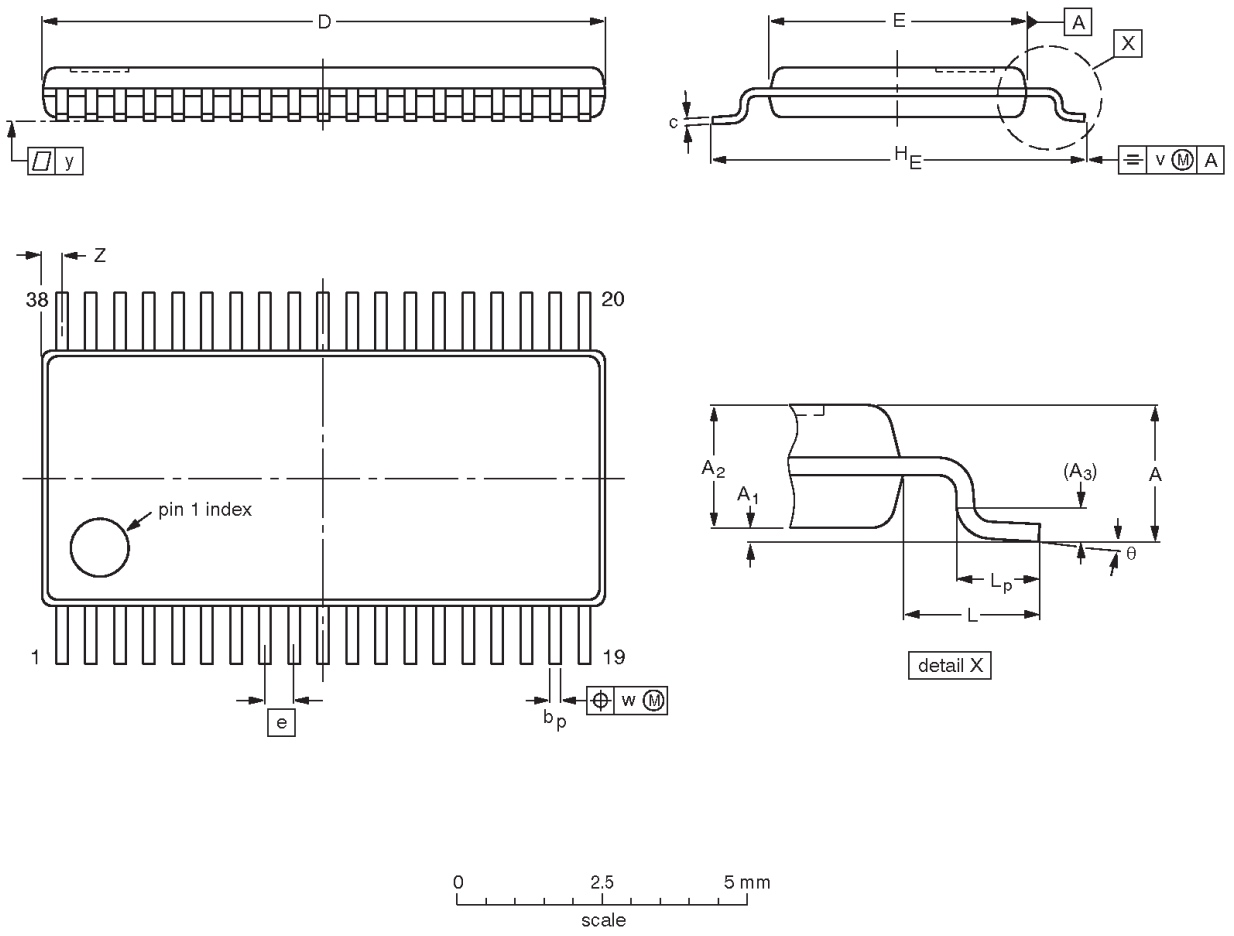
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.63 0.59	0.63 0.59	0.695 0.685	0.695 0.685	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT187-2	112E10	MS-018	EDR-7319			~~99-12-27~~ 01-11-14

TSSOP38: plastic thin shrink small outline package; 38 leads; body width 4.4 mm; lead pitch 0.5 mm **SOT510-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	q
mm	1.10	0.15 0.05	0.95 0.85	0.25	0.27 0.17	0.20 0.09	9.80 9.60	4.50 4.30	0.50	6.40	1.00	0.70 0.50	0.20	0.08	0.08	0.49 0.21	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT510-1							98-09-16

REVISION HISTORY

Rev	Date	Description
_6	20030124	**Product data (9397 750 10995); ECN 853-2337 29260 of 06 December 2002** Modifications: • Added TSSOP38 package details
_5	20020912	**Product data (9397 750 10361); ECN 853-2337 28906 of 12 September 2002**
_4	20020612	**Product data (9397 750 09969); ECN 853-2337 28427 of 12 June 2002**
_3	20020422	**Product data (9397 750 09779); ECN 853-2337 28059 of 22 April 2002**
_2	20020219	**Preliminary data (9397 750 09467)**
_1	20010924	**Preliminary data (9397 750 08895); initial release**