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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-fl.com/product-detail/nxp-semiconductors/p87c58x2fa-512

80C51 8-bit microcontroller family
4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
P87C5xX2

PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER				TYPE	NAME AND FUNCTION
	DIP	PLCC	LQFP	TSSOP		
V _{SS}	20	22	16	9	I	Ground: 0 V reference.
V _{CC}	40	44	38	29	I	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.
P0.0–P0.7	39–32	43–36	37–30	28–21	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification and received code bytes during EPROM programming. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	40–44, 1–3	30–37	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 1 also receives the low-order address byte during program memory verification. Alternate functions for Port 1 include:
	1	2	40	30	I/O	T2 (P1.0): Timer/Counter 2 external count input/clockout (see Programmable Clock-Out)
	2	3	41	31	I	T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction control
P2.0–P2.7	21–28	24–31	18–25	10–17	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. Some Port 2 pins receive the high order address bits during EPROM programming and verification.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	1–6	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	10	11	5	1	I	RxD (P3.0): Serial input port
	11	13	7	2	O	TxD (P3.1): Serial output port
	12	14	8		I	INT0 (P3.2): External interrupt ¹
	13	15	9	3	I	INT1 (P3.3): External interrupt
	14	16	10	4	I	T0 (P3.4): Timer 0 external input
	15	17	11		I	T1 (P3.5): Timer 1 external input ¹
	16	18	12	5	O	WR (P3.6): External data memory write strobe
	17	19	13	6	O	RD (P3.7): External data memory read strobe
RST	9	10	4	38	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V _{SS} permits a power-on reset using only an external capacitor to V _{CC} .
ALE/PROG	30	33	27	19	O	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (12-clock Mode) or 1/3 (6-clock Mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming. ALE can be disabled by setting SFR auxiliary.0. With this bit set, ALE will be active only during a MOVX instruction.

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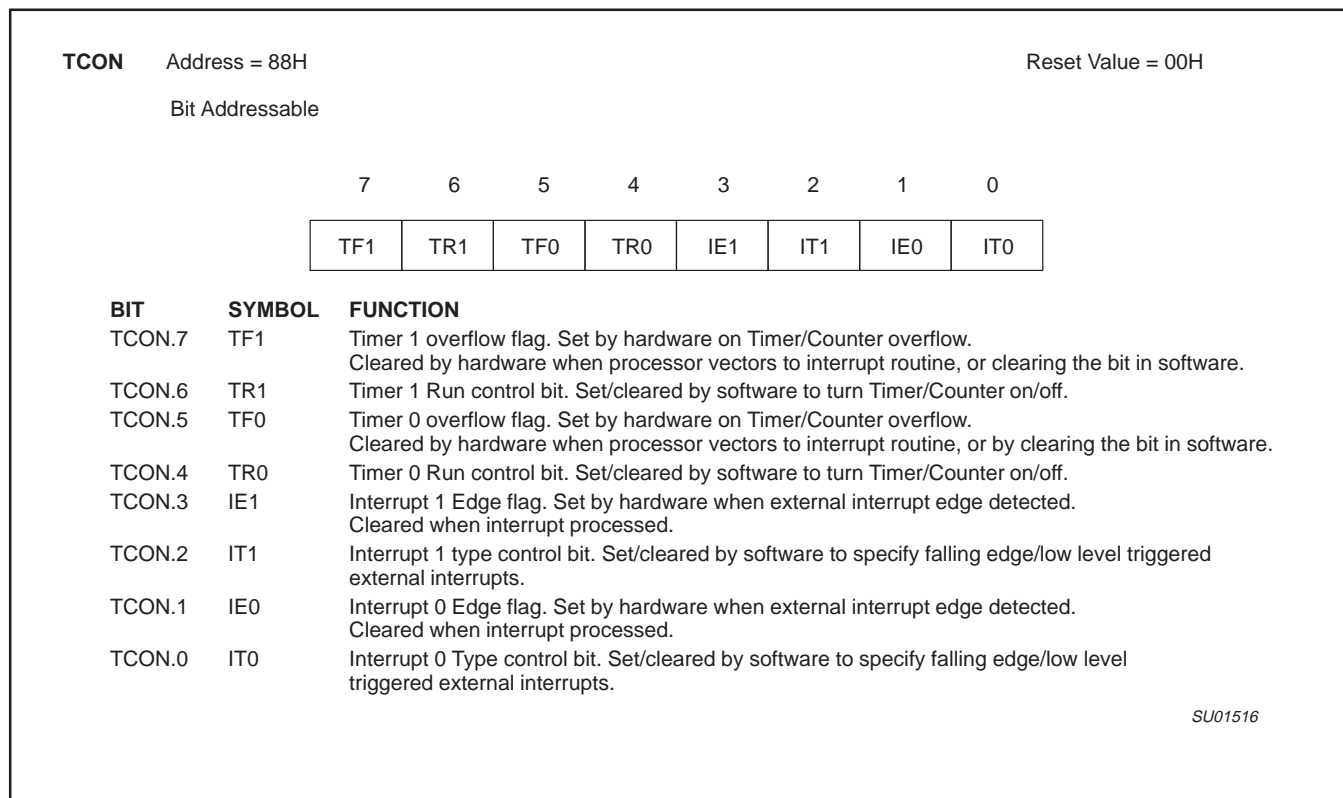


Figure 3. Timer/Counter 0/1 Control (TCON) Register

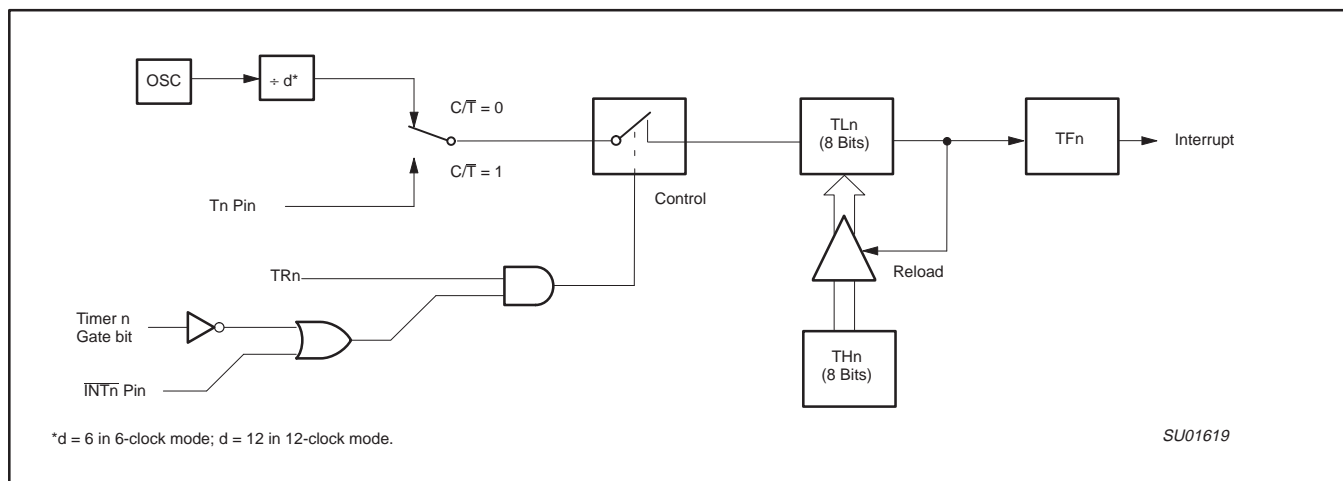


Figure 4. Timer/Counter 0/1 Mode 2: 8-Bit Auto-Reload

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Table 5. Timer 2 Generated Commonly Used Baud Rates

Baud Rate		Osc Freq	Timer 2	
12-clk mode	6-clk mode		RCAP2H	RCAP2L
375 K	750 K	12 MHz	FF	FF
9.6 K	19.2 K	12 MHz	FF	D9
4.8 K	9.6 K	12 MHz	FF	B2
2.4 K	4.8 K	12 MHz	FF	64
1.2 K	2.4 K	12 MHz	FE	C8
300	600	12 MHz	FB	1E
110	220	12 MHz	F2	AF
300	600	6 MHz	FD	8F
110	220	6 MHz	F9	57

Summary Of Baud Rate Equations

Timer 2 is in baud rate generating mode. If Timer 2 is being clocked through pin T2(P1.0) the baud rate is:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

If Timer 2 is being clocked internally, the baud rate is:

$$\text{Baud Rate} = \frac{f_{\text{OSC}}}{[n \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]]}$$

Where:

$n = 16$ in 6-clock mode, 32 in 12-clock mode.

f_{OSC} = Oscillator Frequency

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

$$\text{RCAP2H}, \text{RCAP2L} = 65536 - \left(\frac{f_{\text{OSC}}}{n \times \text{Baud Rate}} \right)$$

Timer/Counter 2 Set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the timer on. See Table 6 for set-up of Timer 2 as a timer. Also see Table 7 for set-up of Timer 2 as a counter.

Table 6. Timer 2 as a Timer

MODE	T2CON	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit Auto-Reload	00H	08H
16-bit Capture	01H	09H
Baud rate generator receive and transmit same baud rate	34H	36H
Receive only	24H	26H
Transmit only	14H	16H

Table 7. Timer 2 as a Counter

MODE	TMOD	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit	02H	0AH
Auto-Reload	03H	0BH

NOTES:

1. Capture/reload occurs only on timer/counter overflow.
2. Capture/reload occurs on timer/counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generator mode.

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FULL-DUPLEX ENHANCED UART

Standard UART operation

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost.) The serial port receive and transmit registers are both accessed at Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

- Mode 0:** Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 the oscillator frequency in 12-clock mode or 1/6 the oscillator frequency in 6-clock mode.
- Mode 1:** 10 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register SCON. The baud rate is variable.
- Mode 2:** 11 bits are transmitted (through TxD) or received (through RxD): start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On Transmit, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency in 12-clock mode or 1/16 or 1/32 the oscillator frequency in 6-clock mode.
- Mode 3:** 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

Multiprocessor Communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. A way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming.

The slaves that weren't being addressed leave their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

Serial Port Control Register

The serial port control and status register is the Special Function Register SCON, shown in Figure 12. This register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Baud Rates

The baud rate in Mode 0 is fixed: Mode 0 Baud Rate = Oscillator Frequency / 12 (12-clock mode) or / 6 (6-clock mode). The baud rate in Mode 2 depends on the value of bit SMOD in Special Function Register PCON. If SMOD = 0 (which is the value on reset), and the port pins in 12-clock mode, the baud rate is 1/64 the oscillator frequency. If SMOD = 1, the baud rate is 1/32 the oscillator frequency. In 6-clock mode, the baud rate is 1/32 or 1/16 the oscillator frequency, respectively.

Mode 2 Baud Rate =

$$\frac{2^{\text{SMOD}}}{n} \times (\text{Oscillator Frequency})$$

Where:

$$n = 64 \text{ in 12-clock mode, } 32 \text{ in 6-clock mode}$$

The baud rates in Modes 1 and 3 are determined by the Timer 1 or Timer 2 overflow rate.

Using Timer 1 to Generate Baud Rates

When Timer 1 is used as the baud rate generator (T2CON.RCLK = 0, T2CON.TCLK = 0), the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

Mode 1, 3 Baud Rate =

$$\frac{2^{\text{SMOD}}}{n} \times (\text{Timer 1 Overflow Rate})$$

Where:

$$n = 32 \text{ in 12-clock mode, } 16 \text{ in 6-clock mode}$$

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either "timer" or "counter" operation, and in any of its 3 running modes. In the most typical applications, it is configured for "timer" operation, in the auto-reload mode (high nibble of TMOD = 0010B). In that case the baud rate is given by the formula:

Mode 1, 3 Baud Rate =

$$\frac{2^{\text{SMOD}}}{n} \times \frac{\text{Oscillator Frequency}}{12 \times [256 - (\text{TH1})]}$$

Where:

$$n = 32 \text{ in 12-clock mode, } 16 \text{ in 6-clock mode}$$

One can achieve very low baud rates with Timer 1 by leaving the Timer 1 interrupt enabled, and configuring the Timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload. Figure 13 lists various commonly used baud rates and how they can be obtained from Timer 1.

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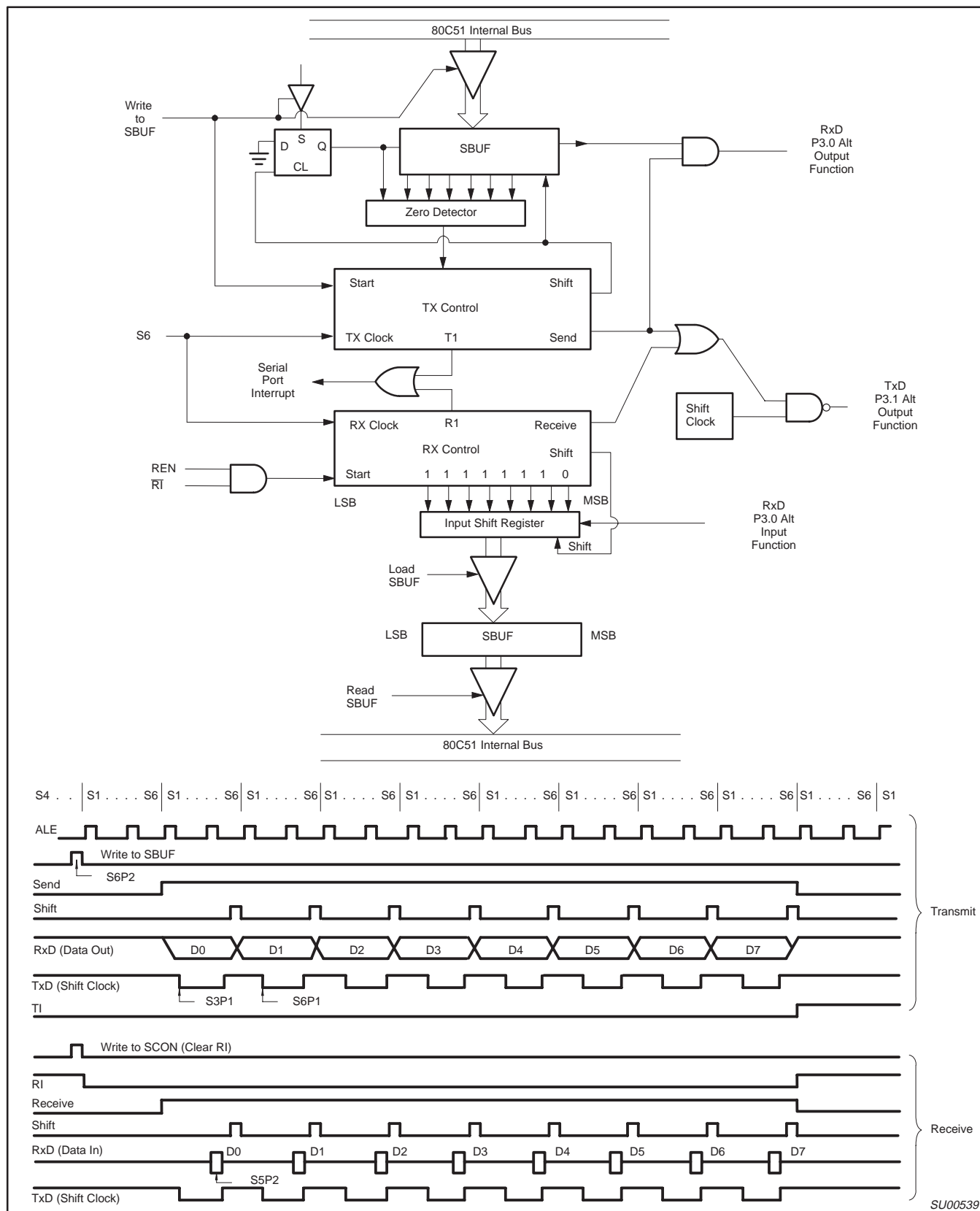
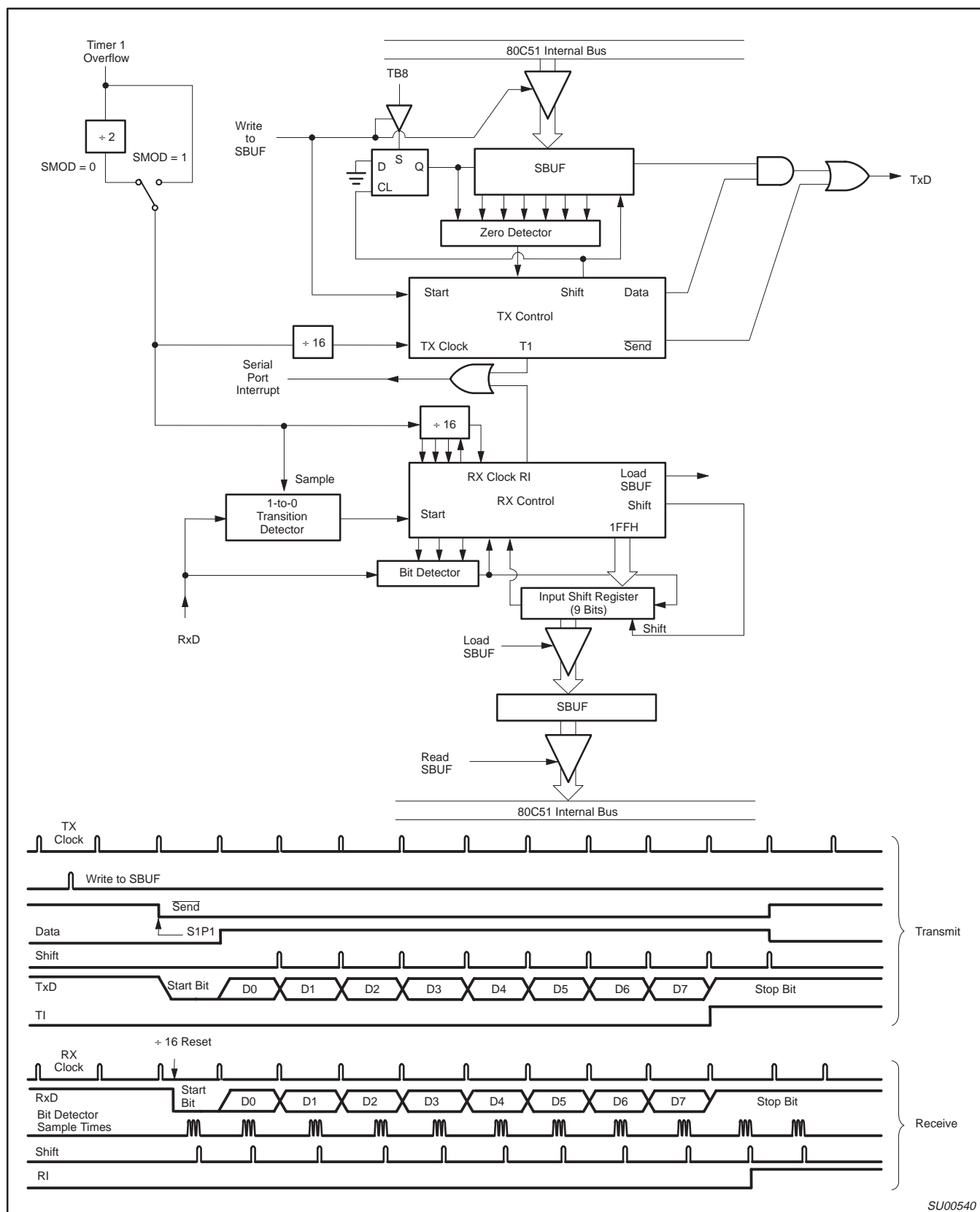


Figure 14. Serial Port Mode 0

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P87C5xX2

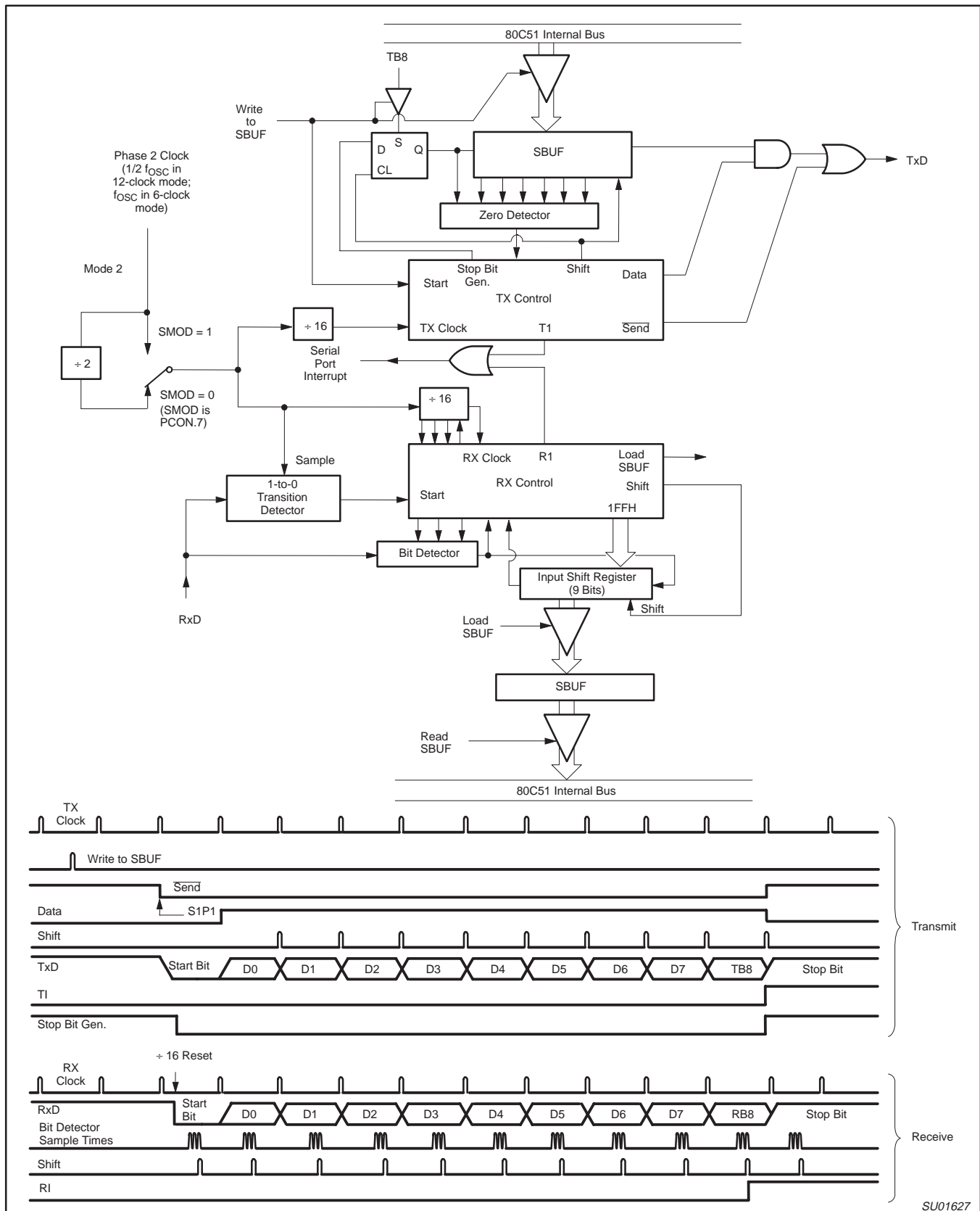


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Figure 15. Serial Port Mode 1

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P87C5xX2



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Figure 16. Serial Port Mode 2

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P80C3xX2; P80C5xX2;
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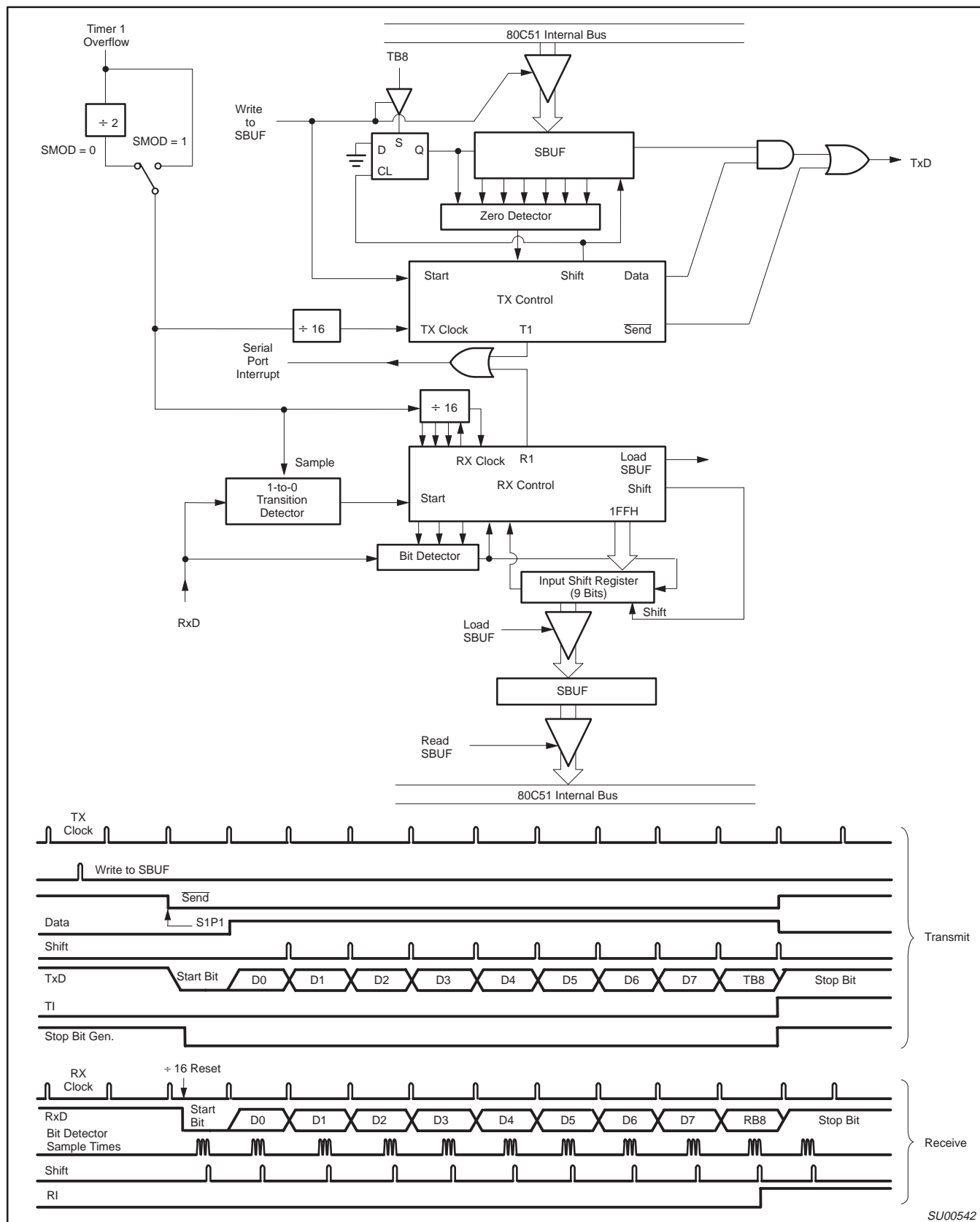


Figure 17. Serial Port Mode 3

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P80C3xX2; P80C5xX2;
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Enhanced UART operation

In addition to the standard operation modes, the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 18). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 19.

Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 20.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0	SADDR =	1100 0000
	SADEN =	<u>1111 1101</u>
	Given =	1100 00X0

Slave 1	SADDR =	1100 0000
	SADEN =	<u>1111 1110</u>
	Given =	1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0	SADDR =	1100 0000
	SADEN =	<u>1111 1001</u>
	Given =	1100 0XX0
Slave 1	SADDR =	1110 0000
	SADEN =	<u>1111 1010</u>
	Given =	1110 0X0X
Slave 2	SADDR =	1110 0000
	SADEN =	<u>1111 1100</u>
	Given =	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are trended as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

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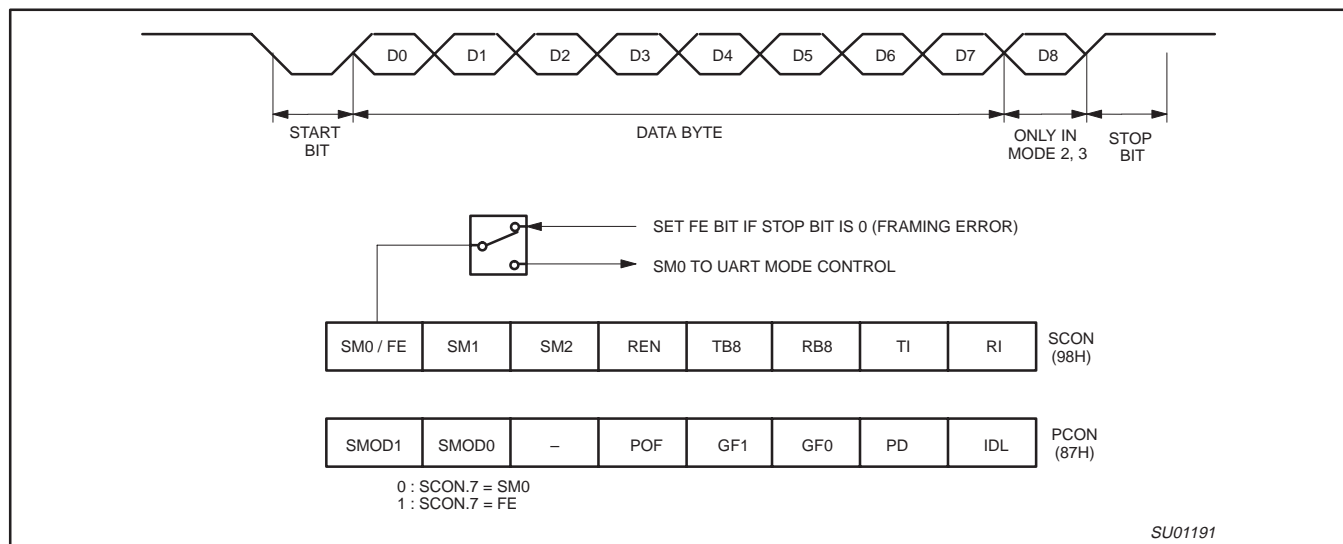


Figure 19. UART Framing Error Detection

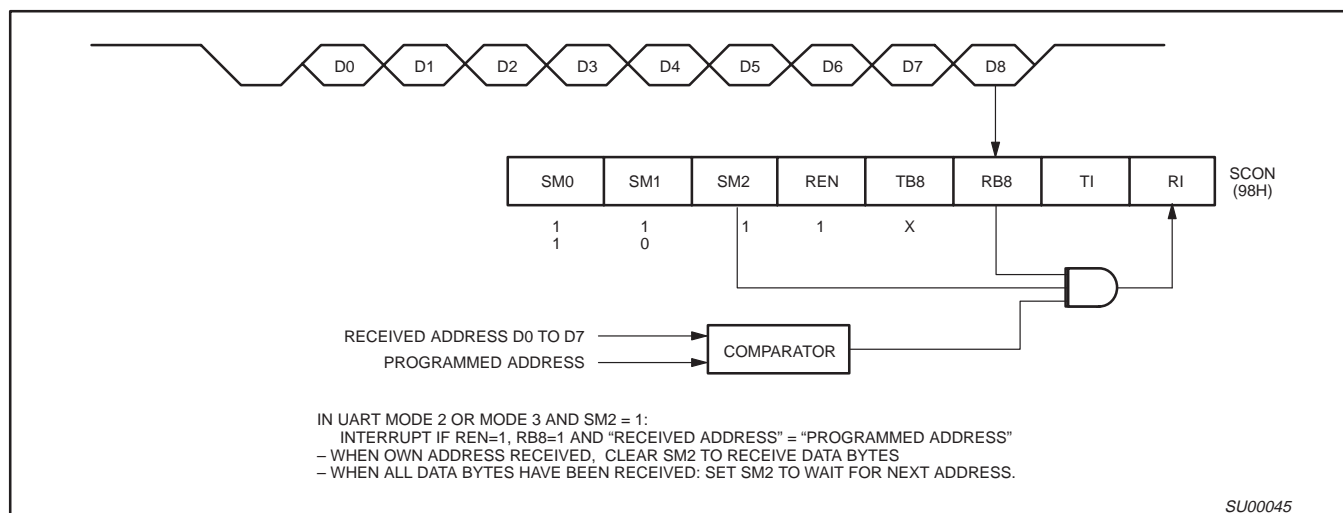


Figure 20. UART Multiprocessor Communication, Automatic Address Recognition

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Interrupt Priority Structure

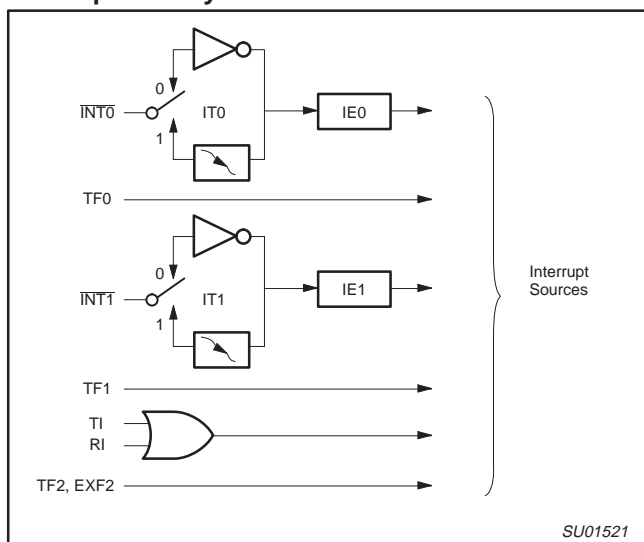


Figure 21. Interrupt Sources

Interrupts

The devices described in this data sheet provide six interrupt sources. These are shown in Figure 21. The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can each be either level-activated or transition-activated, depending on bits IT0 and IT1 in Register TCON. The flags that actually generate these interrupts are bits IE0 and IE1 in TCON. When an external interrupt is generated, the flag that generated it is cleared by the hardware when the service routine is vectored to only if the interrupt was transition-activated. If the interrupt was level-activated, then the external requesting source is what controls the request flag, rather than the on-chip hardware.

The Timer 0 and Timer 1 Interrupts are generated by TF0 and TF1, which are set by a rollover in their respective Timer/Counter registers (except see Timer 0 in Mode 3). When a timer interrupt is generated, the flag that generated it is cleared by the on-chip hardware when the service routine is vectored to.

The Serial Port Interrupt is generated by the logical OR of RI and TI. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine will normally have to determine whether it was RI or TI that generated the interrupt, and the bit will have to be cleared in software.

All of the bits that generate interrupts can be set or cleared by software, with the same result as though it had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be canceled in software.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE (Figure 22). IE also contains a global disable bit, EA, which disables all interrupts at once.

Priority Level Structure

Each interrupt source can also be individually programmed to one of four priority levels by setting or clearing bits in Special Function Registers IP (Figure 23) and IPH (Figure 24). A lower-priority interrupt can itself be interrupted by a higher-priority interrupt, but not by another interrupt of the same level. A high-priority level 3 interrupt can't be interrupted by any other interrupt source.

If two request of different priority levels are received simultaneously, the request of higher priority level is serviced. If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as follows:

Source	Priority Within Level
1. IE0 (External Int 0)	(highest)
2. TF0 (Timer 0)	
3. IE1 (External Int 1)	
4. TF1 (Timer 1)	
5. RI+TI (UART)	
6. TF2, EXF2 (Timer 2)	(lowest)

Note that the "priority within level" structure is only used to resolve simultaneous requests of the same priority level.

The IP and IPH registers contain a number of unimplemented bits. User software should not write 1s to these positions, since they may be used in other 80C51 Family products.

How Interrupts Are Handled

The interrupt flags are sampled at S5P2 of every machine cycle. The samples are polled during the following machine cycle. If one of the flags was in a set condition at S5P2 of the preceding cycle, the polling cycle will find it and the interrupt system will generate an LCALL to the appropriate service routine, provided this hardware-generated LCALL is not blocked by any of the following conditions:

1. An interrupt of equal or higher priority level is already in progress.
2. The current (polling) cycle is not the final cycle in the execution of the instruction in progress.
3. The instruction in progress is RETI or any write to the IE or IP registers.

Any of these three conditions will block the generation of the LCALL to the interrupt service routine. Condition 2 ensures that the instruction in progress will be completed before vectoring to any service routine. Condition 3 ensures that if the instruction in progress is RETI or any access to IE or IP, then at least one more instruction will be executed before any interrupt is vectored to.

The polling cycle is repeated with each machine cycle, and the values polled are the values that were present at S5P2 of the previous machine cycle. Note that if an interrupt flag is active but not being responded to for one of the above conditions, if the flag is not still active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the fact that the interrupt flag was once active but not serviced is not remembered. Every polling cycle is new.

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IE

Address = 0A8H

Reset Value = 0X000000B

Bit Addressable

7	6	5	4	3	2	1	0
EA	—	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables it.

BIT	SYMBOL	FUNCTION
IE.7	EA	Global disable bit. If EA = 0, all interrupts are disabled. If EA = 1, each interrupt can be individually enabled or disabled by setting or clearing its enable bit.
IE.6	—	Not implemented. Reserved for future use.
IE.5	ET2	Timer 2 interrupt enable bit.
IE.4	ES	Serial Port interrupt enable bit.
IE.3	ET1	Timer 1 interrupt enable bit.
IE.2	EX1	External interrupt 1 enable bit.
IE.1	ET0	Timer 0 interrupt enable bit.
IE.0	EX0	External interrupt 0 enable bit.

SU01522

SU01522

Figure 22. Interrupt Enable (IE) Register

IP

Address = 0B8H

Reset Value = xx000000B

Bit Addressable

7	6	5	4	3	2	1	0
—	—	PT2	PS	PT1	PX1	PT0	PX0

Priority Bit = 1 assigns higher priority

Priority Bit = 0 assigns lower priority

BIT	SYMBOL	FUNCTION
IP.7	—	Not implemented, reserved for future use.
IP.6	—	Not implemented, reserved for future use.
IP.5	PT2	Timer 2 interrupt priority bit.
IP.4	PS	Serial Port interrupt priority bit.
IP.3	PT1	Timer 1 interrupt priority bit.
IP.2	PX1	External interrupt 1 priority bit.
IP.1	PT0	Timer 0 interrupt priority bit.
IP.0	PX0	External interrupt 0 priority bit.

SU01523

SU01523

Figure 23. Interrupt Priority (IP) Register

IPH

Address = B7H

Reset Value = xx000000B

Bit Addressable

7	6	5	4	3	2	1	0
—	—	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Priority Bit = 1 assigns higher priority

Priority Bit = 0 assigns lower priority

BIT	SYMBOL	FUNCTION
IPH.7	—	Not implemented, reserved for future use.
IPH.6	—	Not implemented, reserved for future use.
IPH.5	PT2H	Timer 2 interrupt priority bit high.
IPH.4	PSH	Serial Port interrupt priority bit high.
IPH.3	PT1H	Timer 1 interrupt priority bit high.
IPH.2	PX1H	External interrupt 1 priority bit high.
IPH.1	PT0H	Timer 0 interrupt priority bit high.
IPH.0	PX0H	External interrupt 0 priority bit high.

SU01524

SU01524

Figure 24. Interrupt Priority HIGH (IPH) Register

80C51 8-bit microcontroller family
 4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
 low power, high speed (30/33 MHz)

**P80C3xX2; P80C5xX2;
 P87C5xX2**

An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level

interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

Table 8. Interrupt Table

SOURCE	POLLING PRIORITY	REQUEST BITS	HARDWARE CLEAR?	VECTOR ADDRESS
External interrupt 0	1	IE0	N (L) ¹ Y (T) ²	03H
Timer 0	2	TF0	Y	0BH
External interrupt 1	3	IE1	N (L) Y (T)	13H
Timer 1	4	TF1	Y	1BH
UART	5	RI, TI	N	23H
Timer 2	6	TF2, EXF2	N	2BH

NOTES:

1. L = Level activated
2. T = Transition activated

Reduced EMI

All port pins have slew rate controlled outputs. This is to limit noise generated by quickly switching output signals. The slew rate is factory set to approximately 10 ns rise and fall times.

Reduced EMI Mode

The AO bit (AUXR.0) in the AUXR register when set disables the ALE output.

AUXR (8EH)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	AO

AUXR.0 AO Turns off ALE output.

Dual DPTR

The dual DPTR structure (see Figure 26) enables a way to specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 that allows the program code to switch between them.

- New Register Name: AUXR1#
- SFR Address: A2H
- Reset Value: xxx000x0B

AUXR1 (A2H)

7	6	5	4	3	2	1	0
—	—	—	LPEP	WUPD	0	—	DPS

Where:

DPS = AUXR1/bit0 = Switches between DPTR0 and DPTR1.

Select Reg	DPS
DPTR0	0
DPTR1	1

The DPS bit status should be saved by software when switching between DPTR0 and DPTR1.

Note that bit 2 is not writable and is always read as a zero. This allows the DPS bit to be quickly toggled simply by executing an INC DPTR instruction without affecting the WUPD or LPEP bits.

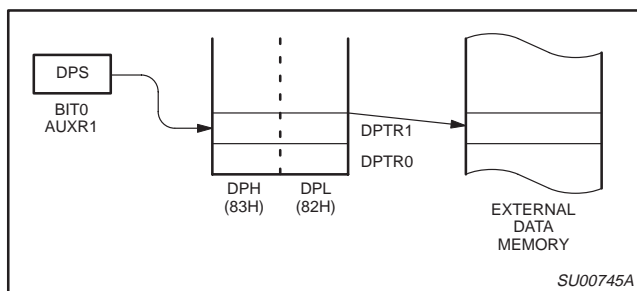


Figure 26.

DPTR Instructions

The instructions that refer to DPTR refer to the data pointer that is currently selected using the AUXR1/bit 0 register. The six instructions that use the DPTR are as follows:

INC DPTR	Increments the data pointer by 1
MOV DPTR, #data16	Loads the DPTR with a 16-bit constant
MOV A, @ A+DPTR	Move code byte relative to DPTR to ACC
MOVX A, @ DPTR	Move external RAM (16-bit address) to ACC
MOVX @ DPTR, A	Move ACC to external RAM (16-bit address)
JMP @ A + DPTR	Jump indirect relative to DPTR

The data pointer can be accessed on a byte-by-byte basis by specifying the low or high byte in an instruction which accesses the SFRs. See application note AN458 for more details.

80C51 8-bit microcontroller family
4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
P87C5xX2

ABSOLUTE MAXIMUM RATINGS^{1, 2, 3}

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or –40 to +85	°C
Storage temperature range	–65 to +150	°C
Voltage on \overline{EA}/V_{PP} pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS}	–0.5 to +6.5	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

AC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ or -40°C to $+85^{\circ}\text{C}$

SYMBOL	FIGURE	PARAMETER	OPERATING MODE	POWER SUPPLY VOLTAGE	CLOCK FREQUENCY RANGE		UNIT
					MIN	MAX	
$1/t_{CLCL}$	31	Oscillator frequency	6-clock	5 V \pm 10%	0	30	MHz
			6-clock	2.7 V to 5.5 V	0	16	MHz
			12-clock	5 V \pm 10%	0	33	MHz
			12-clock	2.7 V to 5.5 V	0	16	MHz

80C51 8-bit microcontroller family
4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
P87C5xX2

DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ or $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{CC} = 2.7\text{ V}$ to 5.5 V ; $V_{SS} = 0\text{ V}$ (16 MHz max. CPU clock)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
V_{IL}	Input low voltage ¹¹	$4.0\text{ V} < V_{CC} < 5.5\text{ V}$	-0.5		$0.2 V_{CC} - 0.1$	V
		$2.7\text{ V} < V_{CC} < 4.0\text{ V}$	-0.5		$0.7 V_{CC}$	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, EA)	—	$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST ¹¹	—	$0.7 V_{CC}$		$V_{CC} + 0.5$	V
V_{OL}	Output low voltage, ports 1, 2, ⁸	$V_{CC} = 2.7\text{ V}$; $I_{OL} = 1.6\text{ mA}^2$	—		0.4	V
V_{OL1}	Output low voltage, port 0, ALE, PSEN ^{8, 7}	$V_{CC} = 2.7\text{ V}$; $I_{OL} = 3.2\text{ mA}^2$	—		0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 ³	$V_{CC} = 2.7\text{ V}$; $I_{OH} = -20\text{ }\mu\text{A}$	$V_{CC} - 0.7$		—	V
		$V_{CC} = 4.5\text{ V}$; $I_{OH} = -30\text{ }\mu\text{A}$	$V_{CC} - 0.7$		—	V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE ⁹ , PSEN ³	$V_{CC} = 2.7\text{ V}$; $I_{OH} = -3.2\text{ mA}$	$V_{CC} - 0.7$		—	V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.4\text{ V}$	-1		-50	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3 ⁶	$V_{IN} = 2.0\text{ V}$; See note 4	—		-650	μA
I_{LI}	Input leakage current, port 0	$0.45 < V_{IN} < V_{CC} - 0.3$	—		± 10	μA
I_{CC}	Power supply current (see Figure 34 and Source Code): Active mode @ 16 MHz Idle mode @ 16 MHz Power-down mode or clock stopped (see Figure 30 for conditions) ¹²	$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$ $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$				μA
				2	30	μA
				3	50	μA
V_{RAM}	RAM keep-alive voltage	—	1.2			V
R_{RST}	Internal reset pull-down resistor	—	40		225	k Ω
C_{IO}	Pin capacitance ¹⁰ (except EA)	—	—		15	pF

NOTES:

- Typical ratings are not guaranteed. Values listed are based on tests conducted on limited number of samples at room temperature.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading $> 100\text{ pF}$), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the $V_{CC} - 0.7$ specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V.
- See Figures 36 through 39 for I_{CC} test conditions and Figure 34 for I_{CC} vs. Frequency
12-clock mode characteristics:
Active mode (operating): $I_{CC} = 1.0\text{ mA} + 0.9\text{ mA} \times \text{FREQ.}[\text{MHz}]$
Active mode (reset): $I_{CC} = 7.0\text{ mA} + 0.5\text{ mA} \times \text{FREQ.}[\text{MHz}]$
Idle mode: $I_{CC} = 1.0\text{ mA} + 0.18\text{ mA} \times \text{FREQ.}[\text{MHz}]$
- This value applies to $T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$. For $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $I_{TL} = -750\text{ }\mu\text{A}$.
- Load capacitance for port 0, ALE, and PSEN = 100 pF, load capacitance for all other outputs = 80 pF.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 15 mA (*NOTE: This is 85 $^{\circ}\text{C}$ specification.)
Maximum I_{OL} per 8-bit port: 26 mA
Maximum total I_{OL} for all outputs: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to V_{OH1} , except when ALE is off then V_{OH} is the voltage specification.
- Pin capacitance is characterized but not tested. Pin capacitance is less than 25 pF. Pin capacitance of ceramic package is less than 15 pF (except EA is 25 pF).
- To improve noise rejection a nominal 100 ns glitch rejection circuitry has been added to the RST pin, and a nominal 15 ns glitch rejection circuitry has been added to the INT0 and INT1 pins. Previous devices provided only an inherent 5 ns of glitch rejection.
- Power down mode for 3 V range: Commercial Temperature Range – typ: 0.5 μA , max. 20 μA ; Industrial Temperature Range – typ. 1.0 μA , max. 30 μA ;

80C51 8-bit microcontroller family
4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
P87C5xX2

AC ELECTRICAL CHARACTERISTICS (12-CLOCK MODE, 2.7 V TO 5.5 V OPERATION)

$T_{amb} = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C or }-40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$ ^{1,2,3,4}

Symbol	Figure	Parameter	Limits		16 MHz Clock		Unit
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	31	Oscillator frequency	0	16	–	–	MHz
t_{LHLL}	27	ALE pulse width	$2t_{CLCL}-10$	–	115	–	ns
t_{AVLL}	27	Address valid to ALE low	$t_{CLCL}-15$	–	47.5	–	ns
t_{LLAX}	27	Address hold after ALE low	$t_{CLCL}-25$	–	37.5	–	ns
t_{LLIV}	27	ALE low to valid instruction in	–	$4t_{CLCL}-55$	–	195	ns
t_{LLPL}	27	ALE low to PSEN low	$t_{CLCL}-15$	–	47.5	–	ns
t_{PLPH}	27	PSEN pulse width	$3t_{CLCL}-15$	–	172.5	–	ns
t_{PLIV}	27	PSEN low to valid instruction in	–	$3t_{CLCL}-55$	–	132.5	ns
t_{PXIX}	27	Input instruction hold after PSEN	0	–	0	–	ns
t_{PXIZ}	27	Input instruction float after PSEN	–	$t_{CLCL}-10$	–	52.5	ns
t_{AVIV}	27	Address to valid instruction in	–	$5t_{CLCL}-50$	–	262.5	ns
t_{PLAZ}	27	PSEN low to address float	–	10	–	10	ns
Data Memory							
t_{RLRH}	28	\overline{RD} pulse width	$6t_{CLCL}-25$	–	350	–	ns
t_{WLWH}	29	\overline{WR} pulse width	$6t_{CLCL}-25$	–	350	–	ns
t_{RLDV}	28	RD low to valid data in	–	$5t_{CLCL}-50$	–	262.5	ns
t_{RHDX}	28	Data hold after RD	0	–	0	–	ns
t_{RHDZ}	28	Data float after RD	–	$2t_{CLCL}-20$	–	105	ns
t_{LLDV}	28	ALE low to valid data in	–	$8t_{CLCL}-55$	–	445	ns
t_{AVDV}	28	Address to valid data in	–	$9t_{CLCL}-50$	–	512.5	ns
t_{LLWL}	28, 29	ALE low to \overline{RD} or \overline{WR} low	$3t_{CLCL}-20$	$3t_{CLCL}+20$	167.5	207.5	ns
t_{AVWL}	28, 29	Address valid to \overline{WR} low or \overline{RD} low	$4t_{CLCL}-20$	–	230	–	ns
t_{QVWX}	29	Data valid to \overline{WR} transition	$t_{CLCL}-30$	–	32.5	–	ns
t_{WHQX}	29	Data hold after \overline{WR}	$t_{CLCL}-20$	–	42.5	–	ns
t_{QVWH}	29	Data valid to \overline{WR} high	$7t_{CLCL}-10$	–	427.5	–	ns
t_{RLAZ}	28	\overline{RD} low to address float	–	0	–	0	ns
t_{WHLH}	28, 29	\overline{RD} or \overline{WR} high to ALE high	$t_{CLCL}-15$	$t_{CLCL}+15$	47.5	77.5	ns
External Clock							
t_{CHCX}	31	High time	$0.32t_{CLCL}$	$t_{CLCL}-t_{CLCX}$	–	–	ns
t_{CLCX}	31	Low time	$0.32t_{CLCL}$	$t_{CLCL}-t_{CHCX}$	–	–	ns
t_{CLCH}	31	Rise time	–	5	–	–	ns
t_{CHCL}	31	Fall time	–	5	–	–	ns
Shift register							
t_{XLXL}	30	Serial port clock cycle time	$12t_{CLCL}$	–	750	–	ns
t_{QVXH}	30	Output data setup to clock rising edge	$10t_{CLCL}-25$	–	600	–	ns
t_{XHQX}	30	Output data hold after clock rising edge	$2t_{CLCL}-15$	–	110	–	ns
t_{XHDX}	30	Input data hold after clock rising edge	0	–	0	–	ns
t_{XHDV}	30	Clock rising edge to input data valid	–	$10t_{CLCL}-133$	–	492	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100 pF, load capacitance for all outputs = 80 pF
- Interfacing the microcontroller to devices with float time up to 45 ns is permitted. This limited bus contention will not cause damage to port 0 drivers.
- Parts are guaranteed by design to operate down to 0 Hz.

80C51 8-bit microcontroller family
4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
P87C5xX2

```

/*
**      as31 version V2.10          / *js* /
**
**
**      source file:  idd_ljmp1.asm
**      list file:   idd_ljmp1.lst   created Fri Apr 20 15:51:40 2001
**
#####
#0000          # AUXR  equ 08Eh
#0000          # CKCON equ 08Fh
#
#
#0000          # org 0
#
# LJMP_LABEL:
0000 /75;/8E;/01; #      MOV      AUXR,#001h   ; turn off ALE
0003 /02;/FF;/FD; #      LJMP     LJMP_LABEL   ; jump to end of address space
0005 /00;         #      NOP
#
#FFFD          # org 0fffdh
#
# LJMP_LABEL:
#
FFFD /02;/FD;FF; #      LJMP LJMP_LABEL
# ;      NOP
#
#
*/

```

SU01499

Figure 35. Source code used in measuring I_{DD} operational

80C51 8-bit microcontroller family
4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
P87C5xX2

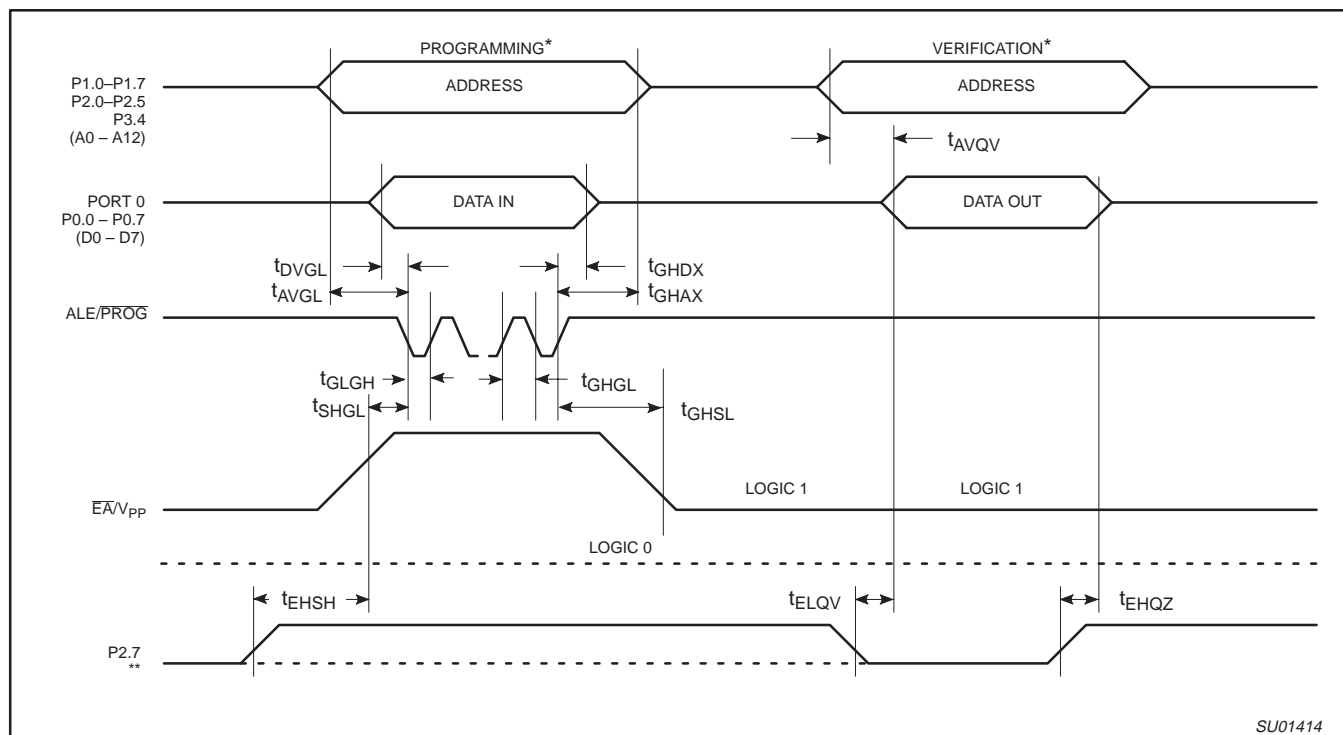
PROGRAMMING AND VERIFICATION CHARACTERISTICS

$T_{amb} = 21\text{ }^{\circ}\text{C}$ to $+27\text{ }^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$ (See Figure 43)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50 ¹	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to \overline{PROG} low	$48t_{CLCL}$		
t_{GHAX}	Address hold after \overline{PROG}	$48t_{CLCL}$		
t_{DVGL}	Data setup to \overline{PROG} low	$48t_{CLCL}$		
t_{GHDX}	Data hold after \overline{PROG}	$48t_{CLCL}$		
t_{EHS}	P2.7 (\overline{ENABLE}) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to \overline{PROG} low	10		μs
t_{GHSL}	V_{PP} hold after \overline{PROG}	10		μs
t_{GLGH}	\overline{PROG} width	90	110	μs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELQZ}	\overline{ENABLE} low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after \overline{ENABLE}	0	$48t_{CLCL}$	
t_{GHGL}	\overline{PROG} high to \overline{PROG} low	10		μs

NOTE:

1. Not tested.



SU01414

NOTES:

* FOR PROGRAMMING CONFIGURATION SEE FIGURE 40.

FOR VERIFICATION CONDITIONS SEE FIGURE 42.

** SEE TABLE 9.

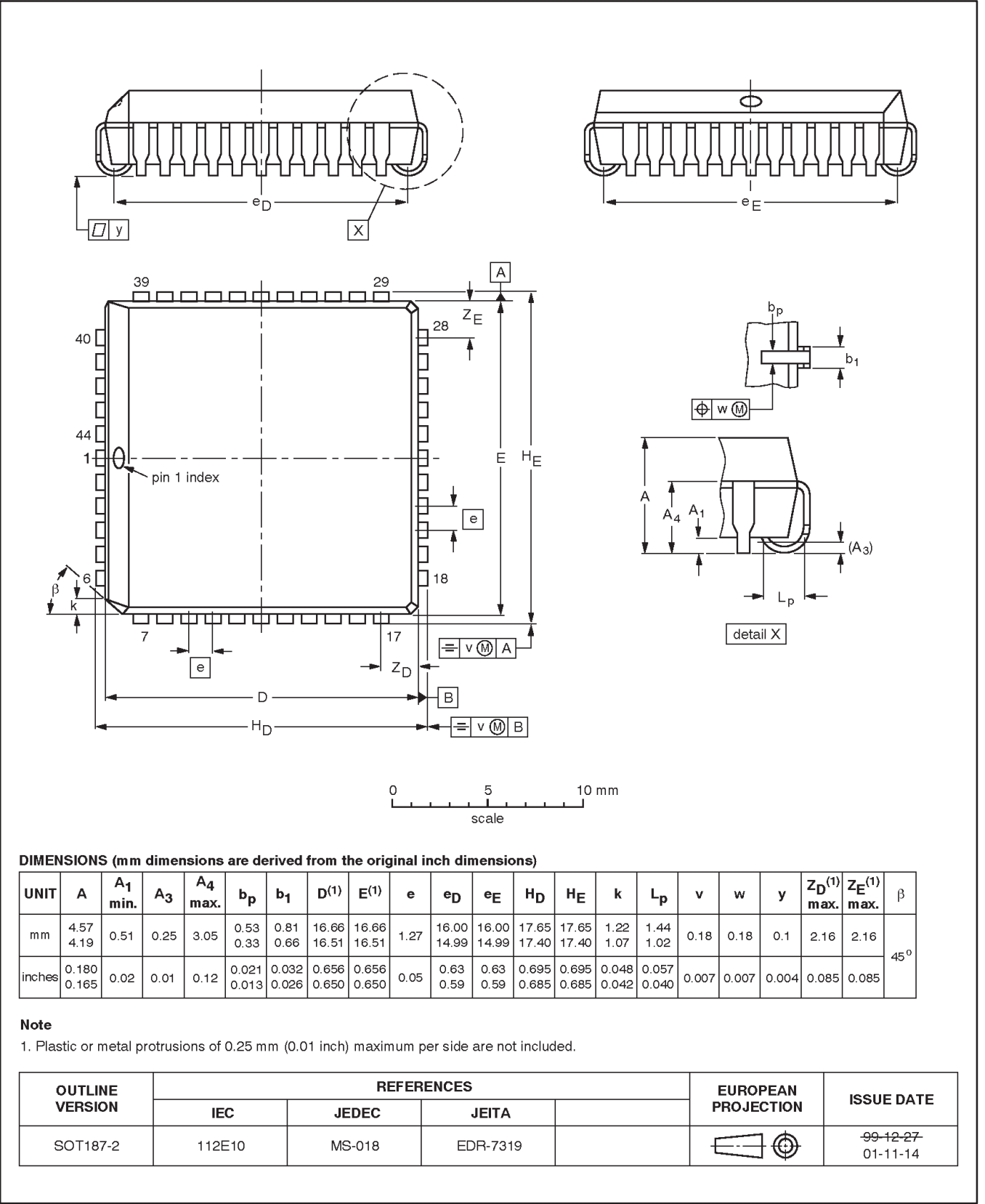
Figure 43. Programming and Verification

80C51 8-bit microcontroller family
4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
P87C5xX2

PLCC44: plastic leaded chip carrier; 44 leads

SOT187-2



80C51 8-bit microcontroller family
 4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
 low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
 P87C5xX2

REVISION HISTORY

Rev	Date	Description
_6	20030124	Product data (9397 750 10995); ECN 853-2337 29260 of 06 December 2002 Modifications: <ul style="list-style-type: none"> • Added TSSOP38 package details
_5	20020912	Product data (9397 750 10361); ECN 853-2337 28906 of 12 September 2002
_4	20020612	Product data (9397 750 09969); ECN 853-2337 28427 of 12 June 2002
_3	20020422	Product data (9397 750 09779); ECN 853-2337 28059 of 22 April 2002
_2	20020219	Preliminary data (9397 750 09467)
_1	20010924	Preliminary data (9397 750 08895); initial release