Infineon Technologies - MB96F353RSBPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	51
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f353rsbpmc-gse2

■ FEATURES

Feature	Description
Technology	• 0.18µm CMOS
CPU	• F²MC-16FX CPU • Up to 56 MHz internal, 17.8 ns instruction cycle time • Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers) • 8-byte instruction execution queue • Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available
System clock	• On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop) • 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor). • Up to 56 MHz external clock • 32-100 kHz subsystem quartz clock • 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog • Clock source selectable from main- and subclock oscillator (part number suffix “W”) and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals. • Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode) • Clock modulator
On-chip voltage regulator	• Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures
Low voltage reset	• Reset is generated when supply voltage is below minimum.
Code Security	• Protects ROM content from unintended read-out
Memory Patch Function	• Replaces ROM content • Can also be used to implement embedded debug support
DMA	• Automatic transfer function independent of CPU, can be assigned freely to resources
Interrupts	• Fast Interrupt processing • 8 programmable priority levels • Non-Maskable Interrupt (NMI)
Timers	• Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer) • Watchdog Timer

■ PIN CIRCUIT TYPE

Pin circuit types

FPT-64P-M23/24	
Pin no.	Circuit type *1
1	Supply
2	G
3 to 15	I
16,17	H
18	Supply
19,20	B *2
19,20	H *3
21 to 23	C
24 to 44	H
45	E
46,47	A
48,49	Supply
50	F
51	H
52,53	N
54 to 61	H
62,63	I
64	Supply

*1: Please refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types
*2: Devices with suffix ”W”
*3: Devices without suffix ”W”

■ RAMSTART/END AND EXTERNAL BUS END ADDRESSES

Devices	Bank 0 RAM size	Bank 1 RAM size	External Bus end address	RAMSTART0	RAMSTART1	RAMEND1
MB96F353/F355	8KByte	-	00:51FF$_H$	00:6240$_H$	-	-
MB96F356	12KByte	-	00:51FF$_H$	00:5240$_H$	-	-

I/O map MB96(F)35x (4 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00006D$_H$	RLT3 - Timer Control Status Register High	TMCSRH3		R/W
00006E$_H$	RLT3 - Reload Register - for writing		TMRLR3	W
00006E$_H$	RLT3 - Reload Register - for reading		TMR3	R
00006F$_H$	RLT3 - Reload Register - for writing			W
00006F$_H$	RLT3 - Reload Register - for reading			R
000070$_H$	RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)	TMCSRL6	TMCSR6	R/W
000071$_H$	RLT6 - Timer Control Status Register High (dedic. RLT for PPG)	TMCSRH6		R/W
000072$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for writing		TMRLR6	W
000072$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R
000073$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for writing			W
000073$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for reading			R
000074$_H$	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10	R/W
000075$_H$	PPG3-PPG0 - General Control register 1 High	GCN1H0		R/W
000076$_H$	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20	R/W
000077$_H$	PPG3-PPG0 - General Control register 2 High	GCN2H0		R/W
000078$_H$	PPG0 - Timer register		PTMR0	R
000079$_H$	PPG0 - Timer register			R
00007A$_H$	PPG0 - Period setting register		PCSR0	W
00007B$_H$	PPG0 - Period setting register			W
00007C$_H$	PPG0 - Duty cycle register		PDUT0	W
00007D$_H$	PPG0 - Duty cycle register			W
00007E$_H$	PPG0 - Control status register Low	PCNL0	PCN0	R/W
00007F$_H$	PPG0 - Control status register High	PCNH0		R/W
000080$_H$	PPG1 - Timer register		PTMR1	R
000081$_H$	PPG1 - Timer register			R
000082$_H$	PPG1 - Period setting register		PCSR1	W

I/O map MB96(F)35x (7 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000DA$_H$	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	R/W
0000DB$_H$	USART2 - Baud Rate Generator Register High	BGRH2		R/W
0000DC$_H$	USART2 - Extended Serial Interrupt Register	ESIR2		R/W
0000DD$_H$	Reserved			-
0000DE$_H$	USART3 - Serial Mode Register	SMR3		R/W
0000DF$_H$	USART3 - Serial Control Register	SCR3		R/W
0000E0$_H$	USART3 - TX Register	TDR3		W
0000E0$_H$	USART3 - RX Register	RDR3		R
0000E1$_H$	USART3 - Serial Status	SSR3		R/W
0000E2$_H$	USART3 - Control/Com. Register	ECCR3		R/W
0000E3$_H$	USART3 - Ext. Status Register	ESCR3		R/W
0000E4$_H$	USART3 - Baud Rate Generator Register Low	BGRL3	BGR3	R/W
0000E5$_H$	USART3 - Baud Rate Generator Register High	BGRH3		R/W
0000E6$_H$	USART3 - Extended Serial Interrupt Register	ESIR3		R/W
0000E7$_H$-0000EF$_H$	Reserved			-
0000F0$_H$-0000FF$_H$	External Bus area	EXTBUS0		R/W
000100$_H$	DMA0 - Buffer address pointer low byte	BAPL0		R/W
000101$_H$	DMA0 - Buffer address pointer middle byte	BAPM0		R/W
000102$_H$	DMA0 - Buffer address pointer high byte	BAPH0		R/W
000103$_H$	DMA0 - DMA control register	DMACS0		R/W
000104$_H$	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	R/W
000105$_H$	DMA0 - I/O register address pointer high byte	IOAH0		R/W
000106$_H$	DMA0 - Data counter low byte	DCTL0	DCT0	R/W
000107$_H$	DMA0 - Data counter high byte	DCTH0		R/W
000108$_H$	DMA1 - Buffer address pointer low byte	BAPL1		R/W
000109$_H$	DMA1 - Buffer address pointer middle byte	BAPM1		R/W
00010A$_H$	DMA1 - Buffer address pointer high byte	BAPH1		R/W
00010B$_H$	DMA1 - DMA control register	DMACS1		R/W
00010C$_H$	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	R/W

I/O map MB96(F)35x (25 of 28)

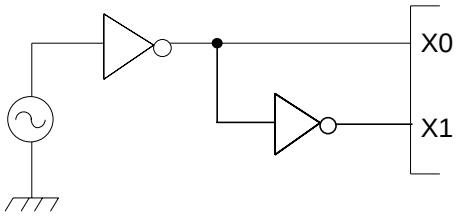
Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000884H-00088FH	Reserved			-
000890H	CAN1 - New Data 1 Register Low	NEWDT1L1	NEWDT11	R
000891H	CAN1 - New Data 1 Register High	NEWDT1H1		R
000892H	CAN1 - New Data 2 Register Low	NEWDT2L1	NEWDT21	R
000893H	CAN1 - New Data 2 Register High	NEWDT2H1		R
000894H-00089FH	Reserved			-
0008A0H	CAN1 - Interrupt Pending 1 Register Low	INTPND1L1	INTPND11	R
0008A1H	CAN1 - Interrupt Pending 1 Register High	INTPND1H1		R
0008A2H	CAN1 - Interrupt Pending 2 Register Low	INTPND2L1	INTPND21	R
0008A3H	CAN1 - Interrupt Pending 2 Register High	INTPND2H1		R
0008A4H-0008AFH	Reserved			-
0008B0H	CAN1 - Message Valid 1 Register Low	MSGVAL1L1	MSGVAL11	R
0008B1H	CAN1 - Message Valid 1 Register High	MSGVAL1H1		R
0008B2H	CAN1 - Message Valid 2 Register Low	MSGVAL2L1	MSGVAL21	R
0008B3H	CAN1 - Message Valid 2 Register High	MSGVAL2H1		R
0008B4H-0008CDH	Reserved			-
0008CEH	CAN1 - Output enable register	COER1		R/W
0008CFH-0008FFH	Reserved			-
000900H	CAN2 - Control register Low	CTRLRL2	CTRLR2	R/W
000901H	CAN2 - Control register High (reserved)	CTRLRH2		R
000902H	CAN2 - Status register Low	STATRL2	STATR2	R/W
000903H	CAN2 - Status register High (reserved)	STATRH2		R
000904H	CAN2 - Error Counter Low (Transmit)	ERRCNTL2	ERRCNT2	R
000905H	CAN2 - Error Counter High (Receive)	ERRCNTH2		R
000906H	CAN2 - Bit Timing Register Low	BTRL2	BTR2	R/W
000907H	CAN2 - Bit Timing Register High	BTRH2		R/W
000908H	CAN2 - Interrupt Register Low	INTRL2	INTR2	R

Interrupt vector table MB96(F)35x (3 of 3)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
67	$2F0_H$				Reserved
68	$2EC_H$	ICU9	Yes	68	Input Capture Unit 9
69	$2E8_H$	ICU10	Yes	69	Input Capture Unit 10
70	$2E4_H$				Reserved
71	$2E0_H$	OCU4	Yes	71	Output Compare Unit 4
72	$2DC_H$	OCU5	Yes	72	Output Compare Unit 5
73	$2D8_H$	OCU6	Yes	73	Output Compare Unit 6
74	$2D4_H$	OCU7	Yes	74	Output Compare Unit 7
75	$2D0_H$				Reserved
76	$2CC_H$				Reserved
77	$2C8_H$	FRT0	Yes	77	Free Running Timer 0
78	$2C4_H$	FRT1	Yes	78	Free Running Timer 1
79	$2C0_H$	FRT2	Yes	79	Free Running Timer 2
80	$2BC_H$	FRT3	Yes	80	Free Running Timer 3
81	$2B8_H$	RTC0	No	81	Real Timer Clock
82	$2B4_H$	CAL0	No	82	Clock Calibration Unit
83	$2B0_H$	IIC0	Yes	83	I2C interface
84	$2AC_H$	ADC0	Yes	84	A/D Converter
85	$2A8_H$	LINR2	Yes	85	LIN USART 2 RX
86	$2A4_H$	LINT2	Yes	86	LIN USART 2 TX
87	$2A0_H$	LINR3	Yes	87	LIN USART 3 RX
88	$29C_H$	LINT3	Yes	88	LIN USART 3 TX
89	298_H	LINR7	Yes	89	LIN USART 7 RX
90	294_H	LINT7	Yes	90	LIN USART 7 TX
91	290_H	LINR8	Yes	91	LIN USART 8 RX
92	$28C_H$	LINT8	Yes	92	LIN USART 8 TX
93	288_H	FLASH_A	No	93	Flash memory A (only Flash devices)

2. Opposite phase external clock

- When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



4. Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

5. Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

6. Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 µF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

7. Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

8. Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

9. Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, AV_{SS} = AVRH = AVRL = V_{SS}.

10. Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2 V to 2.7 V.

3. DC characteristics

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
			CMOS Hysteresis 0.7/0.3 input selected	0.7 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} \geq 4.5V$
				0.74 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} < 4.5V$
			AUTOMOTIVE Hysteresis input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
			TTL input selected	2.0	-	V_{CC} + 0.3	V	
	V_{IHX0F}	X0	External clock in “Fast Clock Input mode”	0.8 V_{CC}	-	V_{CC} + 0.3	V	
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	2.5	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	0.8 V_{CC}	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	V_{SS} - 0.3	-	0.2 V_{CC}	V	
			CMOS Hysteresis 0.7/0.3 input selected	V_{SS} - 0.3	-	0.3 V_{CC}	V	
			AUTOMOTIVE Hysteresis input selected	V_{SS} - 0.3	-	0.5 V_{CC}	V	$V_{CC} \geq 4.5V$
				V_{SS} - 0.3	-	0.46 V_{CC}		$V_{CC} < 4.5V$
			TTL input selected	V_{SS} - 0.3	-	0.8	V	
	V_{ILX0F}	X0	External clock in “Fast Clock Input mode”	V_{SS} - 0.3	-	0.2 V_{CC}	V	
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	V_{SS} - 0.3	-	0.4	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes*	I_{CCPLL}	PLL Run mode with CLKS1/2 = CLKB = CLKP1 = 16MHz, CLKP2 = 8MHz 1 Flash/ROM wait state (CLKRC and CLKSC stopped)	+25˚C	14.5	19.5	mA	MB96F353/F355
			+125˚C	16	23		
			+25˚C	15	20	mA	MB96F356
			+125˚C	16.5	23.5		
		PLL Run mode with CLKS1/2 = CLKB = CLKP1 = 32MHz, CLKP2 = 16MHz 2 Flash/ROM wait states (CLKRC and CLKSC stopped)	+25˚C	23	29	mA	MB96F353/F355
			+125˚C	25	33		
			+25˚C	24	30	mA	MB96F356
			+125˚C	26	34		
		PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz 0 Flash/ROM wait states (CLKRC and CLKSC stopped)	+25˚C	26	38	mA	MB96F353/F355
			+125˚C	28	42		
			+25˚C	28	40	mA	MB96F356
			+125˚C	30	44		
		PLL Run mode with CLKS1/2 = CLKB = CLKP1= 56MHz, CLKP2 = 28MHz 2 Flash/ROM wait states (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	40	51	mA	MB96F353/F355
			+125˚C	42	55		
			+25˚C	41	52	mA	MB96F356
			+125˚C	43	56		
		PLL Run mode with CLKS1/2 = 96MHz, CLKB = CLKP1= 48MHz, CLKP2 = 24MHz 1 Flash/ROM wait state (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	43	56	mA	MB96F353/F355
			+125˚C	45	60		
			+25˚C	44	58	mA	MB96F356
			+125˚C	46	62		

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes*	I_{CCMAIN}	Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz 1 Flash/ROM wait state (CLKPLL, CLKSC and CLKRC stopped)	+25˚C	4	5	mA	MB96F353/F355
			+125˚C	4.7	8		
			+25˚C	4.2	5.2	mA	MB96F356
			+125˚C	4.9	8.2		
	I_{CCRCH}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 2MHz 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped)	+25˚C	2.5	3.5	mA	MB96F353/F355
			+125˚C	3.2	6.5		
			+25˚C	2.7	3.7	mA	MB96F356
			+125˚C	3.4	6.7		
	I_{CCRCL}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 0 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.18	0.3	mA	MB96F353/F355
			+125˚C	0.73	3.1		
			+25˚C	0.4	0.6	mA	MB96F356
			+125˚C	0.95	3.4		
		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 1 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed)	+25˚C	0.15	0.25	mA	MB96F353/F355/F356
			+125˚C	0.7	3.05		
	I_{CCSUB}	Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed)	+25˚C	0.1	0.2	mA	MB96F353/F355/F356
			+125˚C	0.65	3		

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes*	I_{CCTRCH}	RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.1	0.2	mA	MB96F353/F355
			+125˚C	0.63	3		
			+25˚C	0.35	0.5	mA	MB96F356
			+125˚C	0.85	3.3		
		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.07	0.15	mA	MB96F353/F355/ F356
			+125˚C	0.6	2.9		
	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.06	0.15	mA	MB96F353/F355
			+125˚C	0.56	2.95		
			+25˚C	0.3	0.45	mA	MB96F356
			+125˚C	0.8	3.2		
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.03	0.1	mA	MB96F353/F355/ F356
			+125˚C	0.53	2.85		
	I_{CCTSUB}	Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25˚C	0.035	0.1	mA	MB96F353/F355/ F356
			+125˚C	0.53	2.85		
Power supply current in Stop Mode	I_{CCH}	VRCR:LPMB[2:0] = 110_B (Core voltage at 1.8V)	+25˚C	0.02	0.08	mA	MB96F353/F355/ F356
			+125˚C	0.52	2.8		
		VRCR:LPMB[2:0] = 000_B (Core voltage at 1.2V)	+25˚C	0.015	0.06	mA	MB96F353/F355/ F356
			+125˚C	0.4	2.3		
Power supply current for active Low Voltage detector	I_{CCLVD}	Low voltage detector enabled (RCR:LVDE = 1)	+25˚C	5	10	µA	MB96F353/F355
			+125˚C	7	20	µA	Must be added to all current above
			+25˚C	90	140	µA	MB96F356
			+125˚C	100	150		Must be added to all current above

Internal Clock timing

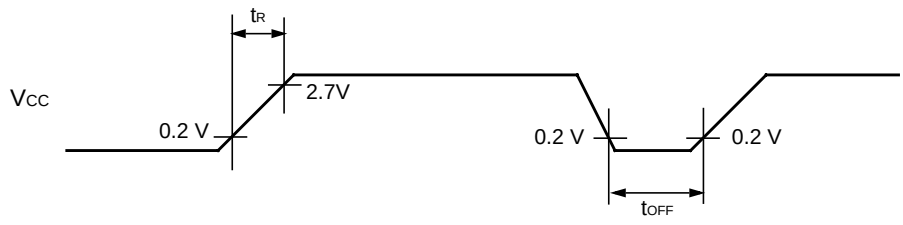
(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8V		1.9V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	0	92	0	96	MHz	Others than below
		0	88	0	96	MHz	MB96F356
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	0	52	0	56	MHz	
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	0	28	0	32	MHz	

Power On Reset timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	



If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

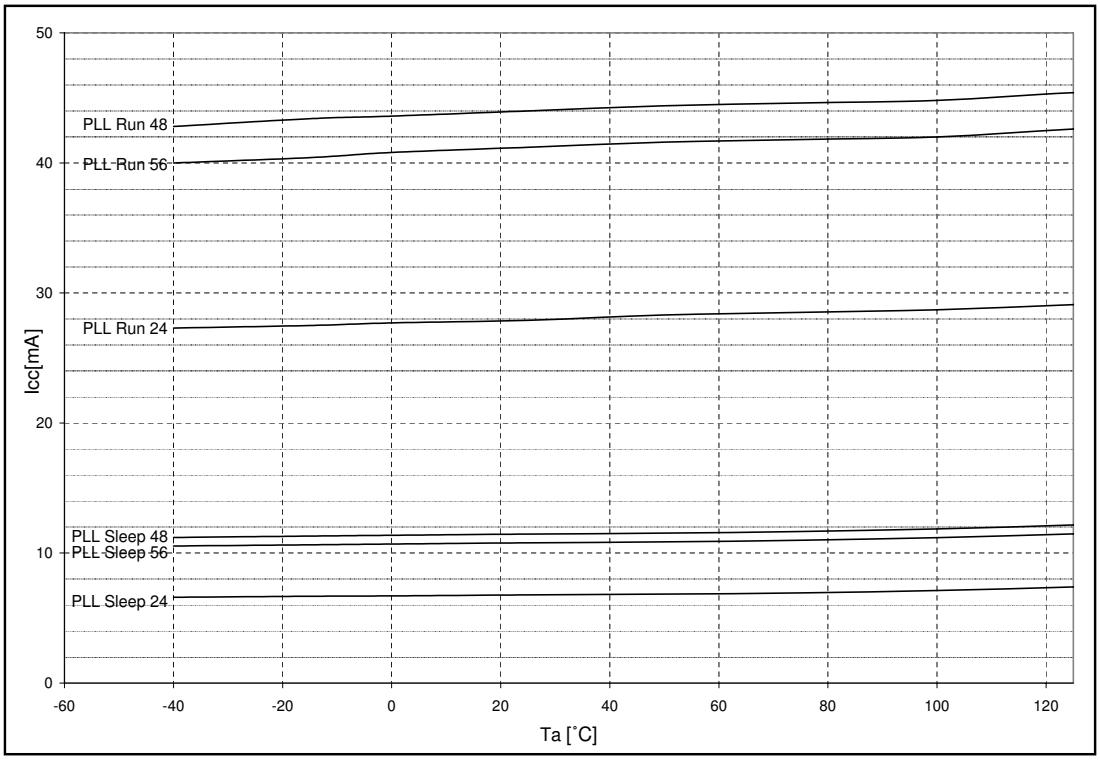
5. Analog Digital Converter

(T_A = -40 ˚C to +125 ˚C, 3.0 V ≤ AVRH - AVRL, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

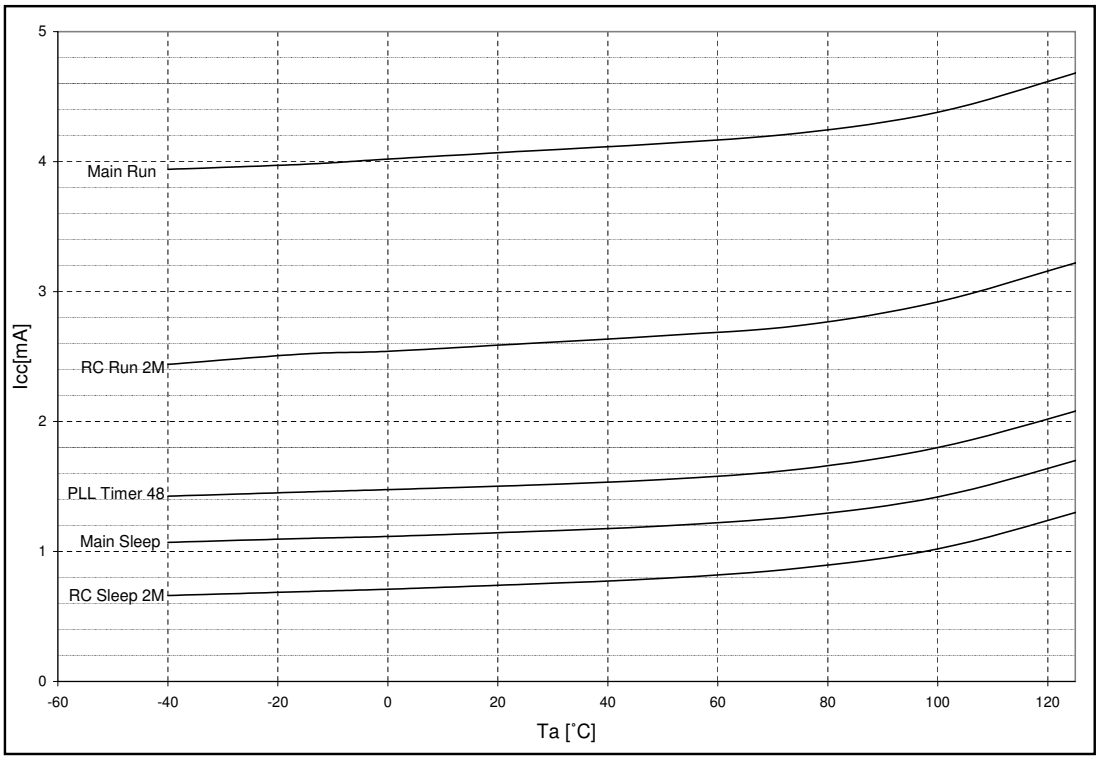
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-	-	± 3	LSB	
Nonlinearity error	-	-	-	-	± 2.5	LSB	
Differential nonlinearity error	-	-	-	-	± 1.9	LSB	
Zero transition voltage	V_{OT}	ANn	AVRL - 1.5 LSB	AVRL+ 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale transition voltage	V_{FST}	ANn	AVRH - 3.5 LSB	AVRH - 1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	-	-	1.0	-	16,500	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.0	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Sampling time	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Analog input leakage current (during conversion)	I_{AIN}	ANn	-1	-	+1	µA	T_A ≤ 105 ˚C, AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
			-1.2	-	+1.2	µA	105 ˚C < T_A ≤ 125 ˚C, AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH	0.75 AVcc	-	AVcc	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AVcc	-	2.5	5	mA	A/D Converter active
	I_{AH}	AVcc	-	-	5	µA	A/D Converter not operated
Reference voltage current	I_R	AVRH/ AVRL	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH/ AVRL	-	-	5	µA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

Note: The accuracy gets worse as |AVRH - AVRL| becomes smaller.

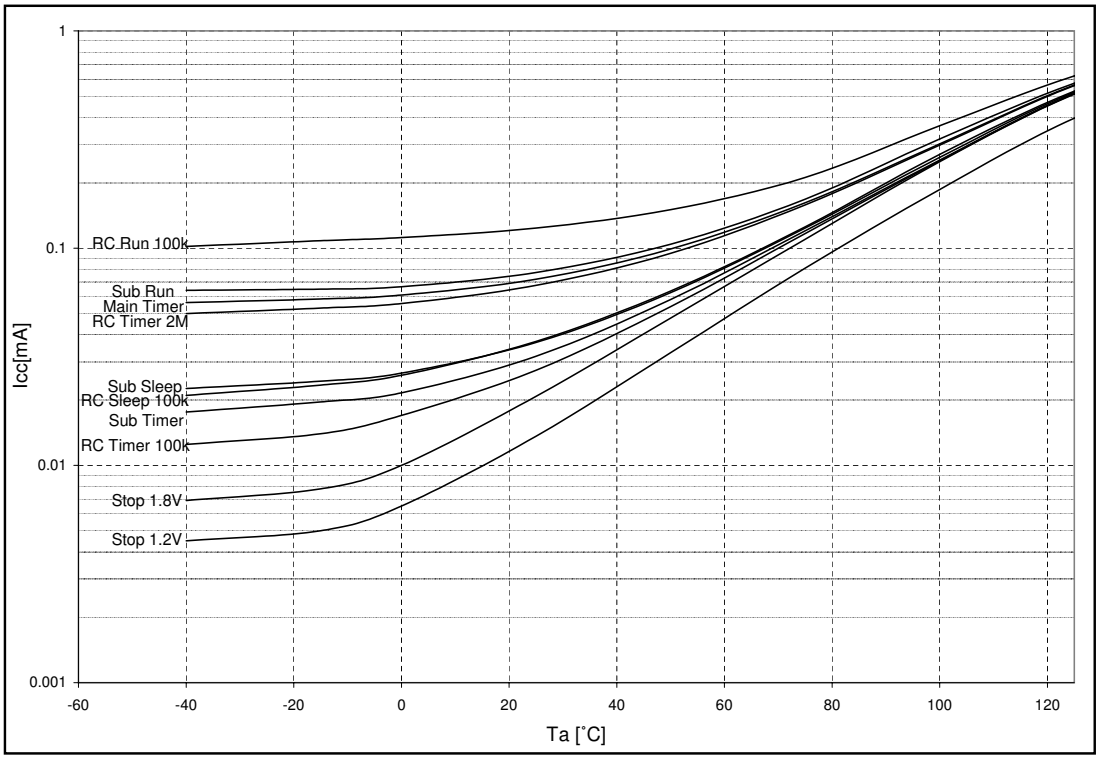
MB96F356 PLL Run and Sleep mode currents



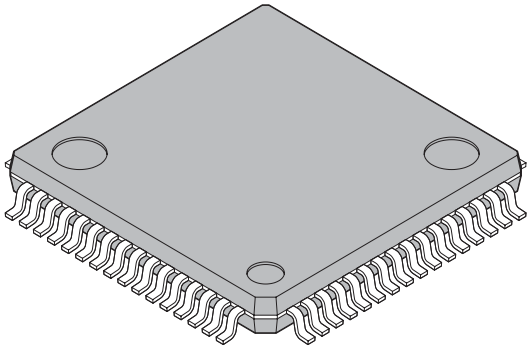
MB96F356 operation modes with medium currents



MB96F356 Low power mode currents

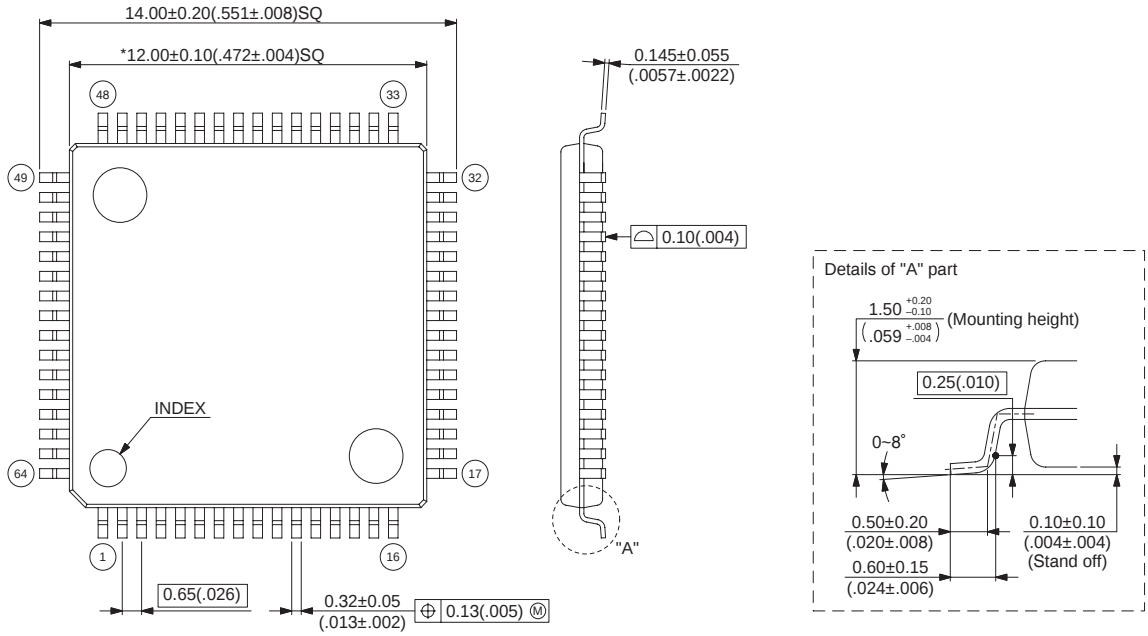


■ PACKAGE DIMENSION MB96(F)35x LQFP 64 - M23

64-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LFQFP64-12×12-0.65
(FPT-64P-M23)		

64-pin plastic LQFP
(FPT-64P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

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