Infineon Technologies - MB96F355ASBPMC1-GSE2 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	51
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f355asbpmc1-gse2

■ PIN FUNCTION DESCRIPTION

Pin Function description (1 of 2)

Pin name	Feature	Description
ADn	External bus	External bus interface (multiplexed mode) address output and data input/output
ADTG_R	ADC	Relocated A/D converter trigger input
ALE	External bus	External bus Address Latch Enable output
An	External bus	External bus address output
ANn	ADC	A/D converter channel n input
AV_{CC}	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AV_{SS}	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTn_R	Clock output function	Relocated Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
ECLK	External bus	External bus clock output
CSn_R	External bus	Relocated External bus chip select n output
FRCKn	Free Running Timer	Free Running Timer n input
HAKX	External bus	External bus Hold Acknowledge
HRQ	External bus	External bus Hold Request
INn	ICU	Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
MDn	Core	Input pins for specifying the operating mode.
NMI_R	External Interrupt	Relocated Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
PPGn_R	PPG	Relocated Programmable Pulse Generator n output
RDX	External bus	External bus interface read strobe output
RDY	External bus	External bus interface external wait state request input

Pin Function description (2 of 2)

Pin name	Feature	Description
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I2C	I2C interface n clock I/O input/output
SDAn	I2C	I2C interface n serial data I/O input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TINn_R	Reload Timer	Relocated Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TOTn_R	Reload Timer	Relocated Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TTGn_R	PPG	Relocated Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
V_{CC}	Supply	Power supply
V_{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte write strobe output
WRLX/WRX	External bus	External bus Low byte / Word write strobe output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

■ USER ROM MEMORY MAP FOR FLASH DEVICES

Alternative mode CPU address	Flash memory mode address	MB96F353 Flash size 96kByte	MB96F355 Flash size 160kByte	MB96F356 Flash size 288kByte	
FF:FFFF$_H$ FF:0000$_H$	3F:FFFF$_H$ 3F:0000$_H$	S39 - 64K	S39 - 64K	S39 - 64K	Flash A
FE:FFFF$_H$ FE:0000$_H$	3E:FFFF$_H$ 3E:0000$_H$	External bus	S38 - 64K	S38 - 64K	
FD:FFFF$_H$ FD:0000$_H$	3D:FFFF$_H$ 3D:0000$_H$		External bus	S37 - 64K	
FC:FFFF$_H$ FC:0000$_H$	3C:FFFF$_H$ 3C:0000$_H$			S36 - 64K	
FB:FFFF$_H$ FB:0000$_H$	3B:FFFF$_H$ 3B:0000$_H$			External bus	
FA:FFFF$_H$ FA:0000$_H$	3A:FFFF$_H$ 3A:0000$_H$				
F9:FFFF$_H$ F9:0000$_H$	39:FFFF$_H$ 39:0000$_H$				
F8:FFFF$_H$ F8:0000$_H$	38:FFFF$_H$ 38:0000$_H$				
F7:FFFF$_H$ F7:0000$_H$	37:FFFF$_H$ 37:0000$_H$				
F6:FFFF$_H$ F6:0000$_H$	36:FFFF$_H$ 36:0000$_H$				
F5:FFFF$_H$ F5:0000$_H$	35:FFFF$_H$ 35:0000$_H$				
F4:FFFF$_H$ F4:0000$_H$	34:FFFF$_H$ 34:0000$_H$				
F3:FFFF$_H$ F3:0000$_H$	33:FFFF$_H$ 33:0000$_H$				
F2:FFFF$_H$ F2:0000$_H$	32:FFFF$_H$ 32:0000$_H$				
F1:FFFF$_H$ F1:0000$_H$	31:FFFF$_H$ 31:0000$_H$				
F0:FFFF$_H$ F0:0000$_H$	30:FFFF$_H$ 30:0000$_H$				
E0:FFFF$_H$ E0:0000$_H$					
DF:FFFF$_H$ DF:8000$_H$		Reserved	Reserved	Reserved	
DF:7FFF$_H$ DF:6000$_H$	1F:7FFF$_H$ 1F:6000$_H$	SA3 - 8K	SA3 - 8K	SA3 - 8K	Flash A
DF:5FFF$_H$ DF:4000$_H$	1F:5FFF$_H$ 1F:4000$_H$	SA2 - 8K	SA2 - 8K	SA2 - 8K	
DF:3FFF$_H$ DF:2000$_H$	1F:3FFF$_H$ 1F:2000$_H$	SA1 - 8K	SA1 - 8K	SA1 - 8K	
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SA0 - 8K *1	SA0 - 8K *1	SA0 - 8K *1	
DE:FFFF$_H$ DE:0000$_H$		Reserved	Reserved	Reserved	

*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

I/O map MB96(F)35x (19 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00058F$_H$	PPG10 - Control status register High	PCNH10		R/W
000590$_H$	PPG11 - Timer register		PTMR11	R
000591$_H$	PPG11 - Timer register			R
000592$_H$	PPG11 - Period setting register		PCSR11	W
000593$_H$	PPG11 - Period setting register			W
000594$_H$	PPG11 - Duty cycle register		PDUT11	W
000595$_H$	PPG11 - Duty cycle register			W
000596$_H$	PPG11 - Control status register Low	PCNL11	PCN11	R/W
000597$_H$	PPG11 - Control status register High	PCNH11		R/W
000598$_H$	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599$_H$	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
00059A$_H$	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
00059B$_H$	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
00059C$_H$	PPG12 - Timer register		PTMR12	R
00059D$_H$	PPG12 - Timer register			R
00059E$_H$	PPG12 - Period setting register		PCSR12	W
00059F$_H$	PPG12 - Period setting register			W
0005A0$_H$	PPG12 - Duty cycle register		PDUT12	W
0005A1$_H$	PPG12 - Duty cycle register			W
0005A2$_H$	PPG12 - Control status register Low	PCNL12	PCN12	R/W
0005A3$_H$	PPG12 - Control status register High	PCNH12		R/W
0005A4$_H$	PPG13 - Timer register		PTMR13	R
0005A5$_H$	PPG13 - Timer register			R
0005A6$_H$	PPG13 - Period setting register		PCSR13	W
0005A7$_H$	PPG13 - Period setting register			W
0005A8$_H$	PPG13 - Duty cycle register		PDUT13	W
0005A9$_H$	PPG13 - Duty cycle register			W
0005AA$_H$	PPG13 - Control status register Low	PCNL13	PCN13	R/W
0005AB$_H$	PPG13 - Control status register High	PCNH13		R/W
0005AC$_H$	PPG14 - Timer register		PTMR14	R

I/O map MB96(F)35x (22 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0006E2H	External Bus - Area configuration register 1 Low	EACL1	EAC1	R/W
0006E3H	External Bus - Area configuration register 1 High	EACH1		R/W
0006E4H	External Bus - Area configuration register 2 Low	EACL2	EAC2	R/W
0006E5H	External Bus - Area configuration register 2 High	EACH2		R/W
0006E6H	External Bus - Area configuration register 3 Low	EACL3	EAC3	R/W
0006E7H	External Bus - Area configuration register 3 High	EACH3		R/W
0006E8H	External Bus - Area configuration register 4 Low	EACL4	EAC4	R/W
0006E9H	External Bus - Area configuration register 4 High	EACH4		R/W
0006EAH	External Bus - Area configuration register 5 Low	EACL5	EAC5	R/W
0006EBH	External Bus - Area configuration register 5 High	EACH5		R/W
0006ECH	External Bus - Area select register 2	EAS2		R/W
0006EDH	External Bus - Area select register 3	EAS3		R/W
0006EEH	External Bus - Area select register 4	EAS4		R/W
0006EFH	External Bus - Area select register 5	EAS5		R/W
0006F0H	External Bus - Mode register	EBM		R/W
0006F1H	External Bus - Clock and Function register	EBCF		R/W
0006F2H	External Bus - Address output enable register 0	EBAE0		R/W
0006F3H	External Bus - Address output enable register 1	EBAE1		R/W
0006F4H	External Bus - Address output enable register 2	EBAE2		R/W
0006F5H	External Bus - Control signal register	EBCS		R/W
0006F6H-0007FFH	Reserved			-
000800H	CAN1 - Control register Low	CTRLRL1	CTRLR1	R/W
000801H	CAN1 - Control register High (reserved)	CTRLRH1		R
000802H	CAN1 - Status register Low	STATRL1	STATR1	R/W
000803H	CAN1 - Status register High (reserved)	STATRH1		R
000804H	CAN1 - Error Counter Low (Transmit)	ERRCNTL1	ERRCNT1	R
000805H	CAN1 - Error Counter High (Receive)	ERRCNTH1		R
000806H	CAN1 - Bit Timing Register Low	BTRL1	BTR1	R/W
000807H	CAN1 - Bit Timing Register High	BTRH1		R/W

I/O map MB96(F)35x (27 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000926H-00093FH	Reserved			-
000940H	CAN2 - IF2 Command request register Low	IF2CREQL2	IF2CREQ2	R/W
000941H	CAN2 - IF2 Command request register High	IF2CREQH2		R/W
000942H	CAN2 - IF2 Command Mask register Low	IF2CMSKL2	IF2CMSK2	R/W
000943H	CAN2 - IF2 Command Mask register High (reserved)	IF2CMSKH2		R
000944H	CAN2 - IF2 Mask 1 Register Low	IF2MSK1L2	IF2MSK12	R/W
000945H	CAN2 - IF2 Mask 1 Register High	IF2MSK1H2		R/W
000946H	CAN2 - IF2 Mask 2 Register Low	IF2MSK2L2	IF2MSK22	R/W
000947H	CAN2 - IF2 Mask 2 Register High	IF2MSK2H2		R/W
000948H	CAN2 - IF2 Arbitration 1 Register Low	IF2ARB1L2	IF2ARB12	R/W
000949H	CAN2 - IF2 Arbitration 1 Register High	IF2ARB1H2		R/W
00094AH	CAN2 - IF2 Arbitration 2 Register Low	IF2ARB2L2	IF2ARB22	R/W
00094BH	CAN2 - IF2 Arbitration 2 Register High	IF2ARB2H2		R/W
00094CH	CAN2 - IF2 Message Control Register Low	IF2MCTRL2	IF2MCTR2	R/W
00094DH	CAN2 - IF2 Message Control Register High	IF2MCTRH2		R/W
00094EH	CAN2 - IF2 Data A1 Low	IF2DTA1L2	IF2DTA12	R/W
00094FH	CAN2 - IF2 Data A1 High	IF2DTA1H2		R/W
000950H	CAN2 - IF2 Data A2 Low	IF2DTA2L2	IF2DTA22	R/W
000951H	CAN2 - IF2 Data A2 High	IF2DTA2H2		R/W
000952H	CAN2 - IF2 Data B1 Low	IF2DTB1L2	IF2DTB12	R/W
000953H	CAN2 - IF2 Data B1 High	IF2DTB1H2		R/W
000954H	CAN2 - IF2 Data B2 Low	IF2DTB2L2	IF2DTB22	R/W
000955H	CAN2 - IF2 Data B2 High	IF2DTB2H2		R/W
000956H-00097FH	Reserved			-
000980H	CAN2 - Transmission Request 1 Register Low	TREQR1L2	TREQR12	R
000981H	CAN2 - Transmission Request 1 Register High	TREQR1H2		R
000982H	CAN2 - Transmission Request 2 Register Low	TREQR2L2	TREQR22	R
000983H	CAN2 - Transmission Request 2 Register High	TREQR2H2		R

I/O map MB96(F)35x (28 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000984H-00098FH	Reserved			-
000990H	CAN2 - New Data 1 Register Low	NEWDT1L2	NEWDT12	R
000991H	CAN2 - New Data 1 Register High	NEWDT1H2		R
000992H	CAN2 - New Data 2 Register Low	NEWDT2L2	NEWDT22	R
000993H	CAN2 - New Data 2 Register High	NEWDT2H2		R
000994H-00099FH	Reserved			-
0009A0H	CAN2 - Interrupt Pending 1 Register Low	INTPND1L2	INTPND12	R
0009A1H	CAN2 - Interrupt Pending 1 Register High	INTPND1H2		R
0009A2H	CAN2 - Interrupt Pending 2 Register Low	INTPND2L2	INTPND22	R
0009A3H	CAN2 - Interrupt Pending 2 Register High	INTPND2H2		R
0009A4H-0009AFH	Reserved			-
0009B0H	CAN2 - Message Valid 1 Register Low	MSGVAL1L2	MSGVAL12	R
0009B1H	CAN2 - Message Valid 1 Register High	MSGVAL1H2		R
0009B2H	CAN2 - Message Valid 2 Register Low	MSGVAL2L2	MSGVAL22	R
0009B3H	CAN2 - Message Valid 2 Register High	MSGVAL2H2		R
0009B4H-0009CDH	Reserved			-
0009CEH	CAN2 - Output enable register	COER2		R/W
0009CFH-000BFFH	Reserved			-

Note: Any write access to reserved addresses in the I/O map should not be performed. A read access to a reserved address results in reading ‘X’.
Registers of resources which are described in this table, but which are not supported by the device, should also be handled as “Reserved”.

■ HANDLING DEVICES

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Serial communication

1. Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

2. Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.

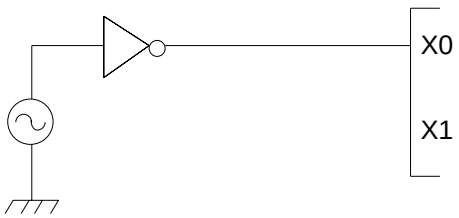
Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

3. External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

1. Single phase external clock

- When using a single phase external clock, X0 (X0A) pin must be driven and X1 (X1A) pin left open.



(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes*	I_{CCSRCL}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.08	0.2	mA	MB96F353/F355
			+125˚C	0.59	2.95		
			+25˚C	0.3	0.5	mA	MB96F356
			+125˚C	0.8	3.3		
		RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.05	0.15	mA	MB96F353/F355/ F356
			+125˚C	0.56	2.9		
	I_{CCSSUB}	Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25˚C	0.04	0.12	mA	MB96F353/F355/ F356
			+125˚C	0.54	2.9		
Power supply current in Timer modes*	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz (CLKRC and CLKSC stopped)	+25˚C	1.3	1.8	mA	MB96F353/F355
			+125˚C	1.9	4.8		
			+25˚C	1.5	2	mA	MB96F356
			+125˚C	2.1	5		
	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.11	0.2	mA	MB96F353/F355
			+125˚C	0.63	3		
			+25˚C	0.35	0.5	mA	MB96F356
			+125˚C	0.85	3.3		
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.08	0.15	mA	MB96F353/F355/ F356
			+125˚C	0.6	2.9		

External Bus timing

Note: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

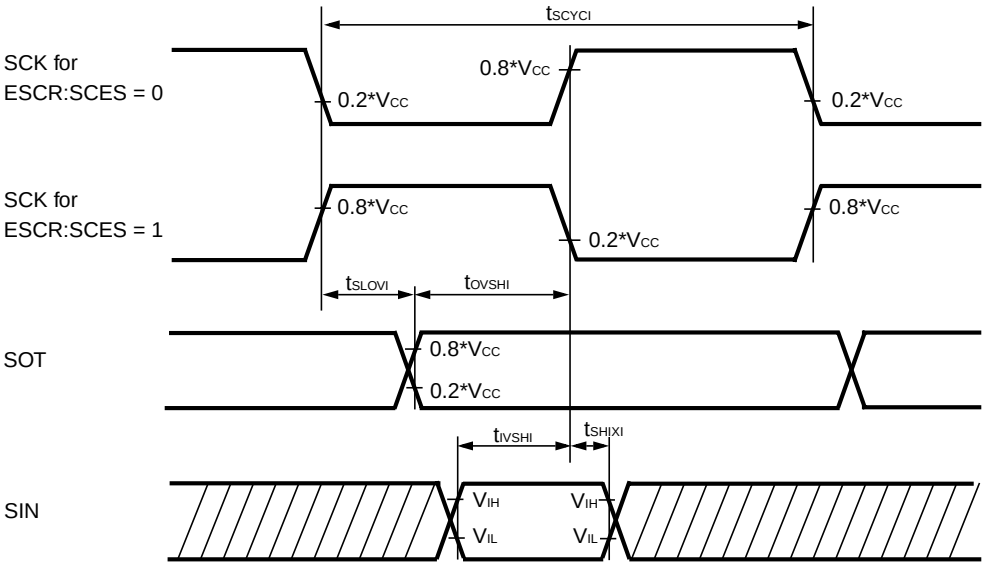
Basic Timing

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

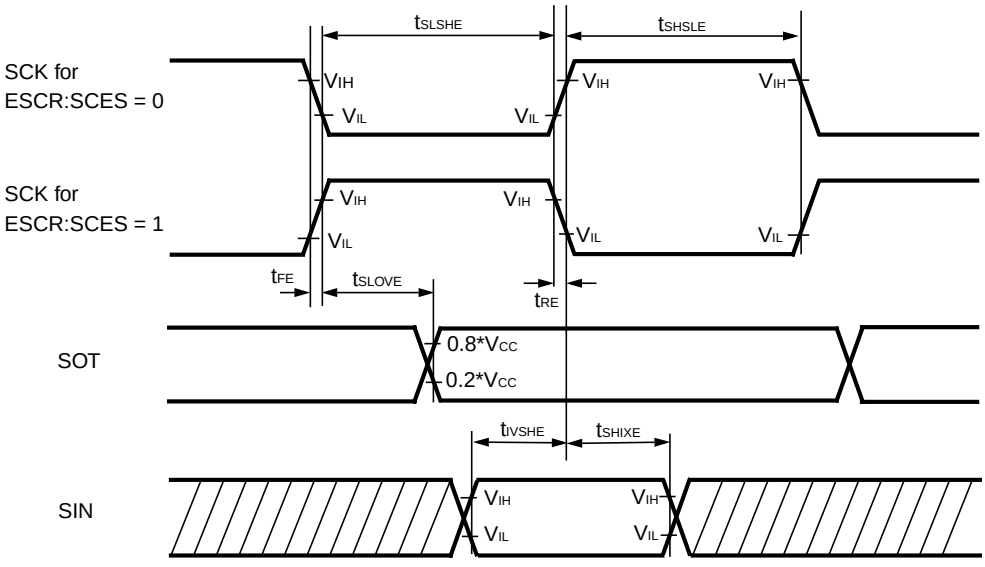
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	25	—	ns	
	t_{CHCL}			t_{CYC}/2-5	t_{CYC}/2+5		
	t_{CLCH}			t_{CYC}/2-5	t_{CYC}/2+5		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	—	-20	20	ns	
	t_{CHCBL}			-20	20		
	t_{CLCBH}			-20	20		
	t_{CLCBL}			-20	20		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-10	10	ns	
	t_{CHLL}			-10	10		
	t_{CLLH}			-10	10		
	t_{CLLL}			-10	10		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	—	-15	15	ns	
	t_{CLAV}			-15	15		
	t_{CLADV}	AD[15:0], ECLK	—	-15	15	ns	
	t_{CHADV}			-15	15		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX,WRHX, ECLK	—	-10	10	ns	
	t_{CHRWL}			-10	10		
	t_{CLRWH}			-10	10		
	t_{CLRWL}			-10	10		

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 20$	—	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 20$	—		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 20$	—	ns	
			EACL:ACE=1	$2t_{CYC} - 20$	—		
Valid address ⇒ Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	—	$3t_{CYC} - 60$	ns	w/o cycle extension
			EACL:ACE=1	—	$4t_{CYC} - 60$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0	—	$5t_{CYC}/2 - 60$	ns	w/o cycle extension
			EACL:ACE=1	—	$7t_{CYC}/2 - 60$		
RDX pulse width	t_{RLRH}	RDX	—	$3t_{CYC}/2 - 8$	—	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	—	—	$3t_{CYC}/2 - 55$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	—	0	—	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:16]	—	0	—	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 15$	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 15$	—		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:16], ECLK	—	$t_{CYC} - 20$	—	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 20$	—		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	—	$t_{CYC}/2 - 15$	—	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1	– 15	—		
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	$t_{CYC} - 55$	ns	



Internal Shift Clock Mode

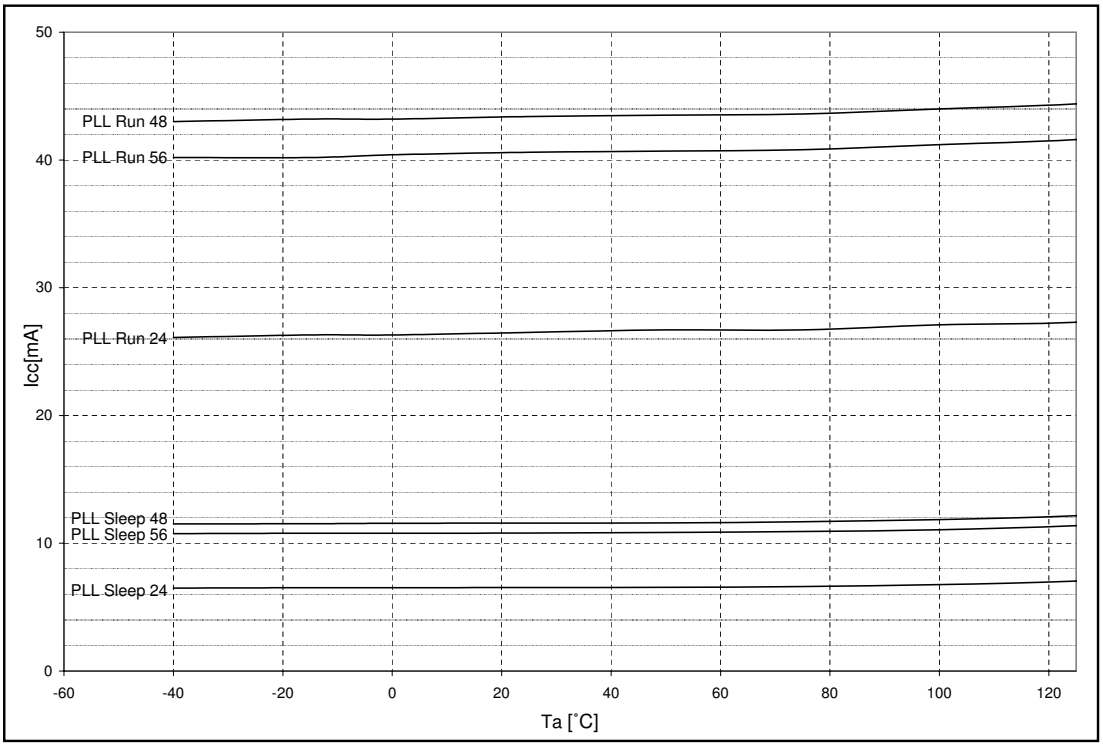


External Shift Clock Mode

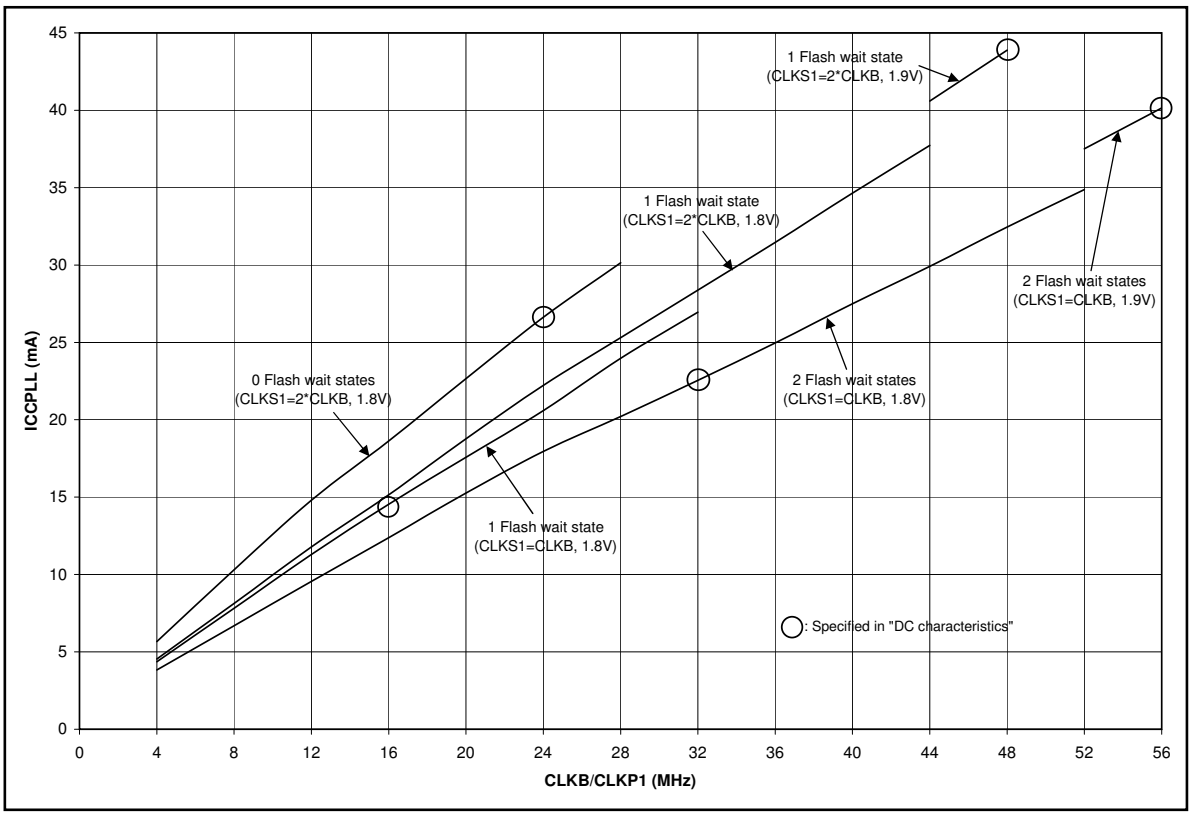
Mode name	Details
RC Sleep 2M	RC Sleep mode current I_{CCSRCH} with the following settings: • RC oscillator set to 2MHz (CKFCR:RCFS = 1) • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 2MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • PLL, Main oscillator and Sub oscillator stopped
RC Sleep 100k	RC Sleep mode current I_{CCSRCL} with the following settings: • RC oscillator set to 100kHz (CKFCR:RCFS = 0) • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 100kHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped
Sub Sleep	Sub Sleep mode current I_{CCSSUB} with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 32kHz • Regulator in Low Power Mode A (by hardware) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Main oscillator stopped
PLL Timer 48	PLL Timer mode current I_{CCTPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 48MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • RC oscillator and Sub oscillator stopped
Main Timer	Main Timer mode current $I_{CCTMAIN}$ with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 4MHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Sub oscillator stopped
RC Timer 2M	RC Timer mode current I_{CCTRCH} with the following settings: • RC oscillator set to 2MHz (CKFCR:RCFS = 1) • $f_{CLKS1} = f_{CLKS2}$ = 2MHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped
RC Timer 100k	RC Timer mode current I_{CCTRCL} with the following settings: • RC oscillator set to 100kHz (CKFCR:RCFS = 0) • $f_{CLKS1} = f_{CLKS2}$ = 100kHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped
Sub Timer	Sub Timer mode current I_{CCTSUB} with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 32kHz • Regulator in Low Power Mode A (by hardware) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Main oscillator stopped

Mode name	Details
Stop 1.8V	Stop mode current I_{CCH} with the following settings: • Regulator in Low Power Mode B (by hardware) • Core voltage at 1.8V (VRCR:LPMB[2:0] = 110_B)
Stop 1.2V	Stop mode current I_{CCH} with the following settings: • Regulator in Low Power Mode B (by hardware) • Core voltage at 1.2V (VRCR:LPMB[2:0] = 000_B)

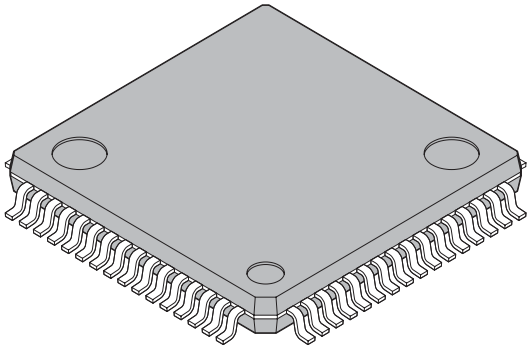
MB96F353/F355 PLL Run and Sleep mode currents



MB96F356 PLL Run mode currents

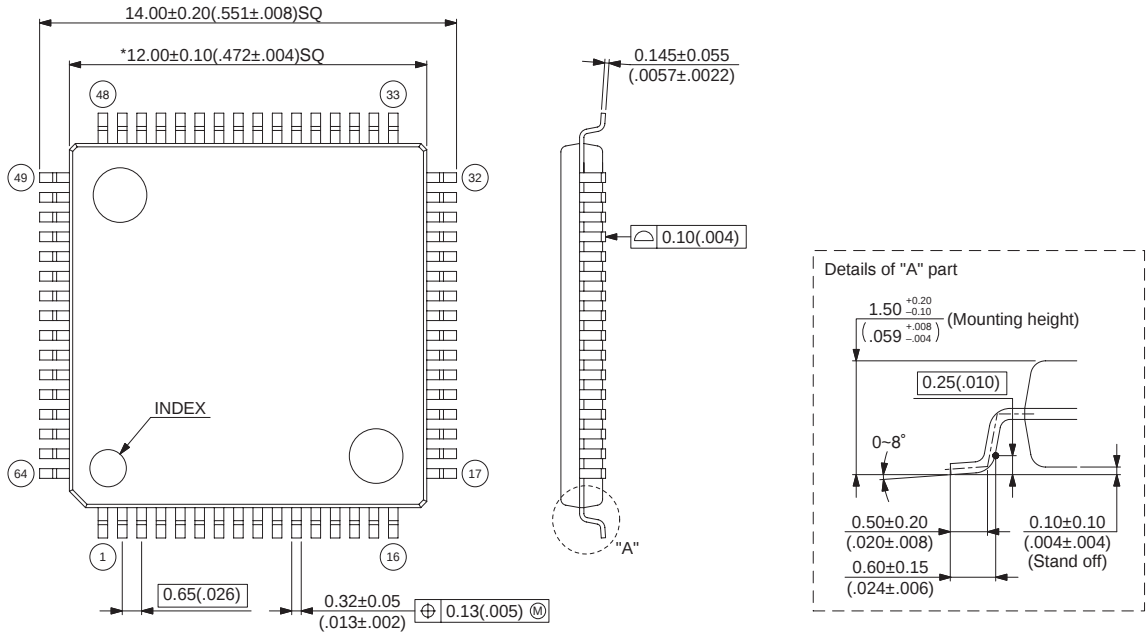


■ PACKAGE DIMENSION MB96(F)35x LQFP 64 - M23

64-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LFQFP64-12×12-0.65
(FPT-64P-M23)		

64-pin plastic LQFP
(FPT-64P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ ORDERING INFORMATION

MCU with CAN controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96F353RSB PMC-GSE2	Flash A (96KB)	No	No	64 pins Plastic LQFP (FPT-64P-M23)
MB96F353RWB PMC-GSE2		Yes		
MB96F353RSB PMC1-GSE2		No		64 pins Plastic LQFP (FPT-64P-M24)
MB96F353RWB PMC1-GSE2		Yes		
MB96F355RSB PMC-GSE2	Flash A (160KB)	No		64 pins Plastic LQFP (FPT-64P-M23)
MB96F355RWB PMC-GSE2		Yes		
MB96F355RSB PMC1-GSE2		No		64 pins Plastic LQFP (FPT-64P-M24)
MB96F355RWB PMC1-GSE2		Yes		
MB96F356YSB PMC-GSE2	Flash A (288KB)	No	Yes	64 pins Plastic LQFP (FPT-64P-M23)
MB96F356RSB PMC-GSE2			No	
MB96F356YWB PMC-GSE2		Yes	Yes	
MB96F356RWB PMC-GSE2			No	
MB96F356YSB PMC1-GSE2		No	Yes	64 pins Plastic LQFP (FPT-64P-M24)
MB96F356RSB PMC1-GSE2			No	
MB96F356YWB PMC1-GSE2		Yes	Yes	
MB96F356RWB PMC1-GSE2			No	
MB96V300BRB-ES (for evaluation)	Emulated by ext. RAM	Yes	No	416 pin Plastic BGA (BGA-416P-M02)

Revision	Date	Modification
7	2010-06-24	• AD converter I_{AIN} spec improved: 1uA valid up to 105deg, 1.2uA above 105deg • Low voltage detector: Detection levels of MB96F353/F355 updated • Note added that PLL phase jitter spec does not include jitter coming from Main clock • Note added in DC characteristics how to select driving strength of ports • I2C AC spec updated: tof, Cb and tSP spec added, wrong footnotes and Condition removed • I/O Circuit type: Note added for type “N” (slew rate control according to I2C spec) • Example characteristics updated, new figures added showing dependency of PLL Run mode current on frequency • Updated Power Supply current spec in Run/Sleep/Timer/Stop modes (new spec items in PLL Run/Sleep mode, small adjustment of most other values) • Package dimension: Added the following sentence under the figure: “Please confirm the latest Package dimension by following URL. http://edevice.fujitsu.com/package/en-search/” • AD converter: Impact of input pin capacitance and external capacitance added to formula for calculation of the sampling time • Added specification of RC clock stabilization time • Ordering information updated: MB96F353/F355**A -> MB96F353/F355**B, the device development is finished • Feature description I2C: ‘8-bit addressing’ corrected to ‘7-bit addressing’ • Feature description PPG: ‘Reload timer overflow as clock input’ corrected to ‘Reload timer underflow as clock input’ • ICCLVD specification updated, at 125deg typical value is 7uA and maximum value is 20uA • Company name updated on the cover page: Fujitsu Microelectronics Limited -> Fujitsu Semiconductor Limited

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