Infineon Technologies - MB96F355RSBPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

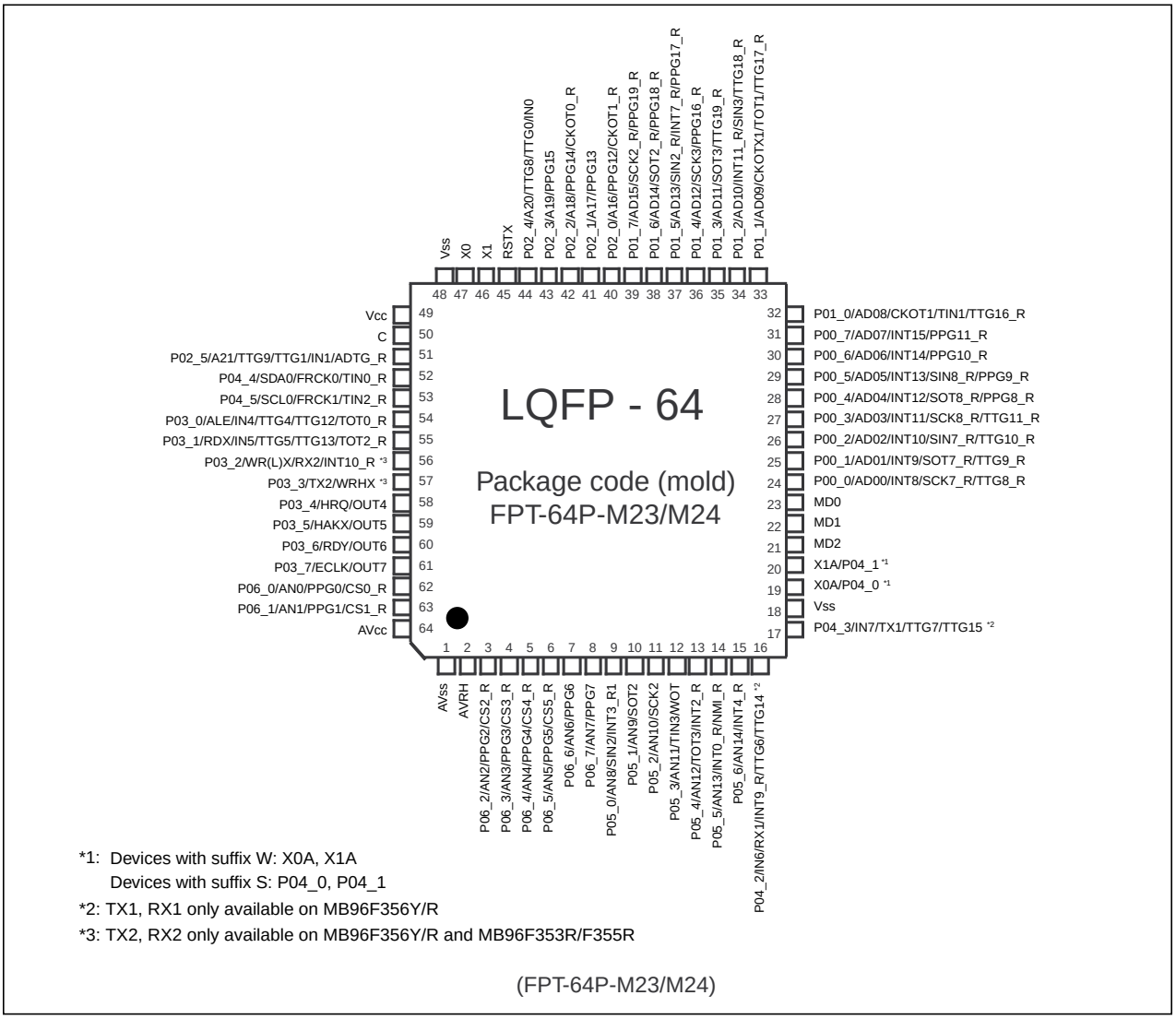
Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	51
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f355rsbpmc-gse2

Feature	Description
Flash Memory	• Supports automatic programming, Embedded Algorithm • Write/Erase/Erase-Suspend/Resume commands • A flag indicating completion of the algorithm • Number of erase cycles: 10,000 times • Data retention time: 20 years • Erase can be performed on each sector individually • Sector protection • Flash Security feature to protect the content of the Flash • Low voltage detection during Flash erase

Features	MB96V300B	MB96(F)35x
Real Time Clock	1	
I/O Ports	136	49 for part number with suffix "W", 51 for part number with suffix "S"
External bus interface	Yes	
Chip select	6 signals	
Clock output function	2 channels	
Low voltage reset	Yes	
On-chip RC-oscillator	Yes	

■ PIN ASSIGNMENTS

Pin assignment of MB96(F)35x



*1: Devices with suffix W: X0A, X1A
Devices with suffix S: P04_0, P04_1

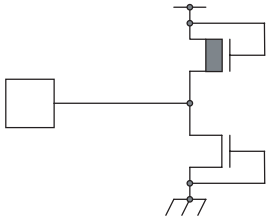
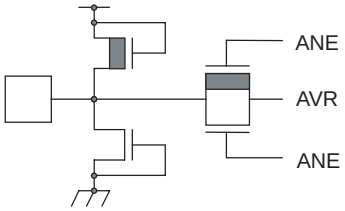
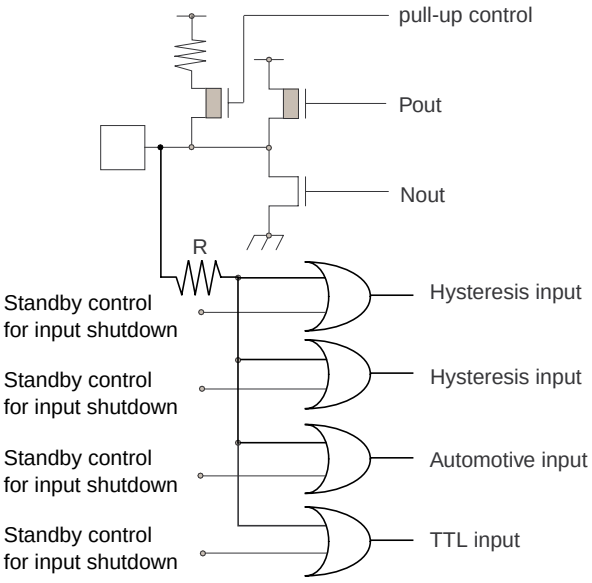
*2: TX1, RX1 only available on MB96F356Y/R

*3: TX2, RX2 only available on MB96F356Y/R and MB96F353R/F355R

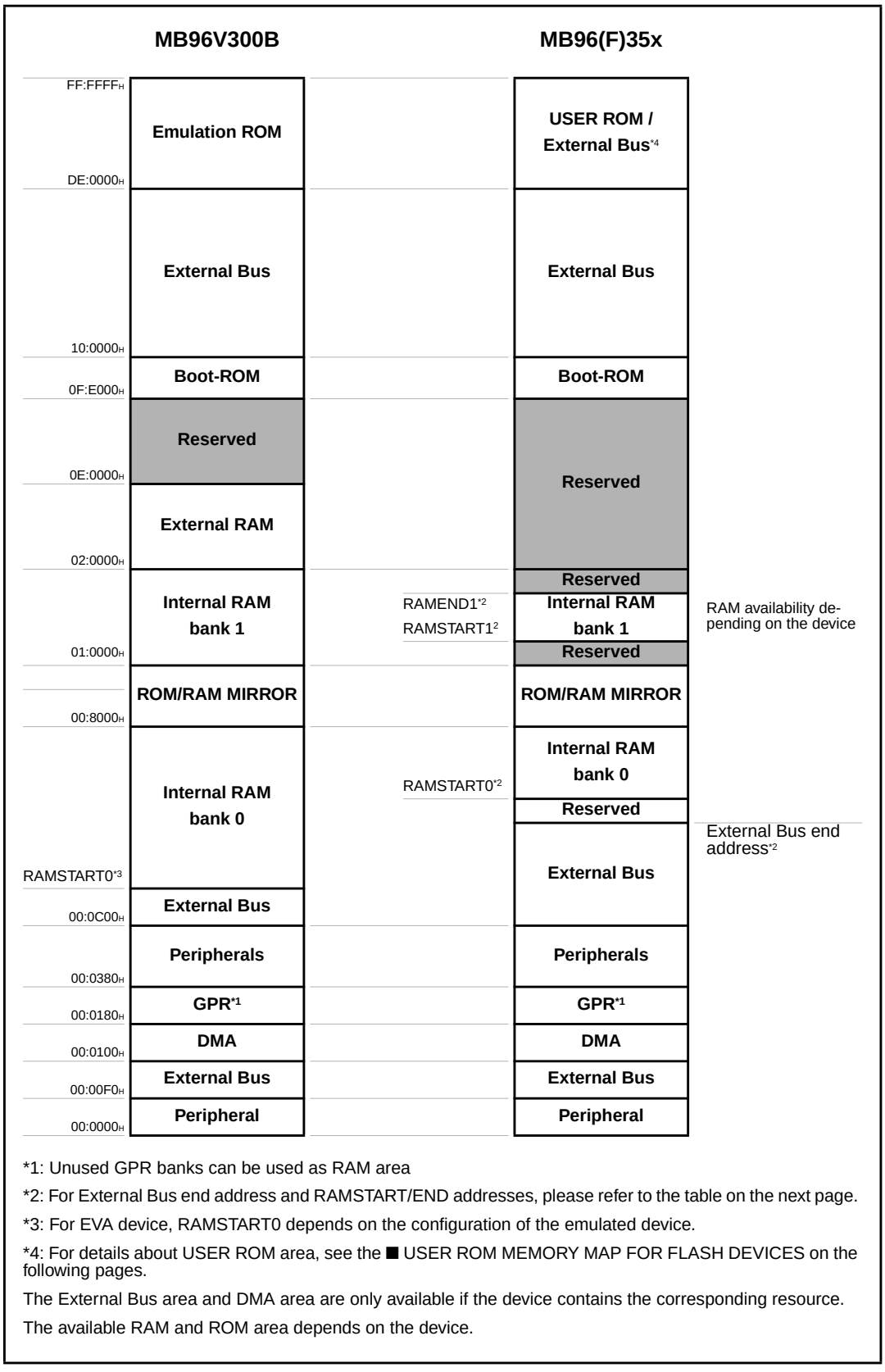
(FPT-64P-M23/M24)

Remark:

MB96(F)35x products are pin-compatible to F²MC-16LX family MB90350 series.

Type	Circuit	Remarks
F		• Power supply input protection circuit
G		• A/D converter ref+ (AVRH) power supply input pin with protection circuit • Flash devices do not have a protection circuit against VCC for pin AVRH
H		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx. Note: MB96F353/F355: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

■ MEMORY MAP



*1: Unused GPR banks can be used as RAM area

*2: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.

*3: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

*4: For details about USER ROM area, see the ■ USER ROM MEMORY MAP FOR FLASH DEVICES on the following pages.

The External Bus area and DMA area are only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

■ USER ROM MEMORY MAP FOR FLASH DEVICES

Alternative mode CPU address	Flash memory mode address	MB96F353 Flash size 96kByte	MB96F355 Flash size 160kByte	MB96F356 Flash size 288kByte	
FF:FFFF$_H$ FF:0000$_H$	3F:FFFF$_H$ 3F:0000$_H$	S39 - 64K	S39 - 64K	S39 - 64K	Flash A
FE:FFFF$_H$ FE:0000$_H$	3E:FFFF$_H$ 3E:0000$_H$	External bus	S38 - 64K	S38 - 64K	
FD:FFFF$_H$ FD:0000$_H$	3D:FFFF$_H$ 3D:0000$_H$		External bus	S37 - 64K	
FC:FFFF$_H$ FC:0000$_H$	3C:FFFF$_H$ 3C:0000$_H$			S36 - 64K	
FB:FFFF$_H$ FB:0000$_H$	3B:FFFF$_H$ 3B:0000$_H$			External bus	
FA:FFFF$_H$ FA:0000$_H$	3A:FFFF$_H$ 3A:0000$_H$				
F9:FFFF$_H$ F9:0000$_H$	39:FFFF$_H$ 39:0000$_H$				
F8:FFFF$_H$ F8:0000$_H$	38:FFFF$_H$ 38:0000$_H$				
F7:FFFF$_H$ F7:0000$_H$	37:FFFF$_H$ 37:0000$_H$				
F6:FFFF$_H$ F6:0000$_H$	36:FFFF$_H$ 36:0000$_H$				
F5:FFFF$_H$ F5:0000$_H$	35:FFFF$_H$ 35:0000$_H$				
F4:FFFF$_H$ F4:0000$_H$	34:FFFF$_H$ 34:0000$_H$				
F3:FFFF$_H$ F3:0000$_H$	33:FFFF$_H$ 33:0000$_H$				
F2:FFFF$_H$ F2:0000$_H$	32:FFFF$_H$ 32:0000$_H$				
F1:FFFF$_H$ F1:0000$_H$	31:FFFF$_H$ 31:0000$_H$				
F0:FFFF$_H$ F0:0000$_H$	30:FFFF$_H$ 30:0000$_H$				
E0:FFFF$_H$ E0:0000$_H$					
DF:FFFF$_H$ DF:8000$_H$		Reserved	Reserved	Reserved	
DF:7FFF$_H$ DF:6000$_H$	1F:7FFF$_H$ 1F:6000$_H$	SA3 - 8K	SA3 - 8K	SA3 - 8K	Flash A
DF:5FFF$_H$ DF:4000$_H$	1F:5FFF$_H$ 1F:4000$_H$	SA2 - 8K	SA2 - 8K	SA2 - 8K	
DF:3FFF$_H$ DF:2000$_H$	1F:3FFF$_H$ 1F:2000$_H$	SA1 - 8K	SA1 - 8K	SA1 - 8K	
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SA0 - 8K *1	SA0 - 8K *1	SA0 - 8K *1	
DE:FFFF$_H$ DE:0000$_H$		Reserved	Reserved	Reserved	

*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

I/O map MB96(F)35x (11 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003DB$_H$	Memory Patch function - Patch data 5 High	PFDH5		R/W
0003DC$_H$	Memory Patch function - Patch data 6 Low	PFDL6	PFD6	R/W
0003DD$_H$	Memory Patch function - Patch data 6 High	PFDH6		R/W
0003DE$_H$	Memory Patch function - Patch data 7 Low	PFDL7	PFD7	R/W
0003DF$_H$	Memory Patch function - Patch data 7 High	PFDH7		R/W
0003E0$_H$-0003F0$_H$	Reserved			-
0003F1$_H$	Memory Control Status Register A	MCSRA		R/W
0003F2$_H$	Memory Timing Configuration Register A Low	MTCRAL	MTCRA	R/W
0003F3$_H$	Memory Timing Configuration Register A High	MTCRAH		R/W
0003F4$_H$-0003F8$_H$	Reserved			-
0003F9$_H$	Flash Memory Write Control register 1	FMWC1		R/W
0003FA$_H$	Flash Memory Write Control register 2	FMWC2		R/W
0003FB$_H$	Flash Memory Write Control register 3	FMWC3		R/W
0003FC$_H$	Flash Memory Write Control register 4	FMWC4		R/W
0003FD$_H$	Flash Memory Write Control register 5	FMWC5		R/W
0003FE$_H$-0003FF$_H$	Reserved			-
000400$_H$	Standby Mode control register	SMCR		R/W
000401$_H$	Clock select register	CKSR		R/W
000402$_H$	Clock Stabilization select register	CKSSR		R/W
000403$_H$	Clock monitor register	CKMR		R
000404$_H$	Clock Frequency control register Low	CKFCRL	CKFCR	R/W
000405$_H$	Clock Frequency control register High	CKFCRH		R/W
000406$_H$	PLL Control register Low	PLLCRL	PLLCR	R/W
000407$_H$	PLL Control register High	PLLCRH		R/W
000408$_H$	RC clock timer control register	RCTCR		R/W
000409$_H$	Main clock timer control register	MCTCR		R/W
00040A$_H$	Sub clock timer control register	SCTCR		R/W

I/O map MB96(F)35x (13 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000446H	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447H	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448H	I/O Port P04 - Port Input Enable Register	PIER04		R/W
000449H	I/O Port P05 - Port Input Enable Register	PIER05		R/W
00044AH	I/O Port P06 - Port Input Enable Register	PIER06		R/W
00044BH-000457H	Reserved			-
000458H	I/O Port P00 - Port Input Level Register	PILR00		R/W
000459H	I/O Port P01 - Port Input Level Register	PILR01		R/W
00045AH	I/O Port P02 - Port Input Level Register	PILR02		R/W
00045BH	I/O Port P03 - Port Input Level Register	PILR03		R/W
00045CH	I/O Port P04 - Port Input Level Register	PILR04		R/W
00045DH	I/O Port P05 - Port Input Level Register	PILR05		R/W
00045EH	I/O Port P06 - Port Input Level Register	PILR06		R/W
00045FH-00046BH	Reserved			-
00046CH	I/O Port P00 - Extended Port Input Level Register	EPILR00		R/W
00046DH	I/O Port P01 - Extended Port Input Level Register	EPILR01		R/W
00046EH	I/O Port P02 - Extended Port Input Level Register	EPILR02		R/W
00046FH	I/O Port P03 - Extended Port Input Level Register	EPILR03		R/W
000470H	I/O Port P04 - Extended Port Input Level Register	EPILR04		R/W
000471H	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472H	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W
000473H-00047FH	Reserved			-
000480H	I/O Port P00 - Port Output Drive Register	PODR00		R/W
000481H	I/O Port P01 - Port Output Drive Register	PODR01		R/W
000482H	I/O Port P02 - Port Output Drive Register	PODR02		R/W
000483H	I/O Port P03 - Port Output Drive Register	PODR03		R/W
000484H	I/O Port P04 - Port Output Drive Register	PODR04		R/W
000485H	I/O Port P05 - Port Output Drive Register	PODR05		R/W

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes*	I_{CCSPLL}	PLL Sleep mode with CLKS1/2 = CLKP1 = 16MHz, CLKP2 = 8MHz (CLKRC and CLKSC stopped)	+25˚C	4	6	mA	MB96F353/F355/ F356
			+125˚C	4.7	9		
		PLL Sleep mode with CLKS1/2 = CLKP1 = 32MHz, CLKP2 = 16MHz (CLKRC and CLKSC stopped)	+25˚C	7	9.5	mA	MB96F353/F355/ F356
			+125˚C	8	12.5		
		PLL Sleep mode with CLKS1/2 = 48MHz, CLKP1/2 = 24MHz (CLKRC and CLKSC stopped)	+25˚C	7	9	mA	MB96F353/F355/ F356
			+125˚C	8	12		
		PLL Sleep mode with CLKS1/2 = CLKP1= 56MHz, CLKP2 = 28MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	11	14.5	mA	MB96F353/F355/ F356
			+125˚C	12	17.5		
		PLL Sleep mode with CLKS1/2 = 96MHz, CLKP1= 48MHz, CLKP2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	12	15	mA	MB96F353/F355/ F356
			+125˚C	13	18		
	$I_{CCSMAIN}$	Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	+25˚C	1	1.3	mA	MB96F353/F355
			+125˚C	1.6	4.1		
			+25˚C	1.3	1.8	mA	MB96F356
			+125˚C	1.9	4.6		
	I_{CCSRCH}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 2MHz (CLKMC, CLKPLL and CLKSC stopped)	+25˚C	0.55	1.1	mA	MB96F353/F355
			+125˚C	1.15	3.9		
			+25˚C	0.8	1.4	mA	MB96F356
			+125˚C	1.4	4.2		

External Bus timing

Note: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

Basic Timing

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

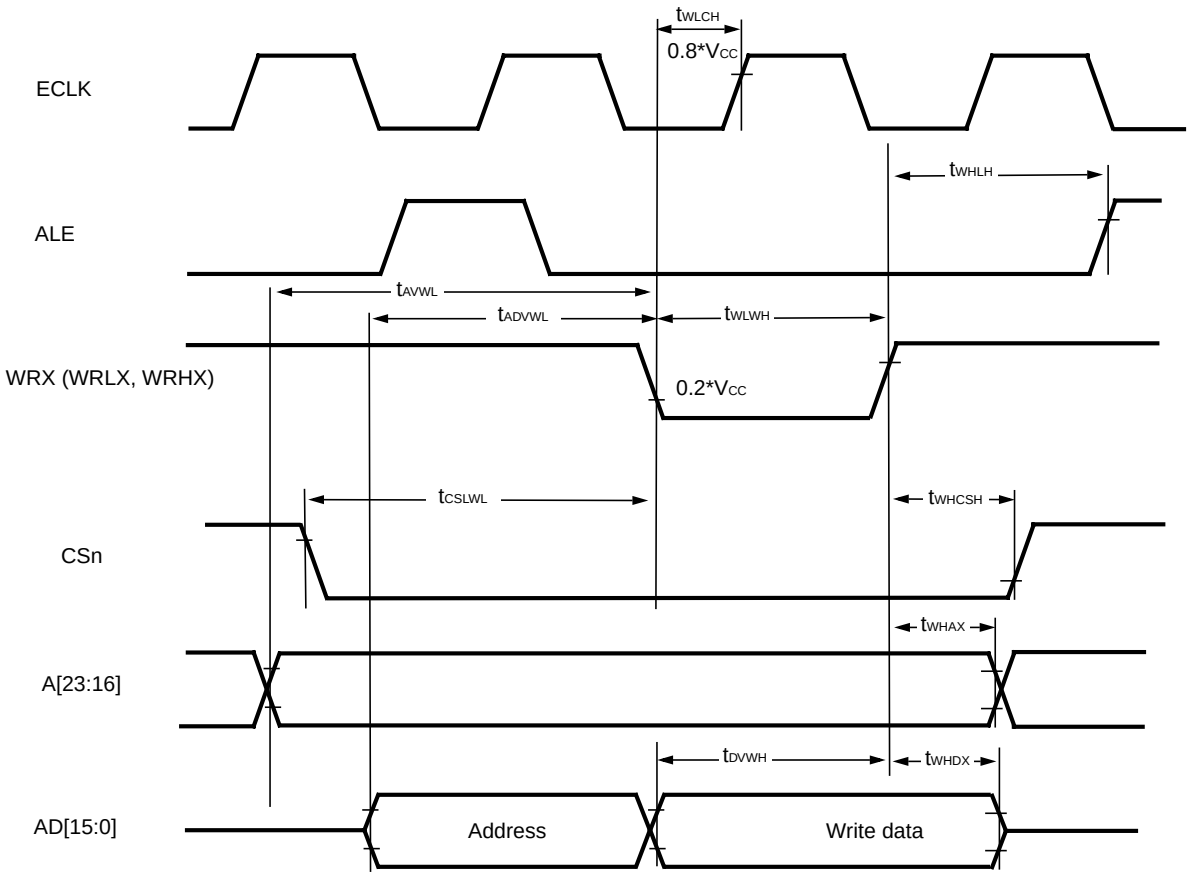
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	25	—	ns	
	t_{CHCL}			t_{CYC}/2-5	t_{CYC}/2+5		
	t_{CLCH}			t_{CYC}/2-5	t_{CYC}/2+5		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	—	-20	20	ns	
	t_{CHCBL}			-20	20		
	t_{CLCBH}			-20	20		
	t_{CLCBL}			-20	20		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-10	10	ns	
	t_{CHLL}			-10	10		
	t_{CLLH}			-10	10		
	t_{CLLL}			-10	10		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	—	-15	15	ns	
	t_{CLAV}			-15	15		
	t_{CLADV}	AD[15:0], ECLK	—	-15	15	ns	
	t_{CHADV}			-15	15		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX,WRHX, ECLK	—	-10	10	ns	
	t_{CHRWL}			-10	10		
	t_{CLRWH}			-10	10		
	t_{CLRWL}			-10	10		

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

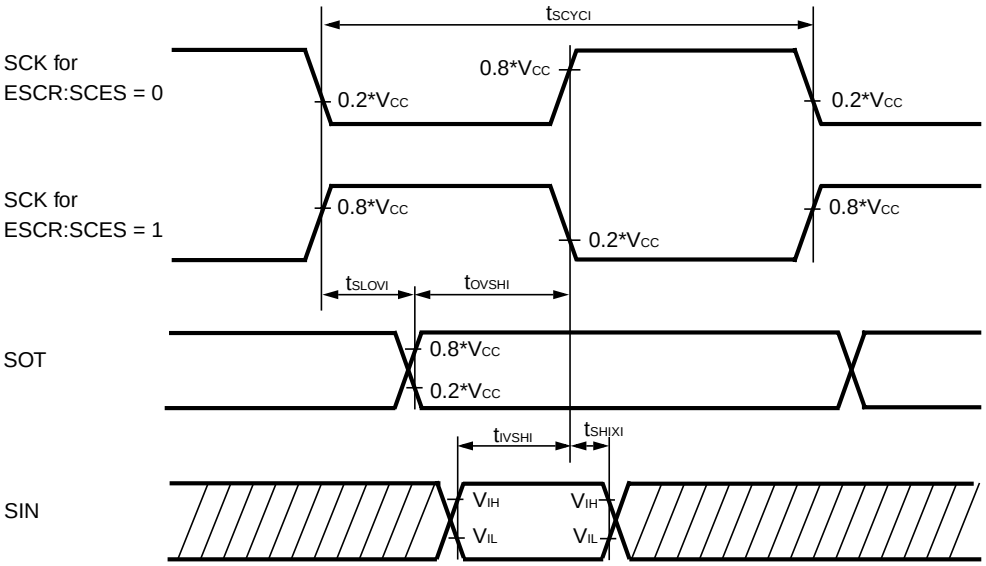
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	30	—	ns	
	t_{CHCL}			t_{CYC}/2-8	t_{CYC}/2+8		
	t_{CLCH}			t_{CYC}/2-8	t_{CYC}/2+8		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	—	-25	25	ns	
	t_{CHCBL}			-25	25		
	t_{CLCBH}			-25	25		
	t_{CLCBL}			-25	25		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-15	15	ns	
	t_{CHLL}			-15	15		
	t_{CLLH}			-15	15		
	t_{CLLL}			-15	15		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	—	-20	20	ns	
	t_{CLAV}			-20	20		
	t_{CLADV}	AD[15:0], ECLK	—	-20	20	ns	
	t_{CHADV}			-20	20		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX, WRHX, ECLK	—	-15	15	ns	
	t_{CHRWL}			-15	15		
	t_{CLRWH}			-15	15		
	t_{CLRWL}			-15	15		

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

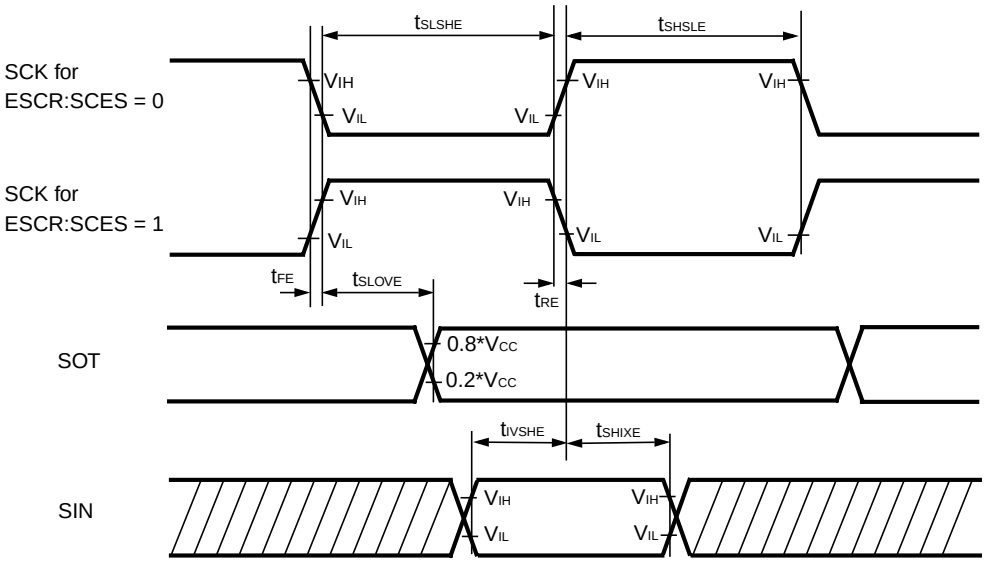
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
WRX ↑ ⇒ ALE ↑ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC}$ – 15	—	ns	
			other EBM:ACE and EACL:STS setting	t_{CYC} – 15	—		
WRX ↓ ⇒ ECLK ↑ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	—	$t_{CYC}/2$ – 15	—	ns	
CSn ⇒ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	—	$3t_{CYC}/2$ – 20	ns	
			EACL:ACE=1	—	$5t_{CYC}/2$ – 20		
WRX ⇒ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	—	$t_{CYC}/2$ – 20	—	ns	



Refer to the Hardware Manual for detailed Timing Charts



Internal Shift Clock Mode



External Shift Clock Mode

I²C Timing

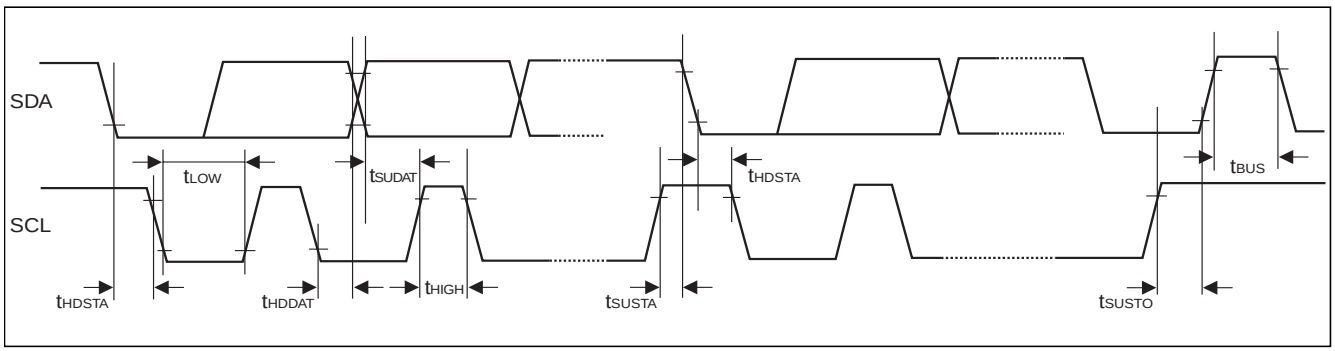
(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} =0V)

Parameter	Symbol	Standard-mode		Fast-mode*1		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t_{HDSTA}	4.0	—	0.6	—	µs
“L” width of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
“H” width of the SCL clock	t_{HIGH}	4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL↑→SDA↓	t_{SUSTA}	4.7	—	0.6	—	µs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}	0	3.45	0	0.9	µs
Data set-up time SDA↓↑→SCL↑	t_{SUDAT}	250	—	100	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t_{SUSTO}	4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUS}	4.7	—	1.3	—	µs
Output fall time from 0.7*Vcc to 0.3*Vcc with a bus capacitance from 10 pF to 400 pF	t_{of}	20 + 0.1*C_b *2	250	20 + 0.1*C_b *2	250	ns
Capacitive load for each bus line	C_b	—	400	—	400	pF
Pulse width of spikes which will be suppressed by input noise filter	t_{SP}	n/a	n/a	0	1*t_{CLKP1}*3	ns

*1 : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.

*2 : C_b = capacitance of one bus line in pF.

*3 : t_{CLKP1} is the cycle time of the peripheral clock CLKP1.

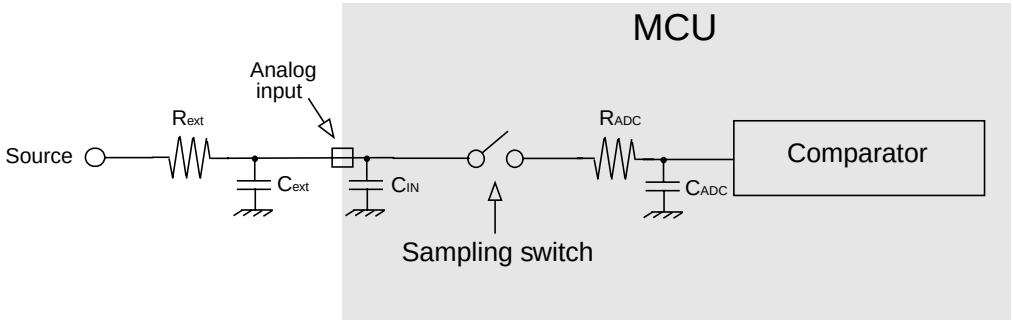


- V_{OH} = 0.7 * V_{CC}
- V_{OL} = 0.3 * V_{CC}
- CMOS Hysteresis 0.7/0.3 input selected

Accuracy and setting of the A/D Converter sampling time

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time depends on the external driving impedance R_{ext}, the board capacitance of the A/D converter input pin C_{ext} and the AV_{cc} voltage level. The following replacement model can be used for the calculation:



R_{ext}: external driving impedance
C_{ext}: capacitance of PCB at A/D converter input
C_{IN}: capacitance of MCU input pin: 15pF (max)
R_{ADC}: resistance within MCU: 2.6kΩ (max) for $4.5V \le AV_{cc} \le 5.5V$
12kΩ (max) for $3.0V \le AV_{cc} < 4.5V$
C_{ADC}: sampling capacitance within MCU: 10pF (max)

The sampling time should be set to minimum “7τ“. The following approximation formula for the replacement model above can be used:

$$T_{samp}\ [min] = 7 \times (R_{ext} \times (C_{ext} + C_{IN}) + (R_{ext} + R_{ADC}) \times C_{ADC})$$

- Do not select a sampling time below the absolute minimum permitted value (0.5µs for $4.5V \le AV_{cc} \le 5.5V$; 1.2 µs for $3.0V \le AV_{cc} < 4.5V$).
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin. In this case the internal sampling capacitance C_{ADC} will be charged out of this external capacitance.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current I_{IL} (static current before the sampling switch) or the analog input leakage current I_{AIN} (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current I_{IL} cannot be compensated by an external capacitor.
- The accuracy gets worse as |AVRH - AVRL| becomes smaller.

■ EXAMPLE CHARACTERISTICS

1. Temperature dependency of power supply currents

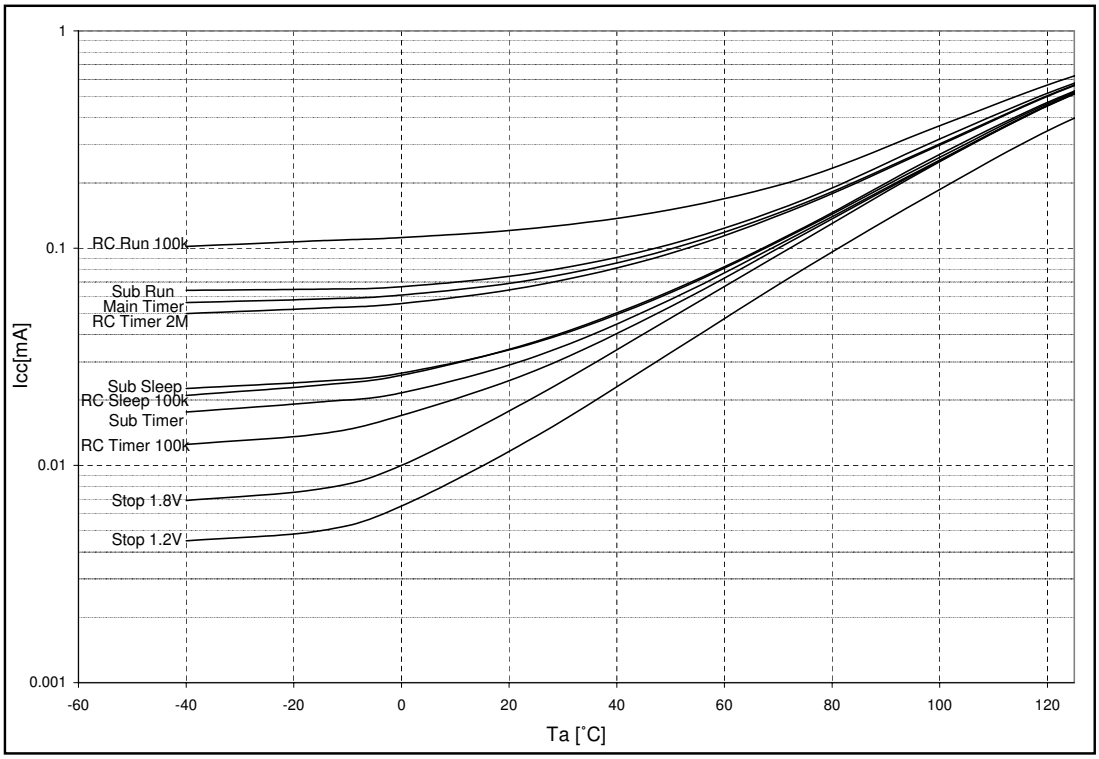
The following diagrams show the current consumption of samples with typical wafer process parameters in different operation modes.

Common condition for all operation modes:
- V_{CC} = AV_{CC} = 5.0V
- Main clock = 4MHz external clock
- Sub clock = 32kHz external clock

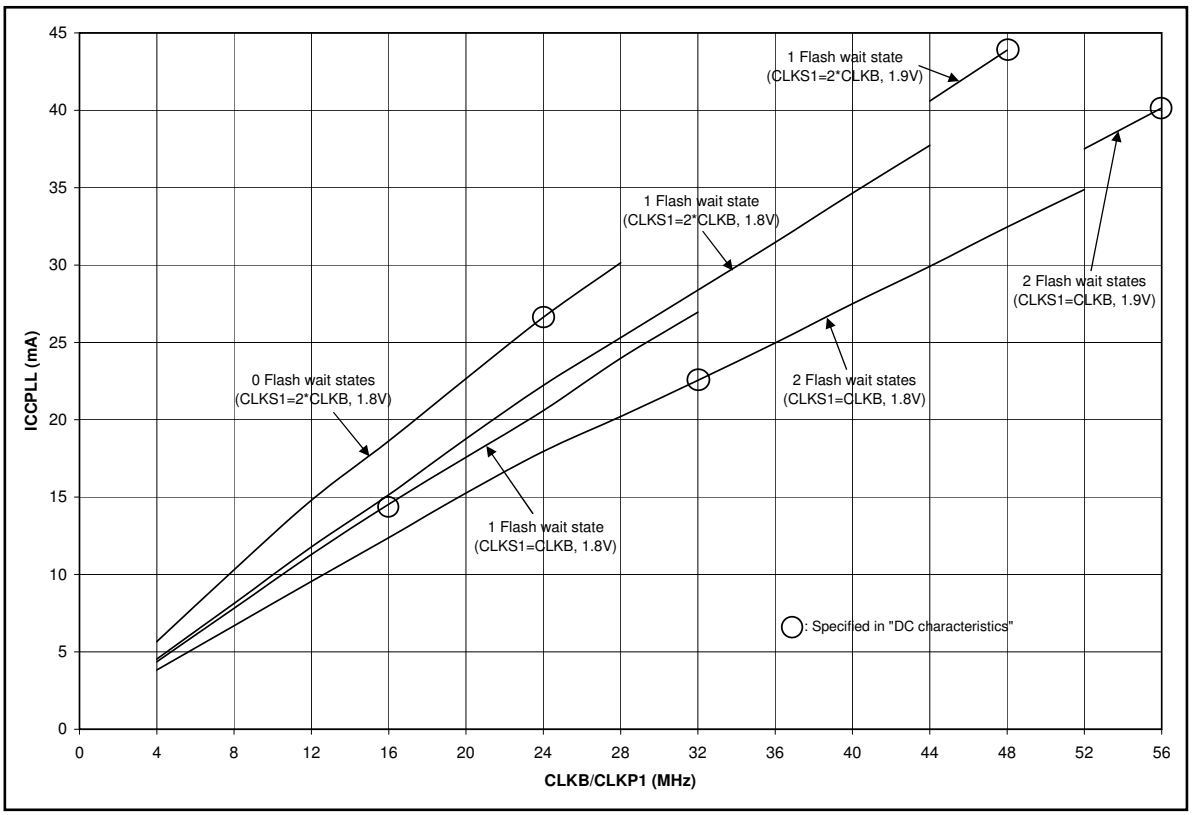
Operation mode details:

Mode name	Details
PLL Run 56	PLL Run mode current I_{CCPLL} with the following settings: • f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = 56MHz • f_{CLKP2} = 28MHz • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • 2 Flash/ROM wait states (MTCRA=$233A_H$) • RC oscillator and Sub oscillator stopped
PLL Run 48	PLL Run mode current I_{CCPLL} with the following settings: • f_{CLKS1} = f_{CLKS2} = 96MHz • f_{CLKB} = f_{CLKP1} = 48MHz • f_{CLKP2} = 24MHz • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • 1 Flash/ROM wait states (MTCRA=$6B09_H$) • RC oscillator and Sub oscillator stopped
PLL Run 24	PLL Run mode current I_{CCPLL} with the following settings: • f_{CLKS1} = f_{CLKS2} = 48MHz • f_{CLKB} = f_{CLKP1} = f_{CLKP2} = 24MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • 0 Flash/ROM wait states (MTCRA=2208_H) • RC oscillator and Sub oscillator stopped
Main Run	Main Run mode current I_{CCMAIN} with the following settings: • f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2} = 4MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • 1 Flash/ROM wait states (MTCRA=0239_H) • PLL, RC oscillator and Sub oscillator stopped

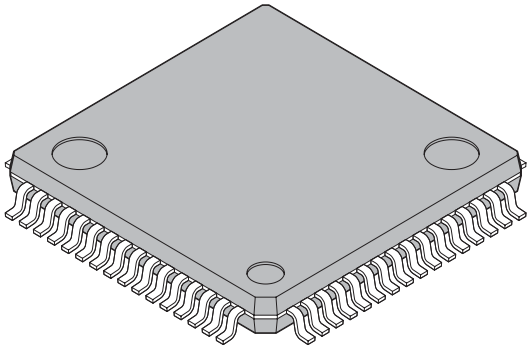
MB96F356 Low power mode currents



MB96F356 PLL Run mode currents

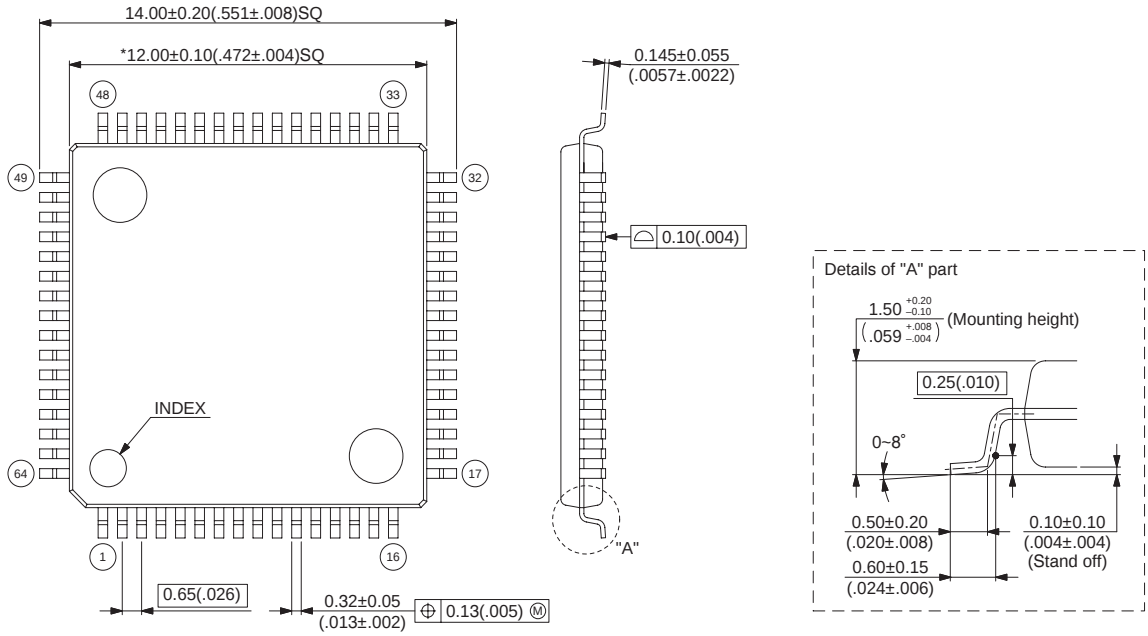


■ PACKAGE DIMENSION MB96(F)35x LQFP 64 - M23

64-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LFQFP64-12×12-0.65
(FPT-64P-M23)		

64-pin plastic LQFP
(FPT-64P-M23)

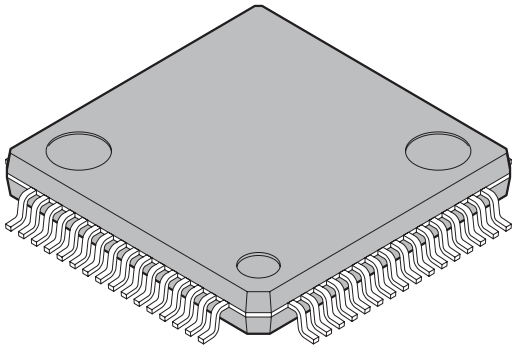
Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

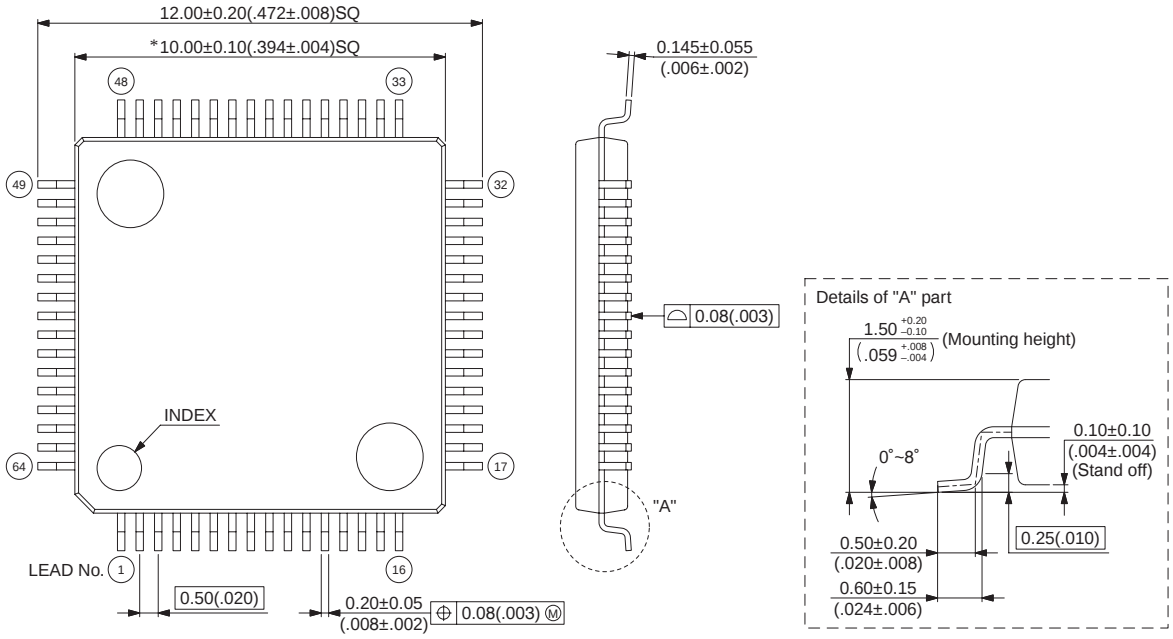
Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ PACKAGE DIMENSION MB96(F)35x LQFP 64 - M24

64-pin plastic LQFP  (FPT-64P-M24)	Lead pitch	0.50 mm
	Package width × package length	10.0 × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
	Code (Reference)	P-LFQFP64-10×10-0.50

64-pin plastic LQFP
(FPT-64P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/