Infineon Technologies - MB96F355RSBPMC1-GSE2 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	51
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f355rsbpmc1-gse2

■ PRODUCT LINEUP

Features		MB96V300B	MB96(F)35x
Product type		Evaluation sample	Flash product: MB96F35x Mask ROM product: MB9635x
Product options			
YS		NA	Low voltage reset persistently on / Single clock devices
RS			Low voltage reset can be disabled / Single clock devices
YW			Low voltage reset persistently on / Dual clock devices
RW			Low voltage reset can be disabled / Dual clock devices
AS			No CAN / Low voltage reset can be disabled / Single clock devices
AW			No CAN / Low voltage reset can be disabled / Dual clock devices
Flash/ ROM	RAM		
96KB	8KB	ROM/Flash memory emulation by external RAM, 92KB internal RAM	MB96F353R, MB96F353A
160KB	8KB		MB96F355R, MB96F355A
288KB	12KB		MB96F356Y, MB96F356R, MB96F356A
Package		BGA416	FPT-64P-M23/24
DMA		16 channels	4 channels
USART		10 channels	4 channels
I2C		2 channels	1 channel
A/D Converter		40 channels	15 channels
A/D Converter Reference Voltage switch		yes	No
16-bit Reload Timer		6 channels + 1 channel (for PPG)	4 channels + 1 channel (for PPG)
16-bit Free-Running Timer		4 channels	4 channels (2 channels with external clock input pin)
16-bit Output Compare		12 channels	4 channels
16-bit Input Capture		12 channels	6 channels (plus 2 channels for LIN USART)
16-bit Programmable Pulse Generator		20 channels	20 channels
CAN Interface		5 channels	MB96F35xA: no MB96F353R/F355R: 1 channel MB96F356Y/R: 2 channels
External Interrupts		16 channels	13 channels
Non-Maskable Interrupt		1 channel	

Features	MB96V300B	MB96(F)35x
Real Time Clock	1	
I/O Ports	136	49 for part number with suffix "W", 51 for part number with suffix "S"
External bus interface	Yes	
Chip select	6 signals	
Clock output function	2 channels	
Low voltage reset	Yes	
On-chip RC-oscillator	Yes	

■ PIN CIRCUIT TYPE

Pin circuit types

FPT-64P-M23/24	
Pin no.	Circuit type *1
1	Supply
2	G
3 to 15	I
16,17	H
18	Supply
19,20	B *2
19,20	H *3
21 to 23	C
24 to 44	H
45	E
46,47	A
48,49	Supply
50	F
51	H
52,53	N
54 to 61	H
62,63	I
64	Supply

*1: Please refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types
*2: Devices with suffix ”W”
*3: Devices without suffix ”W”

I/O map MB96(F)35x (5 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000083H	PPG1 - Period setting register			W
000084H	PPG1 - Duty cycle register		PDUT1	W
000085H	PPG1 - Duty cycle register			W
000086H	PPG1 - Control status register Low	PCNL1	PCN1	R/W
000087H	PPG1 - Control status register High	PCNH1		R/W
000088H	PPG2 - Timer register		PTMR2	R
000089H	PPG2 - Timer register			R
00008AH	PPG2 - Period setting register		PCSR2	W
00008BH	PPG2 - Period setting register			W
00008CH	PPG2 - Duty cycle register		PDUT2	W
00008DH	PPG2 - Duty cycle register			W
00008EH	PPG2 - Control status register Low	PCNL2	PCN2	R/W
00008FH	PPG2 - Control status register High	PCNH2		R/W
000090H	PPG3 - Timer register		PTMR3	R
000091H	PPG3 - Timer register			R
000092H	PPG3 - Period setting register		PCSR3	W
000093H	PPG3 - Period setting register			W
000094H	PPG3 - Duty cycle register		PDUT3	W
000095H	PPG3 - Duty cycle register			W
000096H	PPG3 - Control status register Low	PCNL3	PCN3	R/W
000097H	PPG3 - Control status register High	PCNH3		R/W
000098H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	R/W
000099H	PPG7-PPG4 - General Control register 1 High	GCN1H1		R/W
00009AH	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	R/W
00009BH	PPG7-PPG4 - General Control register 2 High	GCN2H1		R/W
00009CH	PPG4 - Timer register		PTMR4	R
00009DH	PPG4 - Timer register			R
00009EH	PPG4 - Period setting register		PCSR4	W
00009FH	PPG4 - Period setting register			W
0000A0H	PPG4 - Duty cycle register		PDUT4	W

I/O map MB96(F)35x (8 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00010D$_H$	DMA1 - I/O register address pointer high byte	IOAH1		R/W
00010E$_H$	DMA1 - Data counter low byte	DCTL1	DCT1	R/W
00010F$_H$	DMA1 - Data counter high byte	DCTH1		R/W
000110$_H$	DMA2 - Buffer address pointer low byte	BAPL2		R/W
000111$_H$	DMA2 - Buffer address pointer middle byte	BAPM2		R/W
000112$_H$	DMA2 - Buffer address pointer high byte	BAPH2		R/W
000113$_H$	DMA2 - DMA control register	DMACS2		R/W
000114$_H$	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W
000115$_H$	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116$_H$	DMA2 - Data counter low byte	DCTL2	DCT2	R/W
000117$_H$	DMA2 - Data counter high byte	DCTH2		R/W
000118$_H$	DMA3 - Buffer address pointer low byte	BAPL3		R/W
000119$_H$	DMA3 - Buffer address pointer middle byte	BAPM3		R/W
00011A$_H$	DMA3 - Buffer address pointer high byte	BAPH3		R/W
00011B$_H$	DMA3 - DMA control register	DMACS3		R/W
00011C$_H$	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
00011D$_H$	DMA3 - I/O register address pointer high byte	IOAH3		R/W
00011E$_H$	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
00011F$_H$	DMA3 - Data counter high byte	DCTH3		R/W
000120$_H$-00017F$_H$	Reserved			-
000180$_H$-00037F$_H$	CPU - General Purpose registers (RAM access)	GPR_RAM		R/W
000380$_H$	DMA0 - Interrupt select	DISEL0		R/W
000381$_H$	DMA1 - Interrupt select	DISEL1		R/W
000382$_H$	DMA2 - Interrupt select	DISEL2		R/W
000383$_H$	DMA3 - Interrupt select	DISEL3		R/W
000384$_H$-00038F$_H$	Reserved			-
000390$_H$	DMA - Status register low byte	DSRL	DSR	R/W
000391$_H$	DMA - Status register high byte	DSRH		R/W

I/O map MB96(F)35x (10 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003BD$_H$	Memory Patch function - Patch address 1 high	PFAH1		R/W
0003BE$_H$	Memory Patch function - Patch address 2 low	PFAL2		R/W
0003BF$_H$	Memory Patch function - Patch address 2 middle	PFAM2		R/W
0003C0$_H$	Memory Patch function - Patch address 2 high	PFAH2		R/W
0003C1$_H$	Memory Patch function - Patch address 3 low	PFAL3		R/W
0003C2$_H$	Memory Patch function - Patch address 3 middle	PFAM3		R/W
0003C3$_H$	Memory Patch function - Patch address 3 high	PFAH3		R/W
0003C4$_H$	Memory Patch function - Patch address 4 low	PFAL4		R/W
0003C5$_H$	Memory Patch function - Patch address 4 middle	PFAM4		R/W
0003C6$_H$	Memory Patch function - Patch address 4 high	PFAH4		R/W
0003C7$_H$	Memory Patch function - Patch address 5 low	PFAL5		R/W
0003C8$_H$	Memory Patch function - Patch address 5 middle	PFAM5		R/W
0003C9$_H$	Memory Patch function - Patch address 5 high	PFAH5		R/W
0003CA$_H$	Memory Patch function - Patch address 6 low	PFAL6		R/W
0003CB$_H$	Memory Patch function - Patch address 6 middle	PFAM6		R/W
0003CC$_H$	Memory Patch function - Patch address 6 high	PFAH6		R/W
0003CD$_H$	Memory Patch function - Patch address 7 low	PFAL7		R/W
0003CE$_H$	Memory Patch function - Patch address 7 middle	PFAM7		R/W
0003CF$_H$	Memory Patch function - Patch address 7 high	PFAH7		R/W
0003D0$_H$	Memory Patch function - Patch data 0 Low	PFDL0	PFD0	R/W
0003D1$_H$	Memory Patch function - Patch data 0 High	PFDH0		R/W
0003D2$_H$	Memory Patch function - Patch data 1 Low	PFDL1	PFD1	R/W
0003D3$_H$	Memory Patch function - Patch data 1 High	PFDH1		R/W
0003D4$_H$	Memory Patch function - Patch data 2 Low	PFDL2	PFD2	R/W
0003D5$_H$	Memory Patch function - Patch data 2 High	PFDH2		R/W
0003D6$_H$	Memory Patch function - Patch data 3 Low	PFDL3	PFD3	R/W
0003D7$_H$	Memory Patch function - Patch data 3 High	PFDH3		R/W
0003D8$_H$	Memory Patch function - Patch data 4 Low	PFDL4	PFD4	R/W
0003D9$_H$	Memory Patch function - Patch data 4 High	PFDH4		R/W
0003DA$_H$	Memory Patch function - Patch data 5 Low	PFDL5	PFD5	R/W

Interrupt vector table MB96(F)35x (3 of 3)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
67	$2F0_H$				Reserved
68	$2EC_H$	ICU9	Yes	68	Input Capture Unit 9
69	$2E8_H$	ICU10	Yes	69	Input Capture Unit 10
70	$2E4_H$				Reserved
71	$2E0_H$	OCU4	Yes	71	Output Compare Unit 4
72	$2DC_H$	OCU5	Yes	72	Output Compare Unit 5
73	$2D8_H$	OCU6	Yes	73	Output Compare Unit 6
74	$2D4_H$	OCU7	Yes	74	Output Compare Unit 7
75	$2D0_H$				Reserved
76	$2CC_H$				Reserved
77	$2C8_H$	FRT0	Yes	77	Free Running Timer 0
78	$2C4_H$	FRT1	Yes	78	Free Running Timer 1
79	$2C0_H$	FRT2	Yes	79	Free Running Timer 2
80	$2BC_H$	FRT3	Yes	80	Free Running Timer 3
81	$2B8_H$	RTC0	No	81	Real Timer Clock
82	$2B4_H$	CAL0	No	82	Clock Calibration Unit
83	$2B0_H$	IIC0	Yes	83	I2C interface
84	$2AC_H$	ADC0	Yes	84	A/D Converter
85	$2A8_H$	LINR2	Yes	85	LIN USART 2 RX
86	$2A4_H$	LINT2	Yes	86	LIN USART 2 TX
87	$2A0_H$	LINR3	Yes	87	LIN USART 3 RX
88	$29C_H$	LINT3	Yes	88	LIN USART 3 TX
89	298_H	LINR7	Yes	89	LIN USART 7 RX
90	294_H	LINT7	Yes	90	LIN USART 7 TX
91	290_H	LINR8	Yes	91	LIN USART 8 RX
92	$28C_H$	LINT8	Yes	92	LIN USART 8 TX
93	288_H	FLASH_A	No	93	Flash memory A (only Flash devices)

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes*	I_{CCMAIN}	Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz 1 Flash/ROM wait state (CLKPLL, CLKSC and CLKRC stopped)	+25˚C	4	5	mA	MB96F353/F355
			+125˚C	4.7	8		
			+25˚C	4.2	5.2	mA	MB96F356
			+125˚C	4.9	8.2		
	I_{CCRCH}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 2MHz 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped)	+25˚C	2.5	3.5	mA	MB96F353/F355
			+125˚C	3.2	6.5		
			+25˚C	2.7	3.7	mA	MB96F356
			+125˚C	3.4	6.7		
	I_{CCRCL}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 0 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.18	0.3	mA	MB96F353/F355
			+125˚C	0.73	3.1		
			+25˚C	0.4	0.6	mA	MB96F356
			+125˚C	0.95	3.4		
		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 1 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed)	+25˚C	0.15	0.25	mA	MB96F353/F355/F356
			+125˚C	0.7	3.05		
	I_{CCSUB}	Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed)	+25˚C	0.1	0.2	mA	MB96F353/F355/F356
			+125˚C	0.65	3		

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes*	I_{CCSRCL}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.08	0.2	mA	MB96F353/F355
			+125˚C	0.59	2.95		
			+25˚C	0.3	0.5	mA	MB96F356
			+125˚C	0.8	3.3		
		RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.05	0.15	mA	MB96F353/F355/ F356
			+125˚C	0.56	2.9		
	I_{CCSSUB}	Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25˚C	0.04	0.12	mA	MB96F353/F355/ F356
			+125˚C	0.54	2.9		
Power supply current in Timer modes*	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz (CLKRC and CLKSC stopped)	+25˚C	1.3	1.8	mA	MB96F353/F355
			+125˚C	1.9	4.8		
			+25˚C	1.5	2	mA	MB96F356
			+125˚C	2.1	5		
	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.11	0.2	mA	MB96F353/F355
			+125˚C	0.63	3		
			+25˚C	0.35	0.5	mA	MB96F356
			+125˚C	0.85	3.3		
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.08	0.15	mA	MB96F353/F355/ F356
			+125˚C	0.6	2.9		

4. AC Characteristics

Source Clock timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	-	16	MHz	When using a crystal oscillator, PLL off
			0	-	16	MHz	When using an opposite phase external clock, PLL off
			3.5	-	16	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Clock frequency	f_{FCI}	X0	0	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode” , PLL off
			3.5	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode” , PLL on
Clock frequency	f_{CL}	X0A, X1A	32	32.768	100	kHz	When using an oscillation circuit
			0	-	100	kHz	When using an opposite phase external clock
		X0A	0	-	50	kHz	When using a single phase external clock
Clock frequency	f_{CR}	-	50	100	200	kHz	When using slow frequency of RC oscillator
			1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	-	64 or 256 RC clock cycles				Applied after any reset and when activating the RC oscillator. MB96F356: 64 cycles others: 256 cycles
PLL Clock frequency	f_{CLKVCO}	-	64	-	200	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL Phase Jitter	T_{PSKEW}	-	-	-	± 5	ns	For CLKMC (PLL input clock) ≥ 4MHz, jitter coming from external oscillator, crystal or resonator is not covered
Input clock pulse width	P_{WH}, P_{WL}	X0,X1	8	-	-	ns	Duty ratio is about 30% to 70%
Input clock pulse width	P_{WHL}, P_{WLL}	X0A,X1A	5	-	-	µs	

External Bus timing

Note: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

Basic Timing

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	25	—	ns	
	t_{CHCL}			t_{CYC}/2-5	t_{CYC}/2+5		
	t_{CLCH}			t_{CYC}/2-5	t_{CYC}/2+5		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	—	-20	20	ns	
	t_{CHCBL}			-20	20		
	t_{CLCBH}			-20	20		
	t_{CLCBL}			-20	20		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-10	10	ns	
	t_{CHLL}			-10	10		
	t_{CLLH}			-10	10		
	t_{CLLL}			-10	10		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	—	-15	15	ns	
	t_{CLAV}			-15	15		
	t_{CLADV}	AD[15:0], ECLK	—	-15	15	ns	
	t_{CHADV}			-15	15		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX,WRHX, ECLK	—	-10	10	ns	
	t_{CHRWL}			-10	10		
	t_{CLRWH}			-10	10		
	t_{CLRWL}			-10	10		

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 20$	—	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 20$	—		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 20$	—	ns	
			EACL:ACE=1	$2t_{CYC} - 20$	—		
Valid address ⇒ Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	—	$3t_{CYC} - 60$	ns	w/o cycle extension
			EACL:ACE=1	—	$4t_{CYC} - 60$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0	—	$5t_{CYC}/2 - 60$	ns	w/o cycle extension
			EACL:ACE=1	—	$7t_{CYC}/2 - 60$		
RDX pulse width	t_{RLRH}	RDX	—	$3t_{CYC}/2 - 8$	—	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	—	—	$3t_{CYC}/2 - 55$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	—	0	—	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:16]	—	0	—	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 15$	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 15$	—		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:16], ECLK	—	$t_{CYC} - 20$	—	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 20$	—		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	—	$t_{CYC}/2 - 15$	—	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1	– 15	—		
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	$t_{CYC} - 55$	ns	

I²C Timing

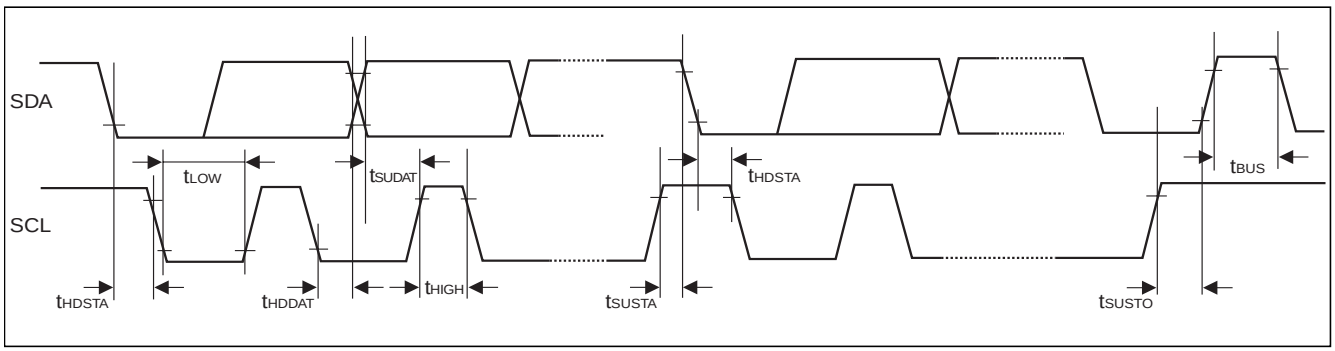
(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} =0V)

Parameter	Symbol	Standard-mode		Fast-mode*1		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t_{HDSTA}	4.0	—	0.6	—	µs
“L” width of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
“H” width of the SCL clock	t_{HIGH}	4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL↑→SDA↓	t_{SUSTA}	4.7	—	0.6	—	µs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}	0	3.45	0	0.9	µs
Data set-up time SDA↓↑→SCL↑	t_{SUDAT}	250	—	100	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t_{SUSTO}	4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUS}	4.7	—	1.3	—	µs
Output fall time from 0.7*Vcc to 0.3*Vcc with a bus capacitance from 10 pF to 400 pF	t_{of}	20 + 0.1*C_b *2	250	20 + 0.1*C_b *2	250	ns
Capacitive load for each bus line	C_b	—	400	—	400	pF
Pulse width of spikes which will be suppressed by input noise filter	t_{SP}	n/a	n/a	0	1*t_{CLKP1}*3	ns

*1 : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.

*2 : C_b = capacitance of one bus line in pF.

*3 : t_{CLKP1} is the cycle time of the peripheral clock CLKP1.



- V_{OH} = 0.7 * V_{CC}
- V_{OL} = 0.3 * V_{CC}
- CMOS Hysteresis 0.7/0.3 input selected

Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.

Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.

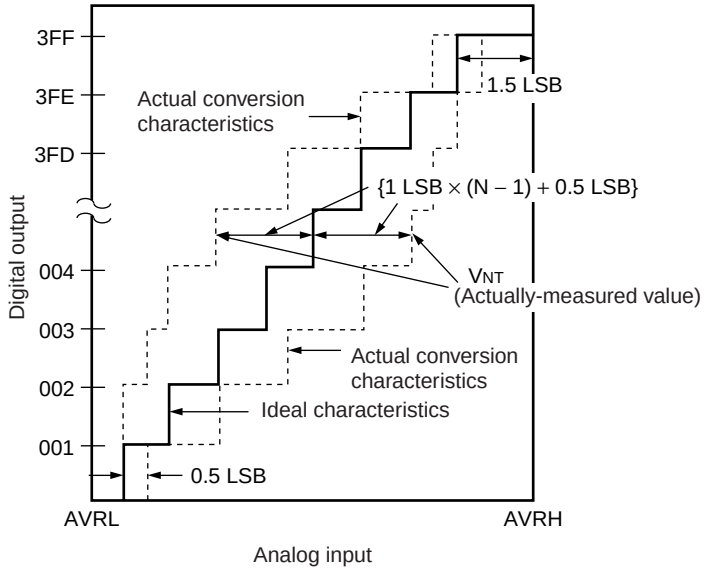
Nonlinearity error: Deviation between a line across zero-transition line (“00 0000 0000” <--> “00 0000 0001”) and full-scale transition line (“11 1111 1110” <--> “11 1111 1111”) and actual conversion characteristics.

Differential nonlinearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

N: A/D converter digital output value

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

V_{NT} : A voltage at which digital output transitions from (N – 1) to N.

7. FLASH memory program/erase characteristics

(T_A = -40˚C to 105˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

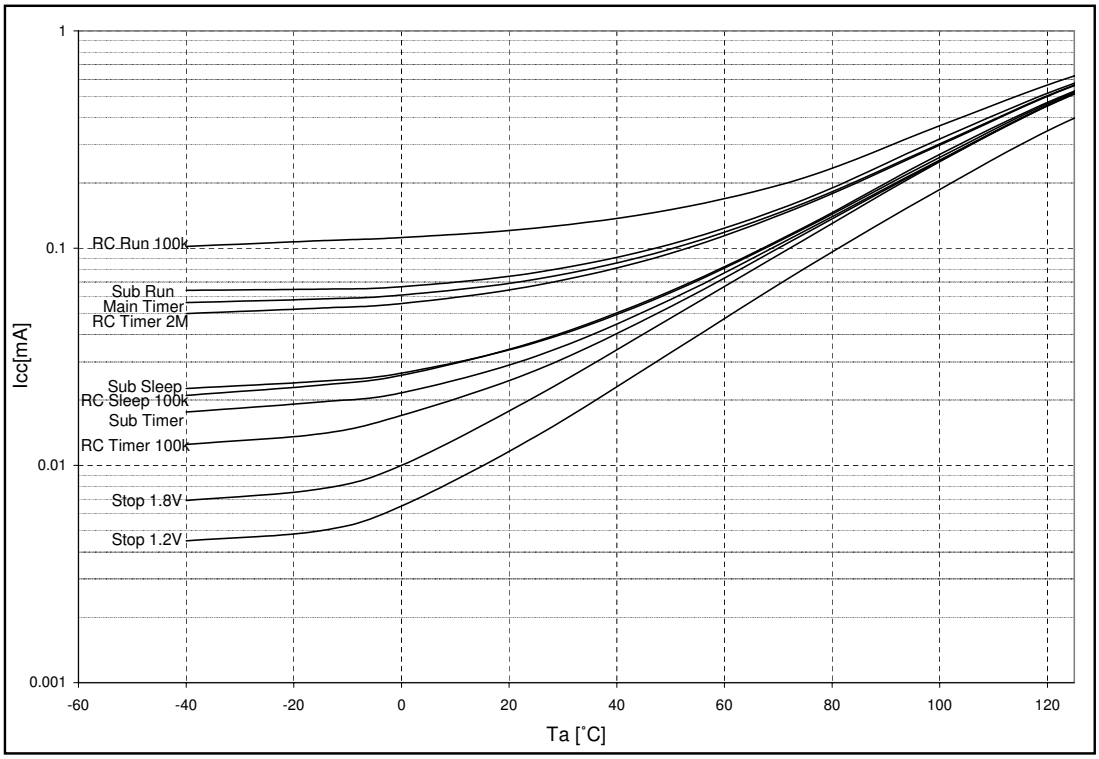
Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Without erasure pre-programming time
Chip erase time	-	n*0.9	n*3.6	s	Without erasure pre-programming time (n is the number of Flash sector of the device)
Word (16-bit width) programming time	-	23	370	us	Without overhead time for submitting write command
Program/Erase cycle	10 000	-	-	cycle	
Flash data retention time	20	-	-	year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85ºC)

Mode name	Details
RC Run 2M	RC Run mode current I_{CCRCH} with the following settings: • RC oscillator set to 2MHz (CKFCR:RCFS = 1) • $f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2}$ = 2MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • 1 Flash/ROM wait states (MTCRA=0239_H) • PLL, Main oscillator and Sub oscillator stopped
RC Run 100k	RC Run mode current I_{CCRCL} with the following settings: • RC oscillator set to 100kHz (CKFCR:RCFS = 0) • $f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2}$ = 100kHz • Regulator in Low Power Mode A (SMCR:LPMS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • 1 Flash/ROM wait states (MTCRA=0239_H) • PLL, Main oscillator and Sub oscillator stopped
Sub Run	Sub Run mode current I_{CCSUB} with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2}$ = 32kHz • Regulator in Low Power Mode A (by hardware) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • 1 Flash/ROM wait states (MTCRA=0239_H) • PLL, RC oscillator and Main oscillator stopped
PLL Sleep 56	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1}$ = 56MHz • f_{CLKP2} = 28MHz • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • RC oscillator and Sub oscillator stopped
PLL Sleep 48	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 96MHz • f_{CLKP1} = 48MHz • f_{CLKP2} = 24MHz • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • RC oscillator and Sub oscillator stopped
PLL Sleep 24	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 48MHz • $f_{CLKP1} = f_{CLKP2}$ = 24MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • RC oscillator and Sub oscillator stopped
Main Sleep	Main Sleep mode current $I_{CCSMAIN}$ with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 4MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • PLL, RC oscillator and Sub oscillator stopped

Mode name	Details
RC Sleep 2M	RC Sleep mode current I_{CCSRCH} with the following settings: • RC oscillator set to 2MHz (CKFCR:RCFS = 1) • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 2MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • PLL, Main oscillator and Sub oscillator stopped
RC Sleep 100k	RC Sleep mode current I_{CCSRCL} with the following settings: • RC oscillator set to 100kHz (CKFCR:RCFS = 0) • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 100kHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped
Sub Sleep	Sub Sleep mode current I_{CCSSUB} with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 32kHz • Regulator in Low Power Mode A (by hardware) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Main oscillator stopped
PLL Timer 48	PLL Timer mode current I_{CCTPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 48MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • RC oscillator and Sub oscillator stopped
Main Timer	Main Timer mode current $I_{CCTMAIN}$ with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 4MHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Sub oscillator stopped
RC Timer 2M	RC Timer mode current I_{CCTRCH} with the following settings: • RC oscillator set to 2MHz (CKFCR:RCFS = 1) • $f_{CLKS1} = f_{CLKS2}$ = 2MHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped
RC Timer 100k	RC Timer mode current I_{CCTRCL} with the following settings: • RC oscillator set to 100kHz (CKFCR:RCFS = 0) • $f_{CLKS1} = f_{CLKS2}$ = 100kHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped
Sub Timer	Sub Timer mode current I_{CCTSUB} with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 32kHz • Regulator in Low Power Mode A (by hardware) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Main oscillator stopped

MB96F356 Low power mode currents



MCU without CAN controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96F353ASB PMC-GSE2	Flash A (96KB)	No	No	64 pins Plastic LQFP (FPT-64P-M23)
MB96F353AWB PMC-GSE2		Yes		
MB96F353ASB PMC1-GSE2		No		64 pins Plastic LQFP (FPT-64P-M24)
MB96F353AWB PMC1-GSE2		Yes		
MB96F355ASB PMC-GSE2	Flash A (160KB)	No		64 pins Plastic LQFP (FPT-64P-M23)
MB96F355AWB PMC-GSE2		Yes		
MB96F355ASB PMC1-GSE2		No		64 pins Plastic LQFP (FPT-64P-M24)
MB96F355AWB PMC1-GSE2		Yes		
MB96F356ASB PMC-GSE2	Flash A (288KB)	No		64 pins Plastic LQFP (FPT-64P-M23)
MB96F356AWB PMC-GSE2		Yes		
MB96F356ASB PMC1-GSE2		No		64 pins Plastic LQFP (FPT-64P-M24)
MB96F356AWB PMC1-GSE2		Yes		

This datasheet is also valid for the following outdated devices:

MB96F356YSA, MB96F356RSA, MB96F356YWA, MB96F356RWA, MB96F356ASA, MB96F356AWA, MB96F353RSA, MB96F353RWA, MB96F355RSA, MB96F355RWA, MB96F353ASA, MB96F353AWA, MB96F355ASA, MB96F355AWA.

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