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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	49
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f355rwbpmc-gse2

MB96350 Series

■ PIN CIRCUIT TYPE

Pin circuit types

FPT-64P-M23/24	
Pin no.	Circuit type ^{*1}
1	Supply
2	G
3 to 15	I
16,17	H
18	Supply
19,20	B ^{*2}
19,20	H ^{*3}
21 to 23	C
24 to 44	H
45	E
46,47	A
48,49	Supply
50	F
51	H
52,53	N
54 to 61	H
62,63	I
64	Supply

*1: Please refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types

*2: Devices with suffix “W”

*3: Devices without suffix “W”

MB96350 Series

■ RAMSTART/END AND EXTERNAL BUS END ADDRESSES

Devices	Bank 0 RAM size	Bank 1 RAM size	External Bus end address	RAMSTART0	RAMSTART1	RAMEND1
MB96F353/F355	8KByte	-	00:51FF _H	00:6240 _H	-	-
MB96F356	12KByte	-	00:51FF _H	00:5240 _H	-	-

MB96350 Series

■ I/O MAP

I/O map MB96(F)35x (1 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000000 _H	I/O Port P00 - Port Data Register	PDR00		R/W
000001 _H	I/O Port P01 - Port Data Register	PDR01		R/W
000002 _H	I/O Port P02 - Port Data Register	PDR02		R/W
000003 _H	I/O Port P03 - Port Data Register	PDR03		R/W
000004 _H	I/O Port P04 - Port Data Register	PDR04		R/W
000005 _H	I/O Port P05 - Port Data Register	PDR05		R/W
000006 _H	I/O Port P06 - Port Data Register	PDR06		R/W
000007 _H - 000017 _H	Reserved			-
000018 _H	ADC0 - Control Status register Low	ADCSL	ADCS	R/W
000019 _H	ADC0 - Control Status register High	ADCSH		R/W
00001A _H	ADC0 - Data Register Low	ADCRL	ADCR	R
00001B _H	ADC0 - Data Register High	ADCRH		R
00001C _H	ADC0 - Setting Register		ADSR	R/W
00001D _H	ADC0 - Setting Register			R/W
00001E _H	ADC0 - Extended Configuration Register	ADECR		R/W
00001F _H	Reserved			-
000020 _H	FRT0 - Data register of free-running timer		TCDT0	R/W
000021 _H	FRT0 - Data register of free-running timer			R/W
000022 _H	FRT0 - Control status register of free-running timer Low	TCCSL0	TCCS0	R/W
000023 _H	FRT0 - Control status register of free-running timer High	TCCSH0		R/W
000024 _H	FRT1 - Data register of free-running timer		TCDT1	R/W
000025 _H	FRT1 - Data register of free-running timer			R/W
000026 _H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	R/W
000027 _H	FRT1 - Control status register of free-running timer High	TCCSH1		R/W
000028 _H - 000033 _H	Reserved			-

MB96350 Series

I/O map MB96(F)35x (4 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00006D _H	RLT3 - Timer Control Status Register High	TMCSRH3		R/W
00006E _H	RLT3 - Reload Register - for writing		TMRLR3	W
00006E _H	RLT3 - Reload Register - for reading		TMR3	R
00006F _H	RLT3 - Reload Register - for writing			W
00006F _H	RLT3 - Reload Register - for reading			R
000070 _H	RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)	TMCSRL6	TMCSR6	R/W
000071 _H	RLT6 - Timer Control Status Register High (dedic. RLT for PPG)	TMCSRH6		R/W
000072 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing		TMRLR6	W
000072 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R
000073 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing			W
000073 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading			R
000074 _H	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10	R/W
000075 _H	PPG3-PPG0 - General Control register 1 High	GCN1H0		R/W
000076 _H	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20	R/W
000077 _H	PPG3-PPG0 - General Control register 2 High	GCN2H0		R/W
000078 _H	PPG0 - Timer register		PTMR0	R
000079 _H	PPG0 - Timer register			R
00007A _H	PPG0 - Period setting register		PCSR0	W
00007B _H	PPG0 - Period setting register			W
00007C _H	PPG0 - Duty cycle register		PDUT0	W
00007D _H	PPG0 - Duty cycle register			W
00007E _H	PPG0 - Control status register Low	PCNL0	PCN0	R/W
00007F _H	PPG0 - Control status register High	PCNH0		R/W
000080 _H	PPG1 - Timer register		PTMR1	R
000081 _H	PPG1 - Timer register			R
000082 _H	PPG1 - Period setting register		PCSR1	W

MB96350 Series

I/O map MB96(F)35x (8 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00010D _H	DMA1 - I/O register address pointer high byte	IOAH1		R/W
00010E _H	DMA1 - Data counter low byte	DCTL1	DCT1	R/W
00010F _H	DMA1 - Data counter high byte	DCTH1		R/W
000110 _H	DMA2 - Buffer address pointer low byte	BAPL2		R/W
000111 _H	DMA2 - Buffer address pointer middle byte	BAPM2		R/W
000112 _H	DMA2 - Buffer address pointer high byte	BAPH2		R/W
000113 _H	DMA2 - DMA control register	DMACS2		R/W
000114 _H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W
000115 _H	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116 _H	DMA2 - Data counter low byte	DCTL2	DCT2	R/W
000117 _H	DMA2 - Data counter high byte	DCTH2		R/W
000118 _H	DMA3 - Buffer address pointer low byte	BAPL3		R/W
000119 _H	DMA3 - Buffer address pointer middle byte	BAPM3		R/W
00011A _H	DMA3 - Buffer address pointer high byte	BAPH3		R/W
00011B _H	DMA3 - DMA control register	DMACS3		R/W
00011C _H	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
00011D _H	DMA3 - I/O register address pointer high byte	IOAH3		R/W
00011E _H	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
00011F _H	DMA3 - Data counter high byte	DCTH3		R/W
000120 _H - 00017F _H	Reserved			-
000180 _H - 00037F _H	CPU - General Purpose registers (RAM access)	GPR_RAM		R/W
000380 _H	DMA0 - Interrupt select	DISEL0		R/W
000381 _H	DMA1 - Interrupt select	DISEL1		R/W
000382 _H	DMA2 - Interrupt select	DISEL2		R/W
000383 _H	DMA3 - Interrupt select	DISEL3		R/W
000384 _H - 00038F _H	Reserved			-
000390 _H	DMA - Status register low byte	DSRL	DSR	R/W
000391 _H	DMA - Status register high byte	DSRH		R/W

MB96350 Series

I/O map MB96(F)35x (9 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000392 _H	DMA - Stop status register low byte	DSSRL	DSSR	R/W
000393 _H	DMA - Stop status register high byte	DSSRH		R/W
000394 _H	DMA - Enable register low byte	DERL	DER	R/W
000395 _H	DMA - Enable register high byte	DERH		R/W
000396 _H - 00039F _H	Reserved			-
0003A0 _H	Interrupt level register	ILR	ICR	R/W
0003A1 _H	Interrupt index register	IDX		R/W
0003A2 _H	Interrupt vector table base register Low	TBRL	TBR	R/W
0003A3 _H	Interrupt vector table base register High	TBRH		R/W
0003A4 _H	Delayed Interrupt register	DIRR		R/W
0003A5 _H	Non Maskable Interrupt register	NMI		R/W
0003A6 _H - 0003AB _H	Reserved			-
0003AC _H	EDSU communication interrupt selection Low	EDSU2L	EDSU2	R/W
0003AD _H	EDSU communication interrupt selection High	EDSU2H		R/W
0003AE _H	ROM mirror control register	ROMM		R/W
0003AF _H	EDSU configuration register	EDSU		R/W
0003B0 _H	Memory patch control/status register ch 0/1		PFCS0	R/W
0003B1 _H	Memory patch control/status register ch 0/1			R/W
0003B2 _H	Memory patch control/status register ch 2/3		PFCS1	R/W
0003B3 _H	Memory patch control/status register ch 2/3			R/W
0003B4 _H	Memory patch control/status register ch 4/5		PFCS2	R/W
0003B5 _H	Memory patch control/status register ch 4/5			R/W
0003B6 _H	Memory patch control/status register ch 6/7		PFCS3	R/W
0003B7 _H	Memory patch control/status register ch 6/7			R/W
0003B8 _H	Memory Patch function - Patch address 0 low	PFAL0		R/W
0003B9 _H	Memory Patch function - Patch address 0 middle	PFAM0		R/W
0003BA _H	Memory Patch function - Patch address 0 high	PFAH0		R/W
0003BB _H	Memory Patch function - Patch address 1 low	PFAL1		R/W
0003BC _H	Memory Patch function - Patch address 1 middle	PFAM1		R/W

MB96350 Series

I/O map MB96(F)35x (13 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000446 _H	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447 _H	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448 _H	I/O Port P04 - Port Input Enable Register	PIER04		R/W
000449 _H	I/O Port P05 - Port Input Enable Register	PIER05		R/W
00044A _H	I/O Port P06 - Port Input Enable Register	PIER06		R/W
00044B _H - 000457 _H	Reserved			-
000458 _H	I/O Port P00 - Port Input Level Register	PILR00		R/W
000459 _H	I/O Port P01 - Port Input Level Register	PILR01		R/W
00045A _H	I/O Port P02 - Port Input Level Register	PILR02		R/W
00045B _H	I/O Port P03 - Port Input Level Register	PILR03		R/W
00045C _H	I/O Port P04 - Port Input Level Register	PILR04		R/W
00045D _H	I/O Port P05 - Port Input Level Register	PILR05		R/W
00045E _H	I/O Port P06 - Port Input Level Register	PILR06		R/W
00045F _H - 00046B _H	Reserved			-
00046C _H	I/O Port P00 - Extended Port Input Level Register	EPILR00		R/W
00046D _H	I/O Port P01 - Extended Port Input Level Register	EPILR01		R/W
00046E _H	I/O Port P02 - Extended Port Input Level Register	EPILR02		R/W
00046F _H	I/O Port P03 - Extended Port Input Level Register	EPILR03		R/W
000470 _H	I/O Port P04 - Extended Port Input Level Register	EPILR04		R/W
000471 _H	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472 _H	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W
000473 _H - 00047F _H	Reserved			-
000480 _H	I/O Port P00 - Port Output Drive Register	PODR00		R/W
000481 _H	I/O Port P01 - Port Output Drive Register	PODR01		R/W
000482 _H	I/O Port P02 - Port Output Drive Register	PODR02		R/W
000483 _H	I/O Port P03 - Port Output Drive Register	PODR03		R/W
000484 _H	I/O Port P04 - Port Output Drive Register	PODR04		R/W
000485 _H	I/O Port P05 - Port Output Drive Register	PODR05		R/W

MB96350 Series

I/O map MB96(F)35x (20 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0005AD _H	PPG14 - Timer register			R
0005AE _H	PPG14 - Period setting register		PCSR14	W
0005AF _H	PPG14 - Period setting register			W
0005B0 _H	PPG14 - Duty cycle register		PDUT14	W
0005B1 _H	PPG14 - Duty cycle register			W
0005B2 _H	PPG14 - Control status register Low	PCNL14	PCN14	R/W
0005B3 _H	PPG14 - Control status register High	PCNH14		R/W
0005B4 _H	PPG15 - Timer register		PTMR15	R
0005B5 _H	PPG15 - Timer register			R
0005B6 _H	PPG15 - Period setting register		PCSR15	W
0005B7 _H	PPG15 - Period setting register			W
0005B8 _H	PPG15 - Duty cycle register		PDUT15	W
0005B9 _H	PPG15 - Duty cycle register			W
0005BA _H	PPG15 - Control status register Low	PCNL15	PCN15	R/W
0005BB _H	PPG15 - Control status register High	PCNH15		R/W
0005BC _H	PPG19-PPG16 - General Control register 1 Low	GCN1L4	GCN14	R/W
0005BD _H	PPG19-PPG16 - General Control register 1 High	GCN1H4		R/W
0005BE _H	PPG19-PPG16 - General Control register 2 Low	GCN2L4	GCN24	R/W
0005BF _H	PPG19-PPG16 - General Control register 2 High	GCN2H4		R/W
0005C0 _H	PPG16 - Timer register		PTMR16	R
0005C1 _H	PPG16 - Timer register			R
0005C2 _H	PPG16 - Period setting register		PCSR16	W
0005C3 _H	PPG16 - Period setting register			W
0005C4 _H	PPG16 - Duty cycle register		PDUT16	W
0005C5 _H	PPG16 - Duty cycle register			W
0005C6 _H	PPG16 - Control status register Low	PCNL16	PCN16	R/W
0005C7 _H	PPG16 - Control status register High	PCNH16		R/W
0005C8 _H	PPG17 - Timer register		PTMR17	R
0005C9 _H	PPG17 - Timer register			R
0005CA _H	PPG17 - Period setting register		PCSR17	W

MB96350 Series

I/O map MB96(F)35x (23 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000808 _H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809 _H	CAN1 - Interrupt Register High	INTRH1		R
00080A _H	CAN1 - Test Register Low	TESTRL1	TESTR1	R/W
00080B _H	CAN1 - Test Register High (reserved)	TESTRH1		R
00080C _H	CAN1 - BRP Extension register Low	BRPERL1	BRPER1	R/W
00080D _H	CAN1 - BRP Extension register High (reserved)	BRPERH1		R
00080E _H - 00080F _H	Reserved			-
000810 _H	CAN1 - IF1 Command request register Low	IF1CREQL1	IF1CREQ1	R/W
000811 _H	CAN1 - IF1 Command request register High	IF1CREQH1		R/W
000812 _H	CAN1 - IF1 Command Mask register Low	IF1CMSKL1	IF1CMSK1	R/W
000813 _H	CAN1 - IF1 Command Mask register High (re- served)	IF1CMSKH1		R
000814 _H	CAN1 - IF1 Mask 1 Register Low	IF1MSK1L1	IF1MSK11	R/W
000815 _H	CAN1 - IF1 Mask 1 Register High	IF1MSK1H1		R/W
000816 _H	CAN1 - IF1 Mask 2 Register Low	IF1MSK2L1	IF1MSK21	R/W
000817 _H	CAN1 - IF1 Mask 2 Register High	IF1MSK2H1		R/W
000818 _H	CAN1 - IF1 Arbitration 1 Register Low	IF1ARB1L1	IF1ARB11	R/W
000819 _H	CAN1 - IF1 Arbitration 1 Register High	IF1ARB1H1		R/W
00081A _H	CAN1 - IF1 Arbitration 2 Register Low	IF1ARB2L1	IF1ARB21	R/W
00081B _H	CAN1 - IF1 Arbitration 2 Register High	IF1ARB2H1		R/W
00081C _H	CAN1 - IF1 Message Control Register Low	IF1MCTRL1	IF1MCTR1	R/W
00081D _H	CAN1 - IF1 Message Control Register High	IF1MCTRH1		R/W
00081E _H	CAN1 - IF1 Data A1 Low	IF1DTA1L1	IF1DTA11	R/W
00081F _H	CAN1 - IF1 Data A1 High	IF1DTA1H1		R/W
000820 _H	CAN1 - IF1 Data A2 Low	IF1DTA2L1	IF1DTA21	R/W
000821 _H	CAN1 - IF1 Data A2 High	IF1DTA2H1		R/W
000822 _H	CAN1 - IF1 Data B1 Low	IF1DTB1L1	IF1DTB11	R/W
000823 _H	CAN1 - IF1 Data B1 High	IF1DTB1H1		R/W
000824 _H	CAN1 - IF1 Data B2 Low	IF1DTB2L1	IF1DTB21	R/W
000825 _H	CAN1 - IF1 Data B2 High	IF1DTB2H1		R/W

MB96350 Series

I/O map MB96(F)35x (25 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000884 _H - 00088F _H	Reserved			-
000890 _H	CAN1 - New Data 1 Register Low	NEWDT1L1	NEWDT11	R
000891 _H	CAN1 - New Data 1 Register High	NEWDT1H1		R
000892 _H	CAN1 - New Data 2 Register Low	NEWDT2L1	NEWDT21	R
000893 _H	CAN1 - New Data 2 Register High	NEWDT2H1		R
000894 _H - 00089F _H	Reserved			-
0008A0 _H	CAN1 - Interrupt Pending 1 Register Low	INTPND1L1	INTPND11	R
0008A1 _H	CAN1 - Interrupt Pending 1 Register High	INTPND1H1		R
0008A2 _H	CAN1 - Interrupt Pending 2 Register Low	INTPND2L1	INTPND21	R
0008A3 _H	CAN1 - Interrupt Pending 2 Register High	INTPND2H1		R
0008A4 _H - 0008AF _H	Reserved			-
0008B0 _H	CAN1 - Message Valid 1 Register Low	MSGVAL1L1	MSGVAL11	R
0008B1 _H	CAN1 - Message Valid 1 Register High	MSGVAL1H1		R
0008B2 _H	CAN1 - Message Valid 2 Register Low	MSGVAL2L1	MSGVAL21	R
0008B3 _H	CAN1 - Message Valid 2 Register High	MSGVAL2H1		R
0008B4 _H - 0008CD _H	Reserved			-
0008CE _H	CAN1 - Output enable register	COER1		R/W
0008CF _H - 0008FF _H	Reserved			-
000900 _H	CAN2 - Control register Low	CTRLRL2	CTRLR2	R/W
000901 _H	CAN2 - Control register High (reserved)	CTRLRH2		R
000902 _H	CAN2 - Status register Low	STATRL2	STATR2	R/W
000903 _H	CAN2 - Status register High (reserved)	STATRH2		R
000904 _H	CAN2 - Error Counter Low (Transmit)	ERRCNTL2	ERRCNT2	R
000905 _H	CAN2 - Error Counter High (Receive)	ERRCNTH2		R
000906 _H	CAN2 - Bit Timing Register Low	BTRL2	BTR2	R/W
000907 _H	CAN2 - Bit Timing Register High	BTRH2		R/W
000908 _H	CAN2 - Interrupt Register Low	INTRL2	INTR2	R

MB96350 Series

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

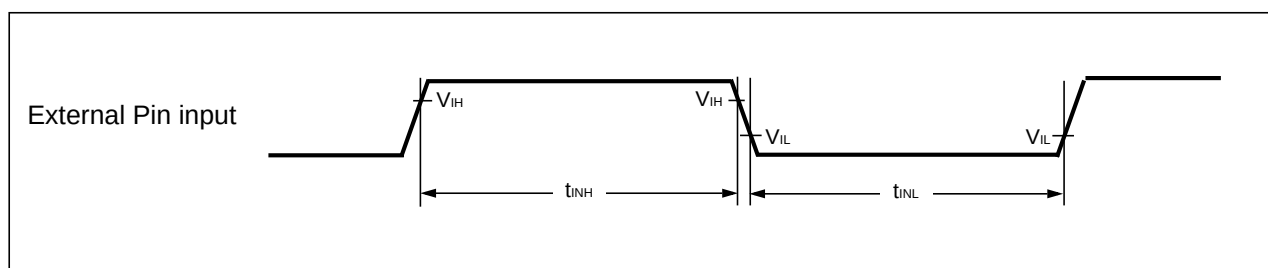
Parameter	Symbol	Condition (at T _A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes*	I _{CCSPLL}	PLL Sleep mode with CLKS1/2 = CLKP1 = 16MHz, CLKP2 = 8MHz (CLKRC and CLKSC stopped)	+25°C	4	6	mA	MB96F353/F355/ F356
			+125°C	4.7	9		
		PLL Sleep mode with CLKS1/2 = CLKP1 = 32MHz, CLKP2 = 16MHz (CLKRC and CLKSC stopped)	+25°C	7	9.5	mA	MB96F353/F355/ F356
			+125°C	8	12.5		
		PLL Sleep mode with CLKS1/2 = 48MHz, CLKP1/2 = 24MHz (CLKRC and CLKSC stopped)	+25°C	7	9	mA	MB96F353/F355/ F356
			+125°C	8	12		
		PLL Sleep mode with CLKS1/2 = CLKP1= 56MHz, CLKP2 = 28MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	11	14.5	mA	MB96F353/F355/ F356
			+125°C	12	17.5		
		PLL Sleep mode with CLKS1/2 = 96MHz, CLKP1= 48MHz, CLKP2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	12	15	mA	MB96F353/F355/ F356
			+125°C	13	18		
	I _{CCSMAIN}	Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	+25°C	1	1.3	mA	MB96F353/F355
			+125°C	1.6	4.1		
			+25°C	1.3	1.8	mA	MB96F356
			+125°C	1.9	4.6		
	I _{CCSRCH}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 2MHz (CLKMC, CLKPLL and CLKSC stopped)	+25°C	0.55	1.1	mA	MB96F353/F355
			+125°C	1.15	3.9		
			+25°C	0.8	1.4	mA	MB96F356
			+125°C	1.4	4.2		

External Input timing

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Used Pin input function
				Min	Max		
Input pulse width	t_{INH} t_{INL}	INTn(_R)	—	200	—	ns	External Interrupt
		NMI(_R)					NMI
		Pnn_m		$2 \cdot t_{CLKP1} + 200$ ($t_{CLKP1} = 1/f_{CLKP1}$)	—	ns	General Purpose IO
		TINn(_R)					Reload Timer
		TTGn(_R)					PPG Trigger input
		ADTG(_R)					AD Converter Trigger
		FRCKn(_R)					Free Running Timer external clock
		INn(_R)					Input Capture

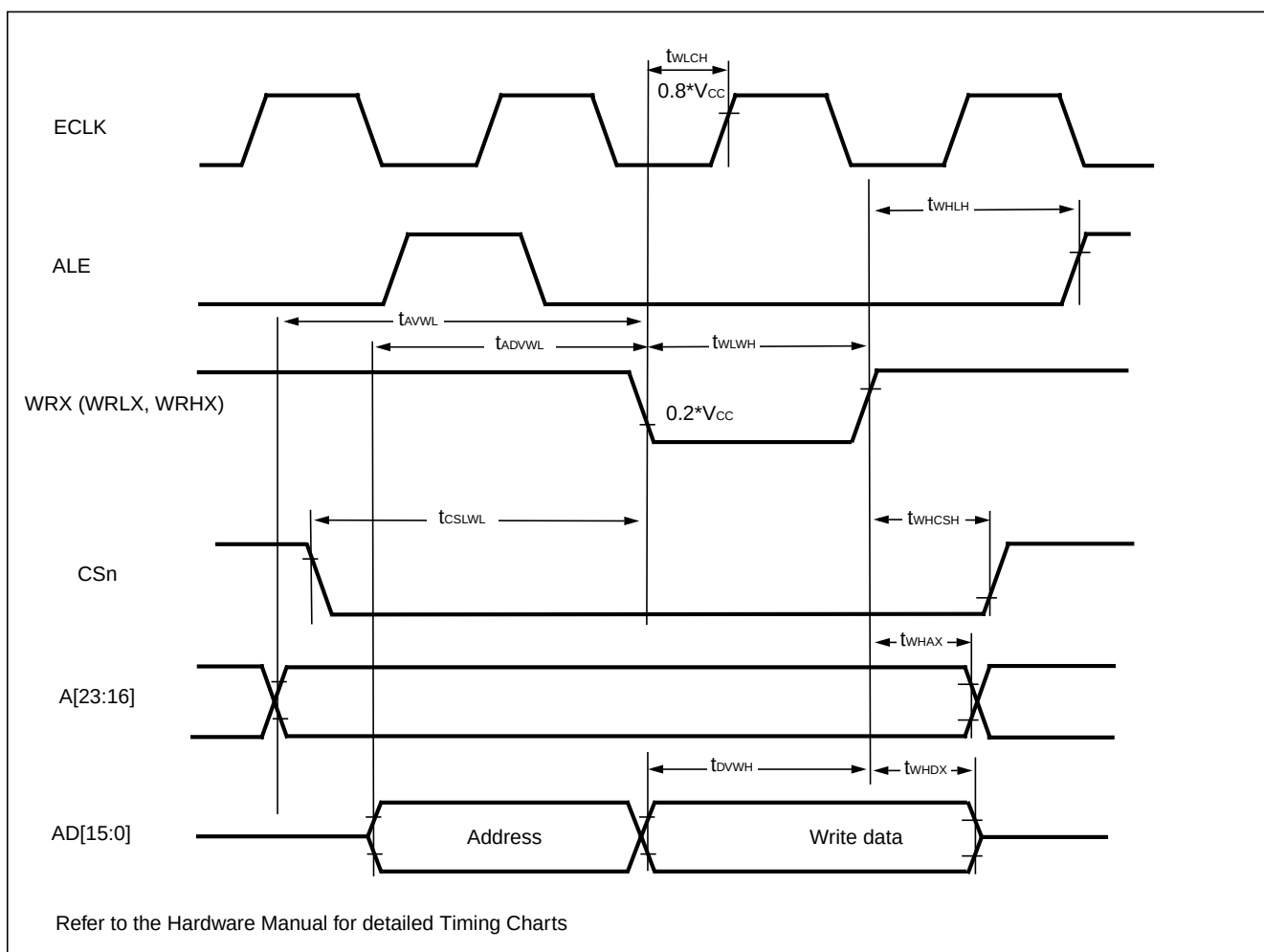
Note : Relocated Resource Inputs have same characteristics



MB96350 Series

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
WRX $\uparrow \Rightarrow$ ALE $\uparrow$ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 15$	—	ns	
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 15$	—		
WRX $\downarrow \Rightarrow$ ECLK $\uparrow$ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	—	$t_{CYC}/2 - 15$	—	ns	
CSn $\Rightarrow$ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	—	$3t_{CYC}/2 - 20$	ns	
			EACL:ACE=1	—	$5t_{CYC}/2 - 20$		
WRX $\Rightarrow$ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	—	$t_{CYC}/2 - 20$	—	ns	



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Ready Input Timing

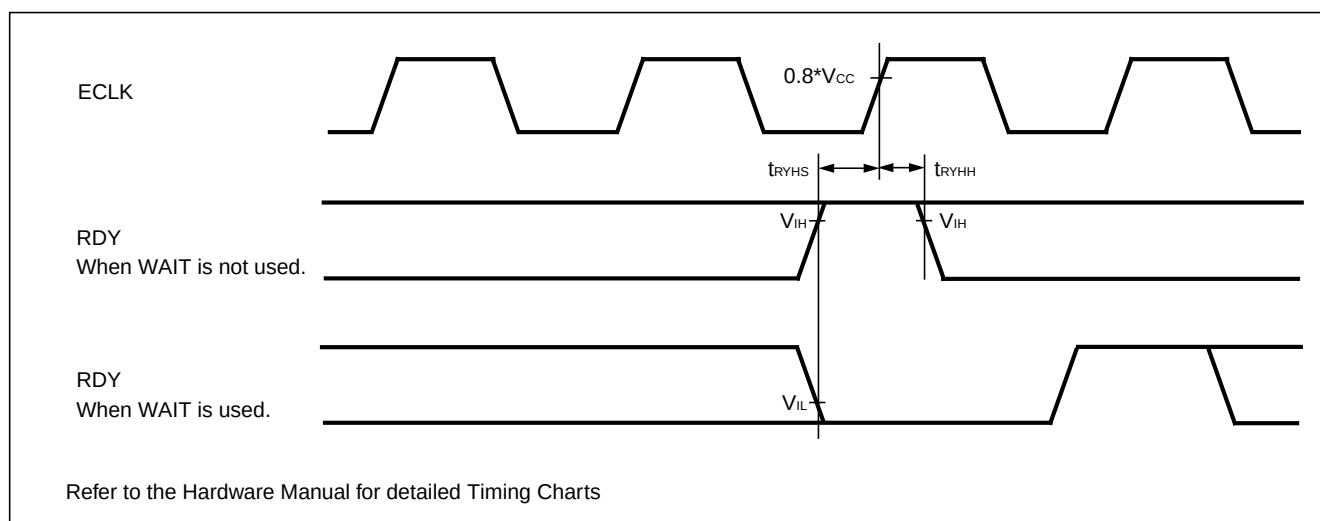
($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{ mA}$, $C_L = 50\text{ pF}$)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t _{RYHS}	RDY	—	35	—	ns	
RDY hold time	t _{RYHH}	RDY		0	—	ns	

(T_A = -40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, I_{Odrive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t _{RYHS}	RDY	—	45	—	ns	
RDY hold time	t _{RYHH}	RDY		0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.



Hold Timing

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{ mA}$, $C_L = 50\text{ pF}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating $\Rightarrow$ HAKX $\downarrow$ time	t _{XHAL}	HAKX	—	t _{CYC} – 20	t _{CYC} + 20	ns	
HAKX $\uparrow$ time $\Rightarrow$ Pin valid time	t _{HAHV}	HAKX		t _{CYC} – 20	t _{CYC} + 20	ns	

(T_A = -40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, I_{Odrive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating $\Rightarrow$ HAKX $\downarrow$ time	t _{XHAL}	HAKX	—	t _{CYC} – 25	t _{CYC} + 25	ns	
HAKX $\uparrow$ time $\Rightarrow$ Pin valid time	t _{HAHV}	HAKX		t _{CYC} – 25	t _{CYC} + 25	ns	

5. Analog Digital Converter

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $3.0\text{ V} \leq \text{AVRH} - \text{AVRL}$, $V_{CC} = \text{AV}_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = \text{AV}_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-	-	± 3	LSB	
Nonlinearity error	-	-	-	-	± 2.5	LSB	
Differential nonlinearity error	-	-	-	-	± 1.9	LSB	
Zero transition voltage	V_{OT}	ANn	$\text{AVRL} - 1.5\text{ LSB}$	$\text{AVRL} + 0.5\text{ LSB}$	$\text{AVRL} + 2.5\text{ LSB}$	V	
Full scale transition voltage	V_{FST}	ANn	$\text{AVRH} - 3.5\text{ LSB}$	$\text{AVRH} - 1.5\text{ LSB}$	$\text{AVRH} + 0.5\text{ LSB}$	V	
Compare time	-	-	1.0	-	16,500	μs	$4.5\text{V} \leq \text{AV}_{CC} \leq 5.5\text{V}$
			2.0	-	-	μs	$3.0\text{V} \leq \text{AV}_{CC} < 4.5\text{V}$
Sampling time	-	-	0.5	-	-	μs	$4.5\text{V} \leq \text{AV}_{CC} \leq 5.5\text{V}$
			1.2	-	-	μs	$3.0\text{V} \leq \text{AV}_{CC} < 4.5\text{V}$
Analog input leakage current (during conversion)	I_{AIN}	ANn	-1	-	+1	μA	$T_A \leq 105\text{ }^{\circ}\text{C}$, AV_{SS} , $\text{AVRL} < V_I < \text{AV}_{CC}$, AVRH
			-1.2	-	+1.2	μA	$105\text{ }^{\circ}\text{C} < T_A \leq 125\text{ }^{\circ}\text{C}$, AV_{SS} , $\text{AVRL} < V_I < \text{AV}_{CC}$, AVRH
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH	0.75 AV_{CC}	-	AV_{CC}	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AV_{CC}	-	2.5	5	mA	A/D Converter active
	I_{AH}	AV_{CC}	-	-	5	μA	A/D Converter not operated
Reference voltage current	I_R	AVRH/ AVRL	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH/ AVRL	-	-	5	μA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

Note: The accuracy gets worse as $|\text{AVRH} - \text{AVRL}|$ becomes smaller.

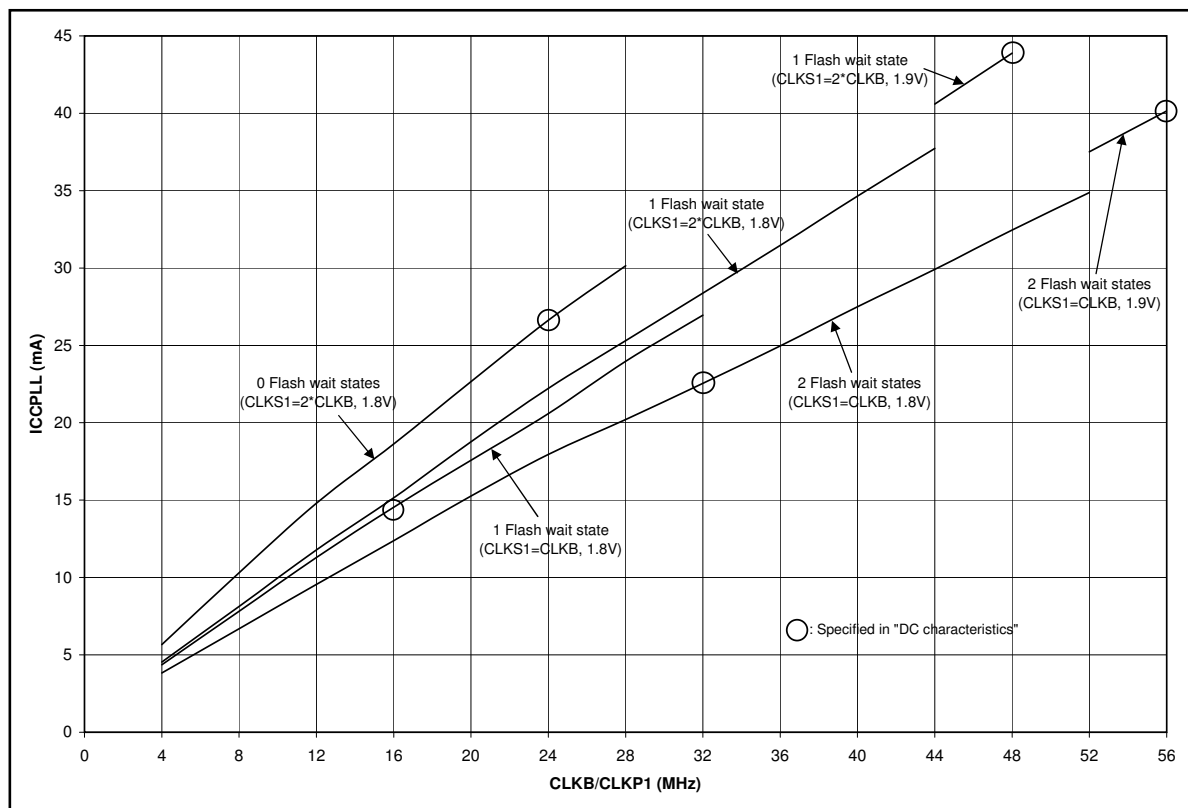
MB96350 Series

Mode name	Details
RC Run 2M	RC Run mode current I_{CCRCH} with the following settings: • RC oscillator set to 2MHz (CKFCR:RCFS = 1) • $f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2} = 2\text{MHz}$ • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • 1 Flash/ROM wait states (MTCRA=0239_H) • PLL, Main oscillator and Sub oscillator stopped
RC Run 100k	RC Run mode current I_{CCRCL} with the following settings: • RC oscillator set to 100kHz (CKFCR:RCFS = 0) • $f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2} = 100\text{kHz}$ • Regulator in Low Power Mode A (SMCR:LPMS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • 1 Flash/ROM wait states (MTCRA=0239_H) • PLL, Main oscillator and Sub oscillator stopped
Sub Run	Sub Run mode current I_{CCSUB} with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2} = 32\text{kHz}$ • Regulator in Low Power Mode A (by hardware) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • 1 Flash/ROM wait states (MTCRA=0239_H) • PLL, RC oscillator and Main oscillator stopped
PLL Sleep 56	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = 56\text{MHz}$ • $f_{CLKP2} = 28\text{MHz}$ • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • RC oscillator and Sub oscillator stopped
PLL Sleep 48	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2} = 96\text{MHz}$ • $f_{CLKP1} = 48\text{MHz}$ • $f_{CLKP2} = 24\text{MHz}$ • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • RC oscillator and Sub oscillator stopped
PLL Sleep 24	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2} = 48\text{MHz}$ • $f_{CLKP1} = f_{CLKP2} = 24\text{MHz}$ • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • RC oscillator and Sub oscillator stopped
Main Sleep	Main Sleep mode current $I_{CCSMAIN}$ with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2} = 4\text{MHz}$ • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • PLL, RC oscillator and Sub oscillator stopped

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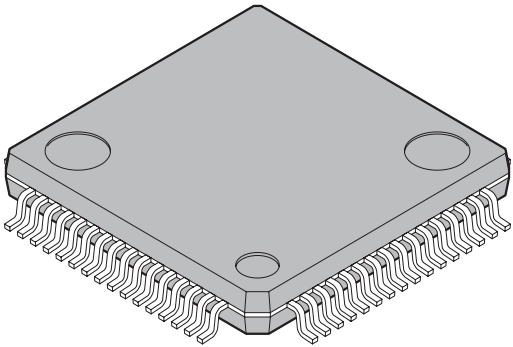
Mode name	Details
RC Sleep 2M	RC Sleep mode current I_{CCSRCH} with the following settings: - RC oscillator set to 2MHz (CKFCR:RCFS = 1) $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2} = 2\text{MHz}$ - Regulator in High Power Mode - Core voltage at 1.8V (VRCCR:HPM[1:0] = 10_B) - PLL, Main oscillator and Sub oscillator stopped
RC Sleep 100k	RC Sleep mode current I_{CCSRCL} with the following settings: - RC oscillator set to 100kHz (CKFCR:RCFS = 0) $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2} = 100\text{kHz}$ - Regulator in Low Power Mode A (SMCR:LPMSS = 1) - Core voltage at 1.8V (VRCCR:LPMA[2:0] = 110_B) - PLL, Main oscillator and Sub oscillator stopped
Sub Sleep	Sub Sleep mode current I_{CCSSUB} with the following settings: $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2} = 32\text{kHz}$ - Regulator in Low Power Mode A (by hardware) - Core voltage at 1.8V (VRCCR:LPMA[2:0] = 110_B) - PLL, RC oscillator and Main oscillator stopped
PLL Timer 48	PLL Timer mode current I_{CCTPLL} with the following settings: $f_{CLKS1} = f_{CLKS2} = 48\text{MHz}$ - Regulator in High Power Mode - Core voltage at 1.8V (VRCCR:HPM[1:0] = 10_B) - RC oscillator and Sub oscillator stopped
Main Timer	Main Timer mode current $I_{CCTMAIN}$ with the following settings: $f_{CLKS1} = f_{CLKS2} = 4\text{MHz}$ - Regulator in Low Power Mode A (SMCR:LPMSS = 1) - Core voltage at 1.8V (VRCCR:LPMA[2:0] = 110_B) - PLL, RC oscillator and Sub oscillator stopped
RC Timer 2M	RC Timer mode current I_{CCTRCH} with the following settings: - RC oscillator set to 2MHz (CKFCR:RCFS = 1) $f_{CLKS1} = f_{CLKS2} = 2\text{MHz}$ - Regulator in Low Power Mode A (SMCR:LPMSS = 1) - Core voltage at 1.8V (VRCCR:LPMA[2:0] = 110_B) - PLL, Main oscillator and Sub oscillator stopped
RC Timer 100k	RC Timer mode current I_{CCTRCL} with the following settings: - RC oscillator set to 100kHz (CKFCR:RCFS = 0) $f_{CLKS1} = f_{CLKS2} = 100\text{kHz}$ - Regulator in Low Power Mode A (SMCR:LPMSS = 1) - Core voltage at 1.8V (VRCCR:LPMA[2:0] = 110_B) - PLL, Main oscillator and Sub oscillator stopped
Sub Timer	Sub Timer mode current I_{CCTSUB} with the following settings: $f_{CLKS1} = f_{CLKS2} = 32\text{kHz}$ - Regulator in Low Power Mode A (by hardware) - Core voltage at 1.8V (VRCCR:LPMA[2:0] = 110_B) - PLL, RC oscillator and Main oscillator stopped

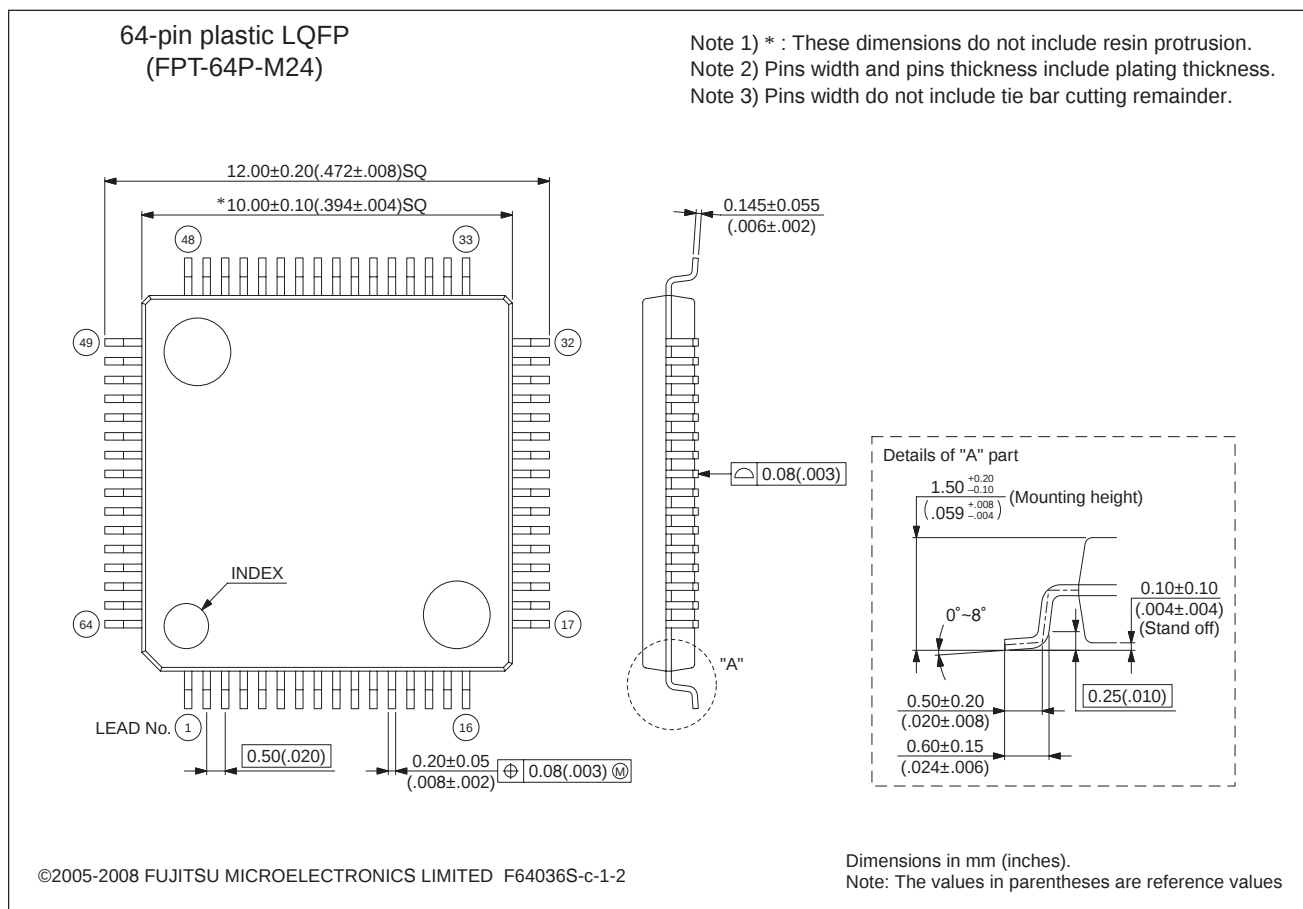
MB96F356 PLL Run mode currents



MB96350 Series

■ PACKAGE DIMENSION MB96(F)35x LQFP 64 - M24

 64-pin plastic LQFP (FPT-64P-M24)	Lead pitch	0.50 mm
	Package width × package length	10.0 × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
	Code (Reference)	P-LFQFP64-10×10-0.50



Please check the latest package dimension at the following URL.
<http://edevic.fujitsu.com/package/en-search/>

MB96350 Series

■ ORDERING INFORMATION

MCU with CAN controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96F353RSB PMC-GSE2	Flash A (96KB)	No	No	64 pins Plastic LQFP (FPT-64P-M23)
MB96F353RWB PMC-GSE2		Yes		
MB96F353RSB PMC1-GSE2		No		64 pins Plastic LQFP (FPT-64P-M24)
MB96F353RWB PMC1-GSE2		Yes		
MB96F355RSB PMC-GSE2	Flash A (160KB)	No		64 pins Plastic LQFP (FPT-64P-M23)
MB96F355RWB PMC-GSE2		Yes		
MB96F355RSB PMC1-GSE2		No		64 pins Plastic LQFP (FPT-64P-M24)
MB96F355RWB PMC1-GSE2		Yes		
MB96F356YSB PMC-GSE2	Flash A (288KB)	No	Yes	64 pins Plastic LQFP (FPT-64P-M23)
MB96F356RSB PMC-GSE2			No	
MB96F356YWB PMC-GSE2		Yes	Yes	
MB96F356RWB PMC-GSE2			No	
MB96F356YSB PMC1-GSE2		No	Yes	64 pins Plastic LQFP (FPT-64P-M24)
MB96F356RSB PMC1-GSE2			No	
MB96F356YWB PMC1-GSE2		Yes	Yes	
MB96F356RWB PMC1-GSE2			No	
MB96V300BRB-ES (for evaluation)	Emulated by ext. RAM	Yes	No	416 pin Plastic BGA (BGA-416P-M02)