Infineon Technologies - MB96F355RWBPMC1-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	49
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f355rwbpmc1-gse2

■ FEATURES

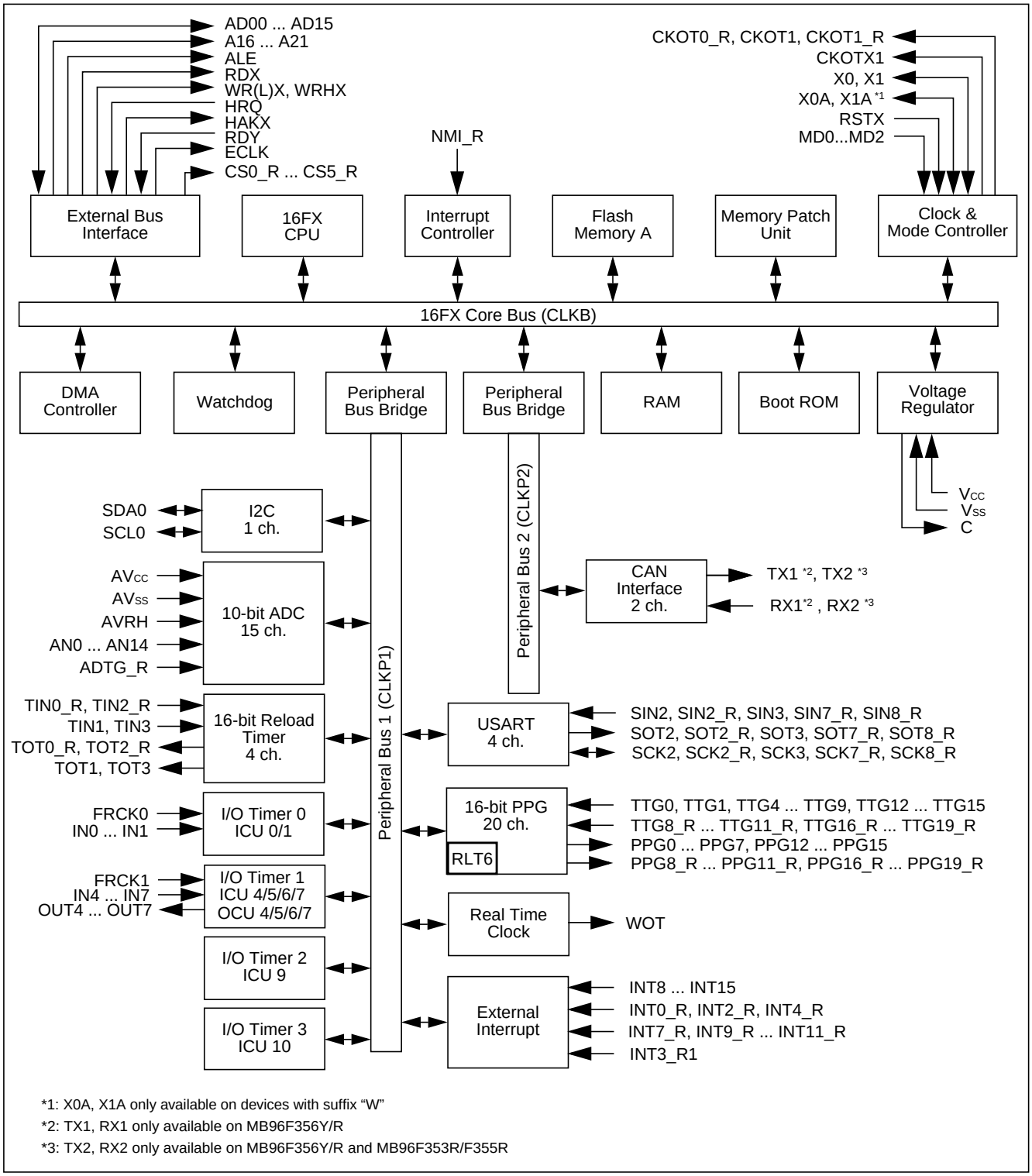
Feature	Description
Technology	• 0.18µm CMOS
CPU	• F²MC-16FX CPU • Up to 56 MHz internal, 17.8 ns instruction cycle time • Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers) • 8-byte instruction execution queue • Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available
System clock	• On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop) • 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor). • Up to 56 MHz external clock • 32-100 kHz subsystem quartz clock • 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog • Clock source selectable from main- and subclock oscillator (part number suffix “W”) and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals. • Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode) • Clock modulator
On-chip voltage regulator	• Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures
Low voltage reset	• Reset is generated when supply voltage is below minimum.
Code Security	• Protects ROM content from unintended read-out
Memory Patch Function	• Replaces ROM content • Can also be used to implement embedded debug support
DMA	• Automatic transfer function independent of CPU, can be assigned freely to resources
Interrupts	• Fast Interrupt processing • 8 programmable priority levels • Non-Maskable Interrupt (NMI)
Timers	• Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer) • Watchdog Timer

Feature	Description
Real Time Clock	• Can be clocked either from sub oscillator (devices with part number suffix “W”), main oscillator or from the RC oscillator • Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration) • Read/write accessible second/minute/hour registers • Can signal interrupts every half second/second/minute/hour/day • Internal clock divider and prescaler provide exact 1s clock
External Interrupts	• Edge sensitive or level sensitive • Interrupt mask and pending bit per channel • Each available CAN channel RX has an external interrupt for wake-up • Selected USART channels SIN have an external interrupt for wake-up
Non Maskable Interrupt	• Disabled after reset • Once enabled, can not be disabled other than by reset. • Level high or level low sensitive • Pin shared with external interrupt 0.
External bus interface	• 8-bit or 16-bit bidirectional data • Up to 24-bit addresses • 6 chip select signals • Multiplexed address/data lines • Wait state request • External bus master possible • Timing programmable
I/O Ports	• Virtually all external pins can be used as general purpose I/O • All push-pull outputs (except when used as I2C SDA/SCL line) • Bit-wise programmable as input/output or peripheral signal • Bit-wise programmable input enable • Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL • Bit-wise programmable pull-up resistor • Bit-wise programmable output driving strength for EMI optimization
Packages	• 64-pin plastic LQFP M23/M24

Feature	Description
Flash Memory	• Supports automatic programming, Embedded Algorithm • Write/Erase/Erase-Suspend/Resume commands • A flag indicating completion of the algorithm • Number of erase cycles: 10,000 times • Data retention time: 20 years • Erase can be performed on each sector individually • Sector protection • Flash Security feature to protect the content of the Flash • Low voltage detection during Flash erase

■ BLOCK DIAGRAM

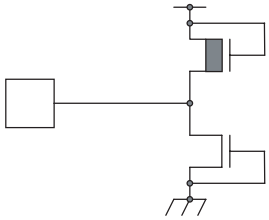
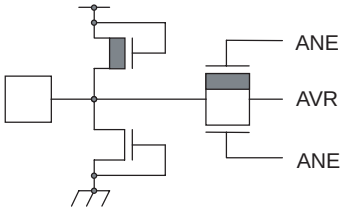
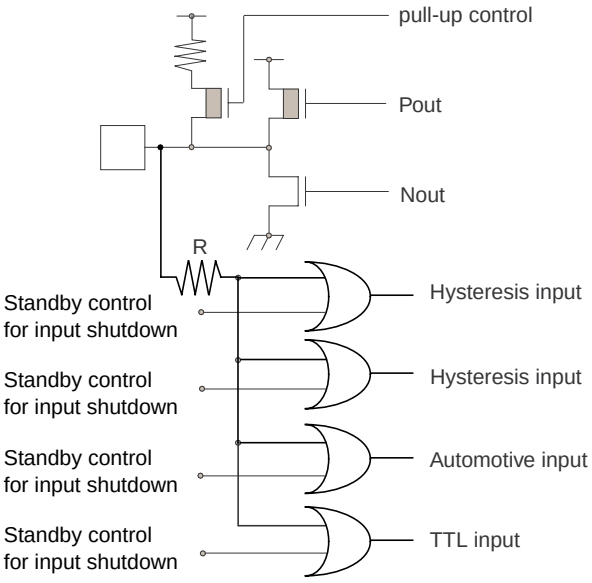
Block diagram of MB96(F)35x



*1: X0A, X1A only available on devices with suffix “W”

*2: TX1, RX1 only available on MB96F356Y/R

*3: TX2, RX2 only available on MB96F356Y/R and MB96F353R/F355R

Type	Circuit	Remarks
F		• Power supply input protection circuit
G		• A/D converter ref+ (AVRH) power supply input pin with protection circuit • Flash devices do not have a protection circuit against VCC for pin AVRH
H		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx. Note: MB96F353/F355: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

I/O map MB96(F)35x (9 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000392H	DMA - Stop status register low byte	DSSRL	DSSR	R/W
000393H	DMA - Stop status register high byte	DSSRH		R/W
000394H	DMA - Enable register low byte	DERL	DER	R/W
000395H	DMA - Enable register high byte	DERH		R/W
000396H-00039FH	Reserved			-
0003A0H	Interrupt level register	ILR	ICR	R/W
0003A1H	Interrupt index register	IDX		R/W
0003A2H	Interrupt vector table base register Low	TBRL	TBR	R/W
0003A3H	Interrupt vector table base register High	TBRH		R/W
0003A4H	Delayed Interrupt register	DIRR		R/W
0003A5H	Non Maskable Interrupt register	NMI		R/W
0003A6H-0003ABH	Reserved			-
0003ACH	EDSU communication interrupt selection Low	EDSU2L	EDSU2	R/W
0003ADH	EDSU communication interrupt selection High	EDSU2H		R/W
0003AEH	ROM mirror control register	ROMM		R/W
0003AFH	EDSU configuration register	EDSU		R/W
0003B0H	Memory patch control/status register ch 0/1		PFCS0	R/W
0003B1H	Memory patch control/status register ch 0/1			R/W
0003B2H	Memory patch control/status register ch 2/3		PFCS1	R/W
0003B3H	Memory patch control/status register ch 2/3			R/W
0003B4H	Memory patch control/status register ch 4/5		PFCS2	R/W
0003B5H	Memory patch control/status register ch 4/5			R/W
0003B6H	Memory patch control/status register ch 6/7		PFCS3	R/W
0003B7H	Memory patch control/status register ch 6/7			R/W
0003B8H	Memory Patch function - Patch address 0 low	PFAL0		R/W
0003B9H	Memory Patch function - Patch address 0 middle	PFAM0		R/W
0003BAH	Memory Patch function - Patch address 0 high	PFAH0		R/W
0003BBH	Memory Patch function - Patch address 1 low	PFAL1		R/W
0003BCH	Memory Patch function - Patch address 1 middle	PFAM1		R/W

I/O map MB96(F)35x (11 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003DB$_H$	Memory Patch function - Patch data 5 High	PFDH5		R/W
0003DC$_H$	Memory Patch function - Patch data 6 Low	PFDL6	PFD6	R/W
0003DD$_H$	Memory Patch function - Patch data 6 High	PFDH6		R/W
0003DE$_H$	Memory Patch function - Patch data 7 Low	PFDL7	PFD7	R/W
0003DF$_H$	Memory Patch function - Patch data 7 High	PFDH7		R/W
0003E0$_H$-0003F0$_H$	Reserved			-
0003F1$_H$	Memory Control Status Register A	MCSRA		R/W
0003F2$_H$	Memory Timing Configuration Register A Low	MTCRAL	MTCRA	R/W
0003F3$_H$	Memory Timing Configuration Register A High	MTCRAH		R/W
0003F4$_H$-0003F8$_H$	Reserved			-
0003F9$_H$	Flash Memory Write Control register 1	FMWC1		R/W
0003FA$_H$	Flash Memory Write Control register 2	FMWC2		R/W
0003FB$_H$	Flash Memory Write Control register 3	FMWC3		R/W
0003FC$_H$	Flash Memory Write Control register 4	FMWC4		R/W
0003FD$_H$	Flash Memory Write Control register 5	FMWC5		R/W
0003FE$_H$-0003FF$_H$	Reserved			-
000400$_H$	Standby Mode control register	SMCR		R/W
000401$_H$	Clock select register	CKSR		R/W
000402$_H$	Clock Stabilization select register	CKSSR		R/W
000403$_H$	Clock monitor register	CKMR		R
000404$_H$	Clock Frequency control register Low	CKFCRL	CKFCR	R/W
000405$_H$	Clock Frequency control register High	CKFCRH		R/W
000406$_H$	PLL Control register Low	PLLCRL	PLLCR	R/W
000407$_H$	PLL Control register High	PLLCRH		R/W
000408$_H$	RC clock timer control register	RCTCR		R/W
000409$_H$	Main clock timer control register	MCTCR		R/W
00040A$_H$	Sub clock timer control register	SCTCR		R/W

I/O map MB96(F)35x (14 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000486H	I/O Port P06 - Port Output Drive Register	PODR06		R/W
000487H-0004A7H	Reserved			-
0004A8H	I/O Port P00 - Pull-Up resistor Control Register	PUCR00		R/W
0004A9H	I/O Port P01 - Pull-Up resistor Control Register	PUCR01		R/W
0004AAH	I/O Port P02 - Pull-Up resistor Control Register	PUCR02		R/W
0004ABH	I/O Port P03 - Pull-Up resistor Control Register	PUCR03		R/W
0004ACH	I/O Port P04 - Pull-Up resistor Control Register	PUCR04		R/W
0004ADH	I/O Port P05 - Pull-Up resistor Control Register	PUCR05		R/W
0004AEH	I/O Port P06 - Pull-Up resistor Control Register	PUCR06		R/W
0004AFH-0004BBH	Reserved			-
0004BCH	I/O Port P00 - External Pin State Register	EPSR00		R
0004BDH	I/O Port P01 - External Pin State Register	EPSR01		R
0004BEH	I/O Port P02 - External Pin State Register	EPSR02		R
0004BFH	I/O Port P03 - External Pin State Register	EPSR03		R
0004C0H	I/O Port P04 - External Pin State Register	EPSR04		R
0004C1H	I/O Port P05 - External Pin State Register	EPSR05		R
0004C2H	I/O Port P06 - External Pin State Register	EPSR06		R
0004C3H-0004CFH	Reserved			-
0004D0H	ADC analog input enable register 0	ADER0		R/W
0004D1H	ADC analog input enable register 1	ADER1		R/W
0004D2H	ADC analog input enable register 2	ADER2		R/W
0004D3H	ADC analog input enable register 3	ADER3		R/W
0004D4H	ADC analog input enable register 4	ADER4		R/W
0004D5H	Reserved			-
0004D6H	Peripheral Resource Relocation Register 0	PRRR0		R/W
0004D7H	Peripheral Resource Relocation Register 1	PRRR1		R/W
0004D8H	Peripheral Resource Relocation Register 2	PRRR2		R/W
0004D9H	Peripheral Resource Relocation Register 3	PRRR3		R/W

I/O map MB96(F)35x (18 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000571H	PPG7 - Duty cycle register			W
000572H	PPG7 - Control status register Low	PCNL7	PCN7	R/W
000573H	PPG7 - Control status register High	PCNH7		R/W
000574H	PPG11-PPG8 - General Control register 1 Low	GCN1L2	GCN12	R/W
000575H	PPG11-PPG8 - General Control register 1 High	GCN1H2		R/W
000576H	PPG11-PPG8 - General Control register 2 Low	GCN2L2	GCN22	R/W
000577H	PPG11-PPG8 - General Control register 2 High	GCN2H2		R/W
000578H	PPG8 - Timer register		PTMR8	R
000579H	PPG8 - Timer register			R
00057AH	PPG8 - Period setting register		PCSR8	W
00057BH	PPG8 - Period setting register			W
00057CH	PPG8 - Duty cycle register		PDUT8	W
00057DH	PPG8 - Duty cycle register			W
00057EH	PPG8 - Control status register Low	PCNL8	PCN8	R/W
00057FH	PPG8 - Control status register High	PCNH8		R/W
000580H	PPG9 - Timer register		PTMR9	R
000581H	PPG9 - Timer register			R
000582H	PPG9 - Period setting register		PCSR9	W
000583H	PPG9 - Period setting register			W
000584H	PPG9 - Duty cycle register		PDUT9	W
000585H	PPG9 - Duty cycle register			W
000586H	PPG9 - Control status register Low	PCNL9	PCN9	R/W
000587H	PPG9 - Control status register High	PCNH9		R/W
000588H	PPG10 - Timer register		PTMR10	R
000589H	PPG10 - Timer register			R
00058AH	PPG10 - Period setting register		PCSR10	W
00058BH	PPG10 - Period setting register			W
00058CH	PPG10 - Duty cycle register		PDUT10	W
00058DH	PPG10 - Duty cycle register			W
00058EH	PPG10 - Control status register Low	PCNL10	PCN10	R/W

I/O map MB96(F)35x (26 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000909H	CAN2 - Interrupt Register High	INTRH2		R
00090AH	CAN2 - Test Register Low	TESTRL2	TESTR2	R/W
00090BH	CAN2 - Test Register High (reserved)	TESTRH2		R
00090CH	CAN2 - BRP Extension register Low	BRPERL2	BRPER2	R/W
00090DH	CAN2 - BRP Extension register High (reserved)	BRPERH2		R
00090EH-00090FH	Reserved			-
000910H	CAN2 - IF1 Command request register Low	IF1CREQL2	IF1CREQ2	R/W
000911H	CAN2 - IF1 Command request register High	IF1CREQH2		R/W
000912H	CAN2 - IF1 Command Mask register Low	IF1CMSKL2	IF1CMSK2	R/W
000913H	CAN2 - IF1 Command Mask register High (reserved)	IF1CMSKH2		R
000914H	CAN2 - IF1 Mask 1 Register Low	IF1MSK1L2	IF1MSK12	R/W
000915H	CAN2 - IF1 Mask 1 Register High	IF1MSK1H2		R/W
000916H	CAN2 - IF1 Mask 2 Register Low	IF1MSK2L2	IF1MSK22	R/W
000917H	CAN2 - IF1 Mask 2 Register High	IF1MSK2H2		R/W
000918H	CAN2 - IF1 Arbitration 1 Register Low	IF1ARB1L2	IF1ARB12	R/W
000919H	CAN2 - IF1 Arbitration 1 Register High	IF1ARB1H2		R/W
00091AH	CAN2 - IF1 Arbitration 2 Register Low	IF1ARB2L2	IF1ARB22	R/W
00091BH	CAN2 - IF1 Arbitration 2 Register High	IF1ARB2H2		R/W
00091CH	CAN2 - IF1 Message Control Register Low	IF1MCTRL2	IF1MCTR2	R/W
00091DH	CAN2 - IF1 Message Control Register High	IF1MCTRH2		R/W
00091EH	CAN2 - IF1 Data A1 Low	IF1DTA1L2	IF1DTA12	R/W
00091FH	CAN2 - IF1 Data A1 High	IF1DTA1H2		R/W
000920H	CAN2 - IF1 Data A2 Low	IF1DTA2L2	IF1DTA22	R/W
000921H	CAN2 - IF1 Data A2 High	IF1DTA2H2		R/W
000922H	CAN2 - IF1 Data B1 Low	IF1DTB1L2	IF1DTB12	R/W
000923H	CAN2 - IF1 Data B1 High	IF1DTB1H2		R/W
000924H	CAN2 - IF1 Data B2 Low	IF1DTB2L2	IF1DTB22	R/W
000925H	CAN2 - IF1 Data B2 High	IF1DTB2H2		R/W

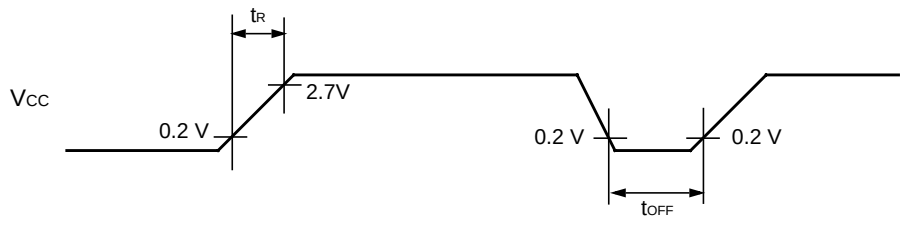
(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes*	I_{CCSRCL}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.08	0.2	mA	MB96F353/F355
			+125˚C	0.59	2.95		
			+25˚C	0.3	0.5	mA	MB96F356
			+125˚C	0.8	3.3		
		RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.05	0.15	mA	MB96F353/F355/ F356
			+125˚C	0.56	2.9		
	I_{CCSSUB}	Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25˚C	0.04	0.12	mA	MB96F353/F355/ F356
			+125˚C	0.54	2.9		
Power supply current in Timer modes*	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz (CLKRC and CLKSC stopped)	+25˚C	1.3	1.8	mA	MB96F353/F355
			+125˚C	1.9	4.8		
			+25˚C	1.5	2	mA	MB96F356
			+125˚C	2.1	5		
	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.11	0.2	mA	MB96F353/F355
			+125˚C	0.63	3		
			+25˚C	0.35	0.5	mA	MB96F356
			+125˚C	0.85	3.3		
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.08	0.15	mA	MB96F353/F355/ F356
			+125˚C	0.6	2.9		

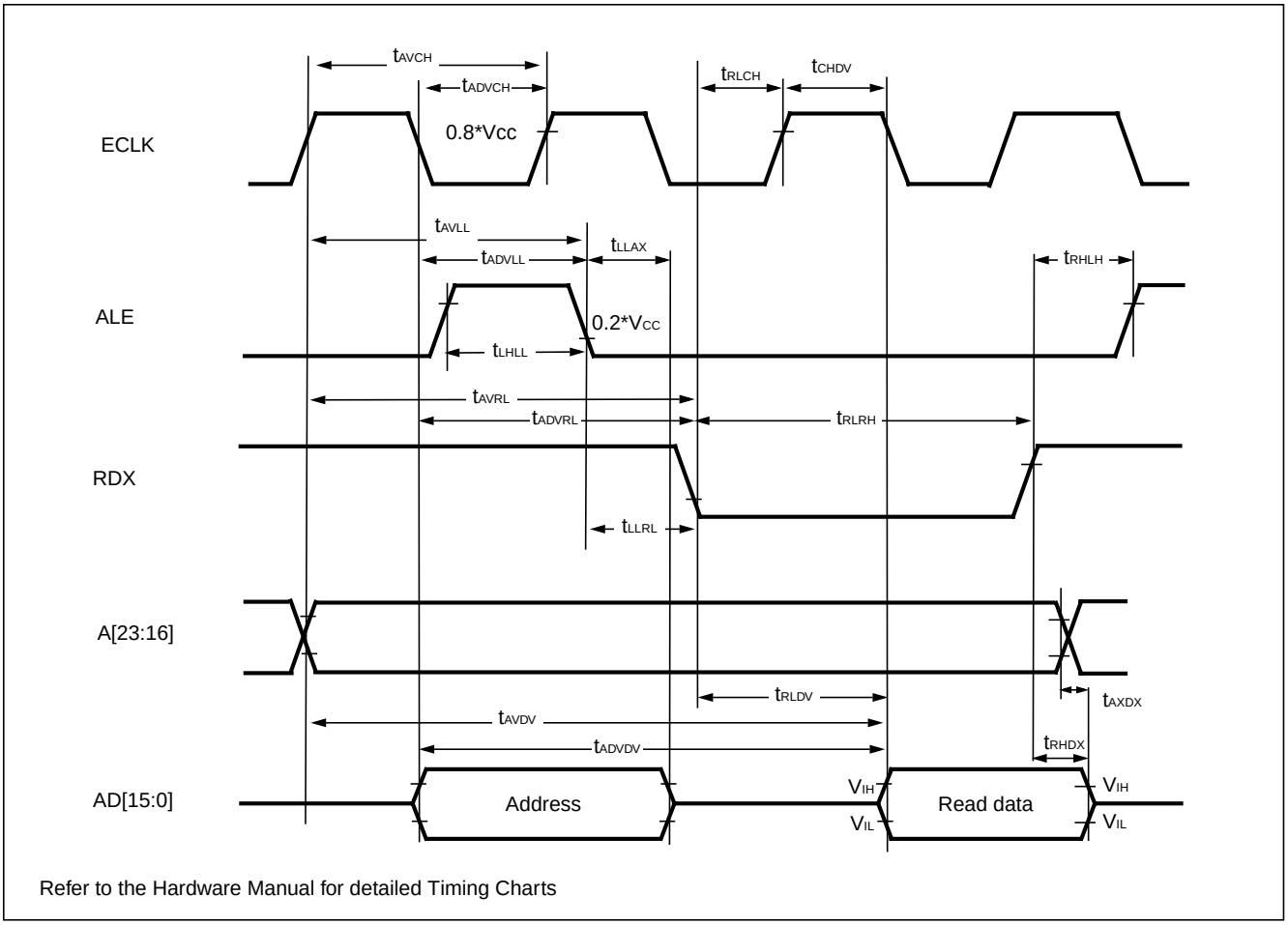
Power On Reset timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	



If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.



Refer to the Hardware Manual for detailed Timing Charts

Bus Timing (Write)

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2$ – 15	—	ns	
			EACL:ACE=1	$5t_{CYC}/2$ – 15	—		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	t_{CYC} – 15	—	ns	
			EACL:ACE=1	$2t_{CYC}$ – 15	—		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	—	t_{CYC} – 5	—	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	—	t_{CYC} – 20	—	ns	w/o cycle extension

USART timing

WARNING: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

(T_A = -40˚C to 125˚C, V_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	V_{CC} = AV_{CC}= 4.5V to 5.5V		V_{CC} = AV_{CC}= 3.0V to 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	4 t_{CLKP1}	—	4 t_{CLKP1}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		N*t_{CLKP1} - 20 *1	—	N*t_{CLKP1} - 30 *1	—	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	—	t_{CLKP1} + 55	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	—	0	—	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn	External Shift Clock Mode	t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		—	2 t_{CLKP1} + 45	—	2 t_{CLKP1} + 55	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		t_{CLKP1}/2 + 10	—	t_{CLKP1}/2 + 10	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK fall time	t_{FE}	SCKn		—	20	—	20	ns
SCK rise time	t_{RE}	SCKn		—	20	—	20	ns

Notes:
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96300 Super series HARDWARE MANUAL”
- t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

*1: Parameter N depends on t_{SCYCI} and can be calculated as follows:
- if t_{SCYCI} = 2*k*t_{CLKP1}, then N = k, where k is an integer > 2
- if t_{SCYCI} = (2*k+1)*t_{CLKP1}, then N = k+1, where k is an integer > 1

Examples:

t_{SCYCI}	N
4*t_{CLKP1}	2
5*t_{CLKP1}, 6*t_{CLKP1}	3
7*t_{CLKP1}, 8*t_{CLKP1}	4
...	...

Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.

Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.

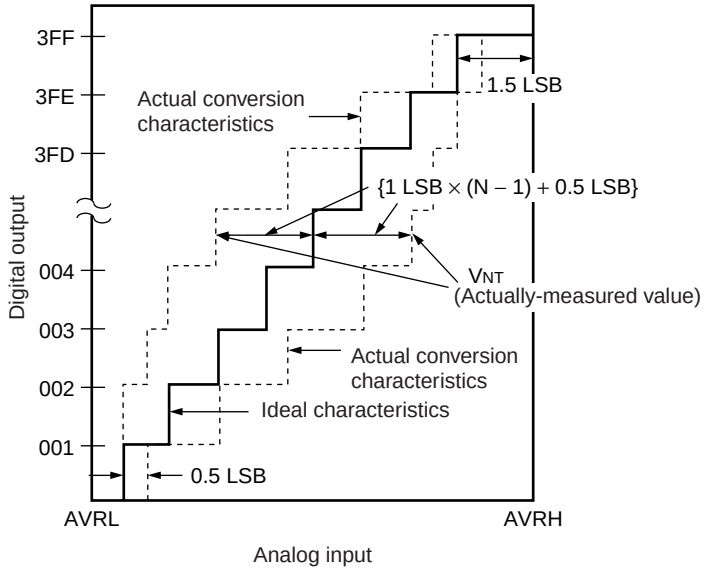
Nonlinearity error: Deviation between a line across zero-transition line (“00 0000 0000” <--> “00 0000 0001”) and full-scale transition line (“11 1111 1110” <--> “11 1111 1111”) and actual conversion characteristics.

Differential nonlinearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

N: A/D converter digital output value

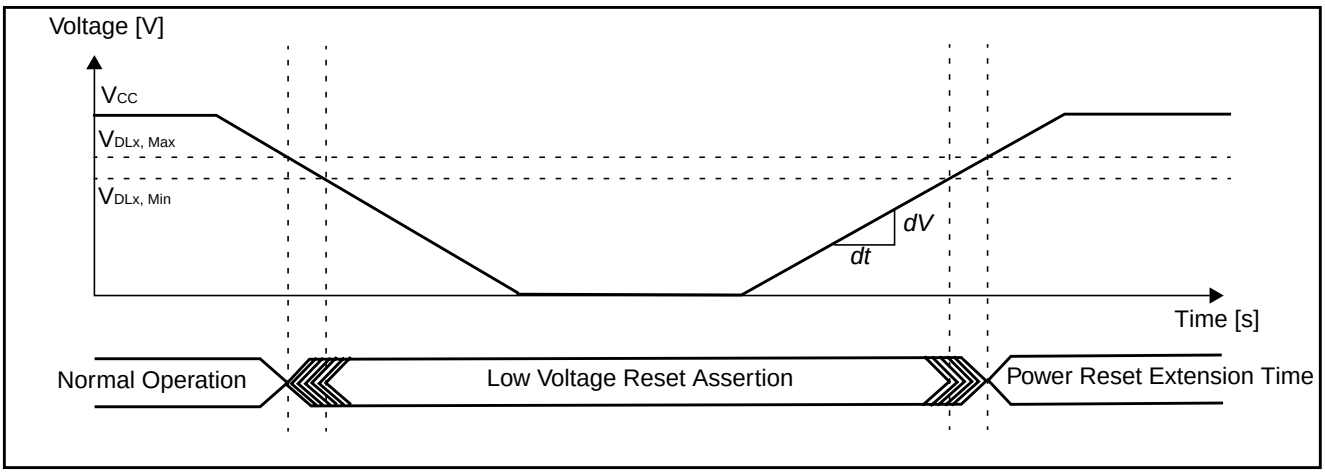
V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

V_{NT} : A voltage at which digital output transitions from (N – 1) to N.

Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.



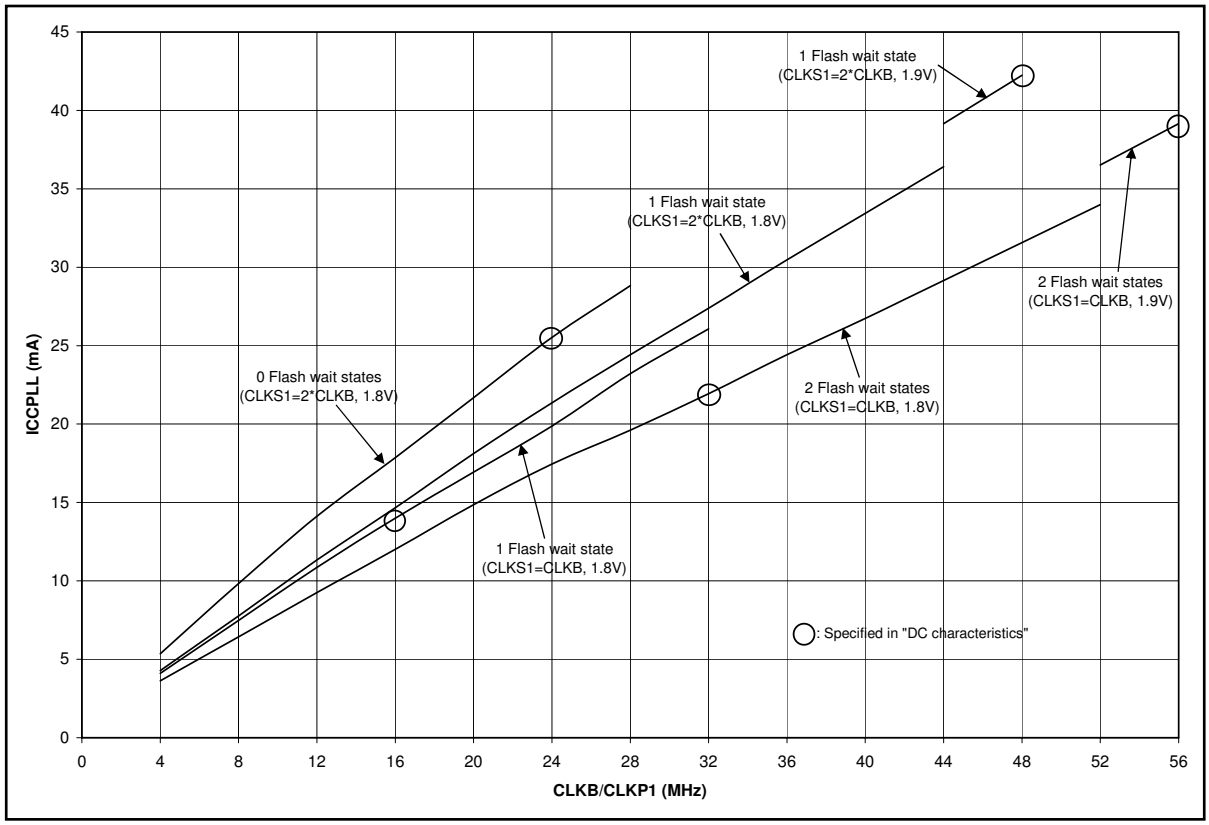
2. Frequency dependency of power supply currents in PLL Run mode

The following diagrams show the current consumption of samples with typical wafer process parameters in PLL Run mode at different frequencies and Flash timing settings.

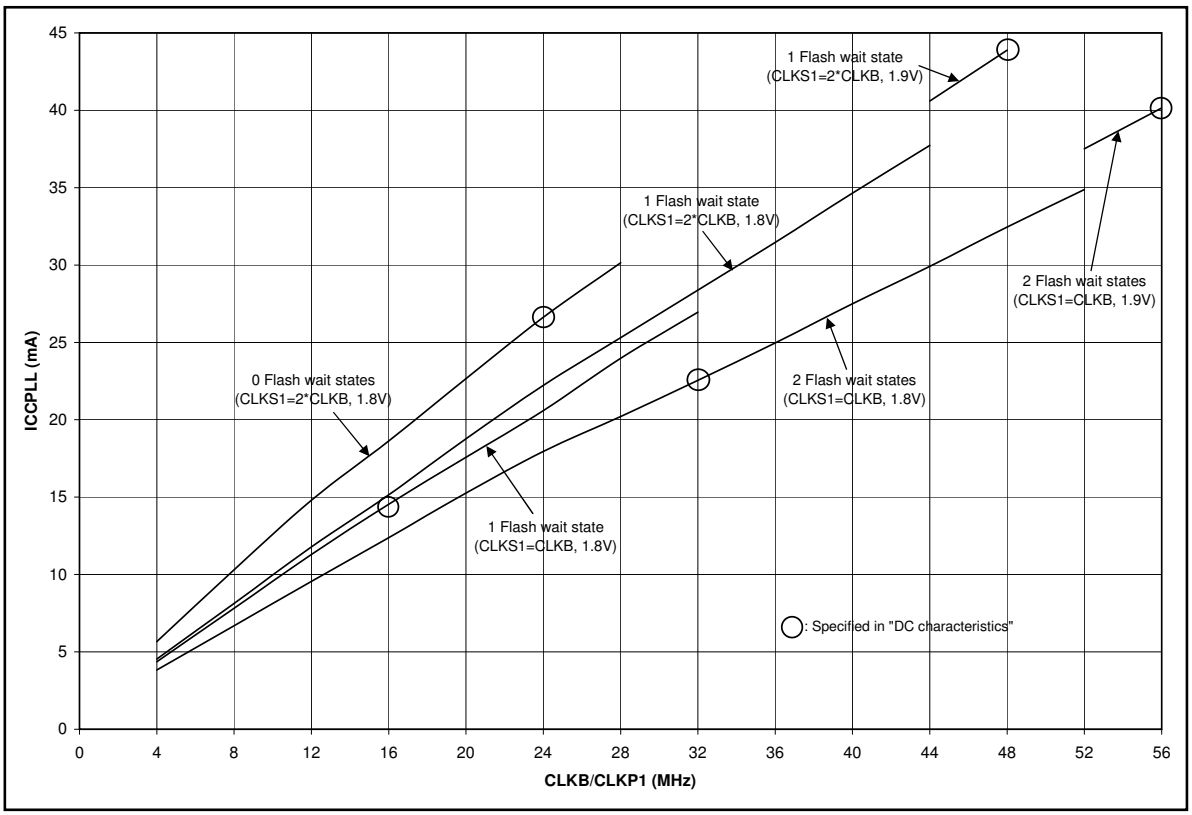
Measurement conditions:

- V_{CC} = AV_{CC} = 5.0V
- Ta = 25˚C
- f_{CLKS1} = f_{CLKB} or f_{CLKS1} = 2*f_{CLKB} as described in diagram
- f_{CLKS2} = f_{CLKS1}
- f_{CLKP1} = f_{CLKB}
- f_{CLKP2} = f_{CLKB}/2
- Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) or 1.9V (VRCR:HPM[1:0] = 11_B) as described in diagram
- Main clock = 4MHz external clock
- Flash memory timing settings:
  - MTCRA=2128_H/2208_H (0 Flash wait states, f_{CLKS1} = 2*f_{CLKB})
  - MTCRA=0239_H/2129_H (1 Flash wait state, f_{CLKS1} = f_{CLKB})
  - MTCRA=$4C09_H$/$6B09_H$ (1 Flash wait state, f_{CLKS1} = 2*f_{CLKB})
  - MTCRA=$233A_H$ (2 Flash wait states, f_{CLKS1} = f_{CLKB})
- Average Flash access rate (number of read accesses to the Flash per CLKB clock cycle, no buffer hit):
  - 0 Flash wait states: 0.5
  - 1 Flash wait states: 0.33
  - 2 Flash wait states: 0.25

MB96F353/F355 PLL Run mode currents



MB96F356 PLL Run mode currents



■ ORDERING INFORMATION

MCU with CAN controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96F353RSB PMC-GSE2	Flash A (96KB)	No	No	64 pins Plastic LQFP (FPT-64P-M23)
MB96F353RWB PMC-GSE2		Yes		
MB96F353RSB PMC1-GSE2		No		64 pins Plastic LQFP (FPT-64P-M24)
MB96F353RWB PMC1-GSE2		Yes		
MB96F355RSB PMC-GSE2	Flash A (160KB)	No		64 pins Plastic LQFP (FPT-64P-M23)
MB96F355RWB PMC-GSE2		Yes		
MB96F355RSB PMC1-GSE2		No		64 pins Plastic LQFP (FPT-64P-M24)
MB96F355RWB PMC1-GSE2		Yes		
MB96F356YSB PMC-GSE2	Flash A (288KB)	No	Yes	64 pins Plastic LQFP (FPT-64P-M23)
MB96F356RSB PMC-GSE2			No	
MB96F356YWB PMC-GSE2		Yes	Yes	
MB96F356RWB PMC-GSE2			No	
MB96F356YSB PMC1-GSE2		No	Yes	64 pins Plastic LQFP (FPT-64P-M24)
MB96F356RSB PMC1-GSE2			No	
MB96F356YWB PMC1-GSE2		Yes	Yes	
MB96F356RWB PMC1-GSE2			No	
MB96V300BRB-ES (for evaluation)	Emulated by ext. RAM	Yes	No	416 pin Plastic BGA (BGA-416P-M02)