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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	51
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f356asbpmc-gse2

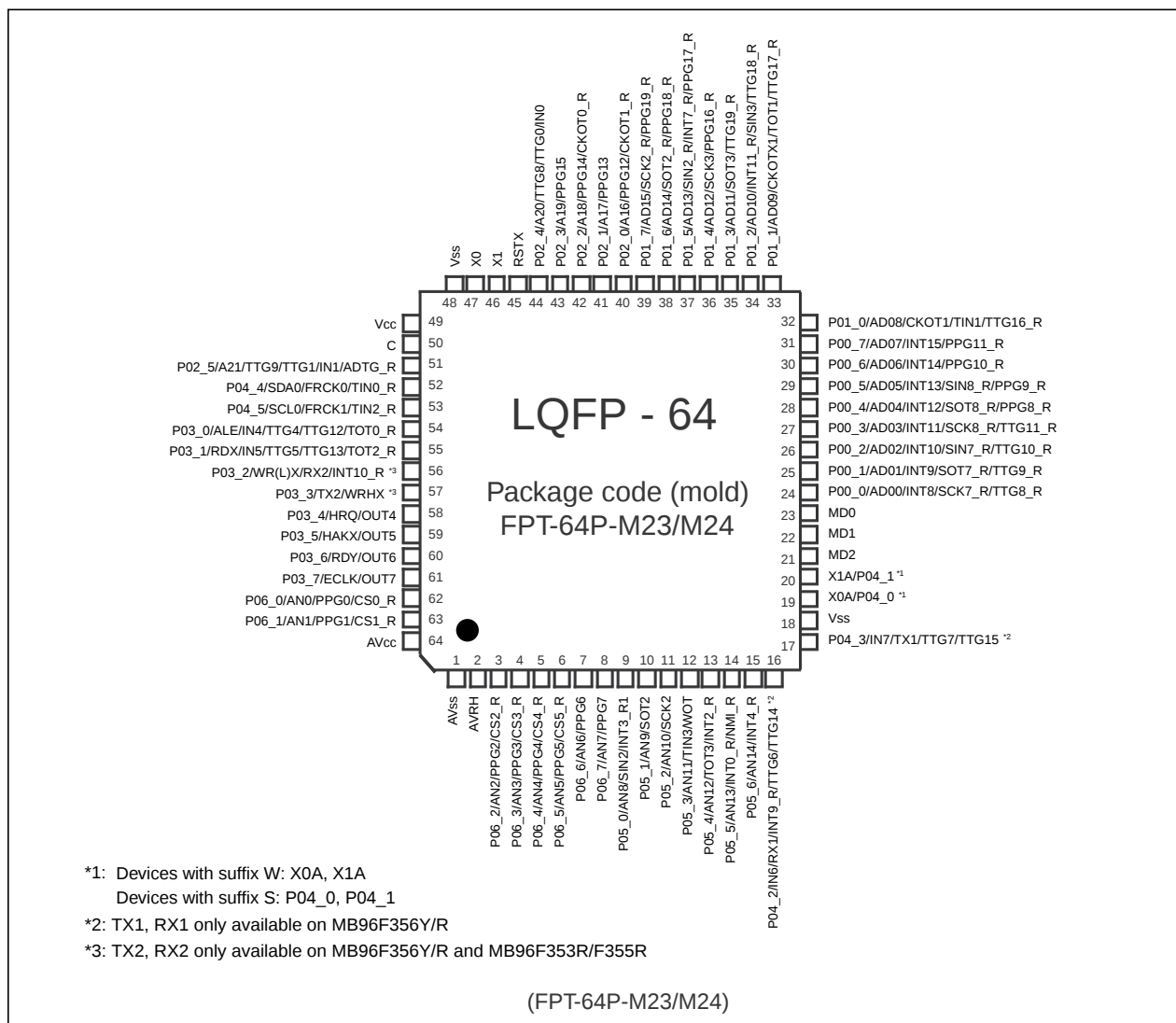
MB96350 Series

Feature	Description
Flash Memory	• Supports automatic programming, Embedded Algorithm • Write/Erase/Erase-Suspend/Resume commands • A flag indicating completion of the algorithm • Number of erase cycles: 10,000 times • Data retention time: 20 years • Erase can be performed on each sector individually • Sector protection • Flash Security feature to protect the content of the Flash • Low voltage detection during Flash erase

MB96350 Series

PIN ASSIGNMENTS

Pin assignment of MB96(F)35x



Remark:

MB96(F)35x products are pin-compatible to F²MC-16LX family MB90350 series.

MB96350 Series

■ USER ROM MEMORY MAP FOR FLASH DEVICES

		MB96F353	MB96F355	MB96F356	
Alternative mode CPU address	Flash memory mode address	Flash size 96kByte	Flash size 160kByte	Flash size 288kByte	
FF:FFFF _H	3F:FFFF _H	S39 - 64K	S39 - 64K	S39 - 64K	Flash A
FF:0000 _H	3F:0000 _H		S38 - 64K	S38 - 64K	
FE:FFFF _H	3E:FFFF _H		External bus	S37 - 64K	
FE:0000 _H	3E:0000 _H			S36 - 64K	
FD:FFFF _H	3D:FFFF _H			External bus	External bus
FD:0000 _H	3D:0000 _H				
FC:FFFF _H	3C:FFFF _H				
FC:0000 _H	3C:0000 _H				
FB:FFFF _H	3B:FFFF _H				
FB:0000 _H	3B:0000 _H				
FA:FFFF _H	3A:FFFF _H				
FA:0000 _H	3A:0000 _H				
F9:FFFF _H	39:FFFF _H	External bus	External bus		
F9:0000 _H	39:0000 _H				
F8:FFFF _H	38:FFFF _H				
F8:0000 _H	38:0000 _H				
F7:FFFF _H	37:FFFF _H				
F7:0000 _H	37:0000 _H				
F6:FFFF _H	36:FFFF _H				
F6:0000 _H	36:0000 _H				
F5:FFFF _H	35:FFFF _H				
F5:0000 _H	35:0000 _H				
F4:FFFF _H	34:FFFF _H	External bus	External bus	External bus	Flash A
F4:0000 _H	34:0000 _H				
F3:FFFF _H	33:FFFF _H				
F3:0000 _H	33:0000 _H				
F2:FFFF _H	32:FFFF _H				
F2:0000 _H	32:0000 _H				
F1:FFFF _H	31:FFFF _H				
F1:0000 _H	31:0000 _H				
F0:FFFF _H	30:FFFF _H				
F0:0000 _H	30:0000 _H				
E0:FFFF _H		Reserved	Reserved	Reserved	Flash A
E0:0000 _H					
DF:FFFF _H					
DF:8000 _H					
DF:7FFF _H	1F:7FFF _H				
DF:6000 _H	1F:6000 _H				
DF:5FFF _H	1F:5FFF _H				
DF:4000 _H	1F:4000 _H				
DF:3FFF _H	1F:3FFF _H				
DF:2000 _H	1F:2000 _H				
DF:1FFF _H	1F:1FFF _H	SA0 - 8K *1	SA0 - 8K *1	SA0 - 8K *1	Flash A
DF:0000 _H	1F:0000 _H				
DE:FFFF _H					
DE:0000 _H					

*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DE:0000_H - DE:007F_H

*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000_H - DF:007F_H

MB96350 Series

I/O map MB96(F)35x (2 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000034 _H	OCU4 - Output Compare Control Status	OCS4		R/W
000035 _H	OCU5 - Output Compare Control Status	OCS5		R/W
000036 _H	OCU4 - Compare Register		OCCP4	R/W
000037 _H	OCU4 - Compare Register			R/W
000038 _H	OCU5 - Compare Register		OCCP5	R/W
000039 _H	OCU5 - Compare Register			R/W
00003A _H	OCU6 - Output Compare Control Status	OCS6		R/W
00003B _H	OCU7 - Output Compare Control Status	OCS7		R/W
00003C _H	OCU6 - Compare Register		OCCP6	R/W
00003D _H	OCU6 - Compare Register			R/W
00003E _H	OCU7 - Compare Register		OCCP7	R/W
00003F _H	OCU7 - Compare Register			R/W
000040 _H	ICU0/ICU1 - Control Status Register	ICS01		R/W
000041 _H	ICU0/ICU1 - Edge register	ICE01		R/W
000042 _H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R
000043 _H	ICU0 - Capture Register High	IPCPH0		R
000044 _H	ICU1 - Capture Register Low	IPCPL1	IPCP1	R
000045 _H	ICU1 - Capture Register High	IPCPH1		R
000046 _H - 00004B _H	Reserved			
00004C _H	ICU4/ICU5 - Control Status Register	ICS45		R/W
00004D _H	ICU4/ICU5 - Edge register	ICE45		R/W
00004E _H	ICU4 - Capture Register Low	IPCPL4	IPCP4	R
00004F _H	ICU4 - Capture Register High	IPCPH4		R
000050 _H	ICU5 - Capture Register Low	IPCPL5	IPCP5	R
000051 _H	ICU5 - Capture Register High	IPCPH5		R
000052 _H	ICU6/ICU7 - Control Status Register	ICS67		R/W
000053 _H	ICU6/ICU7 - Edge register	ICE67		R/W
000054 _H	ICU6 - Capture Register Low	IPCPL6	IPCP6	R
000055 _H	ICU6 - Capture Register High	IPCPH6		R

MB96350 Series

I/O map MB96(F)35x (7 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000DA _H	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	R/W
0000DB _H	USART2 - Baud Rate Generator Register High	BGRH2		R/W
0000DC _H	USART2 - Extended Serial Interrupt Register	ESIR2		R/W
0000DD _H	Reserved			-
0000DE _H	USART3 - Serial Mode Register	SMR3		R/W
0000DF _H	USART3 - Serial Control Register	SCR3		R/W
0000E0 _H	USART3 - TX Register	TDR3		W
0000E0 _H	USART3 - RX Register	RDR3		R
0000E1 _H	USART3 - Serial Status	SSR3		R/W
0000E2 _H	USART3 - Control/Com. Register	ECCR3		R/W
0000E3 _H	USART3 - Ext. Status Register	ESCR3		R/W
0000E4 _H	USART3 - Baud Rate Generator Register Low	BGRL3	BGR3	R/W
0000E5 _H	USART3 - Baud Rate Generator Register High	BGRH3		R/W
0000E6 _H	USART3 - Extended Serial Interrupt Register	ESIR3		R/W
0000E7 _H ~ 0000EF _H	Reserved			-
0000F0 _H ~ 0000FF _H	External Bus area	EXTBUS0		R/W
000100 _H	DMA0 - Buffer address pointer low byte	BAPL0		R/W
000101 _H	DMA0 - Buffer address pointer middle byte	BAPM0		R/W
000102 _H	DMA0 - Buffer address pointer high byte	BAPH0		R/W
000103 _H	DMA0 - DMA control register	DMACS0		R/W
000104 _H	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	R/W
000105 _H	DMA0 - I/O register address pointer high byte	IOAH0		R/W
000106 _H	DMA0 - Data counter low byte	DCTL0	DCT0	R/W
000107 _H	DMA0 - Data counter high byte	DCTH0		R/W
000108 _H	DMA1 - Buffer address pointer low byte	BAPL1		R/W
000109 _H	DMA1 - Buffer address pointer middle byte	BAPM1		R/W
00010A _H	DMA1 - Buffer address pointer high byte	BAPH1		R/W
00010B _H	DMA1 - DMA control register	DMACS1		R/W
00010C _H	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	R/W

MB96350 Series

I/O map MB96(F)35x (8 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00010D _H	DMA1 - I/O register address pointer high byte	IOAH1		R/W
00010E _H	DMA1 - Data counter low byte	DCTL1	DCT1	R/W
00010F _H	DMA1 - Data counter high byte	DCTH1		R/W
000110 _H	DMA2 - Buffer address pointer low byte	BAPL2		R/W
000111 _H	DMA2 - Buffer address pointer middle byte	BAPM2		R/W
000112 _H	DMA2 - Buffer address pointer high byte	BAPH2		R/W
000113 _H	DMA2 - DMA control register	DMACS2		R/W
000114 _H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W
000115 _H	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116 _H	DMA2 - Data counter low byte	DCTL2	DCT2	R/W
000117 _H	DMA2 - Data counter high byte	DCTH2		R/W
000118 _H	DMA3 - Buffer address pointer low byte	BAPL3		R/W
000119 _H	DMA3 - Buffer address pointer middle byte	BAPM3		R/W
00011A _H	DMA3 - Buffer address pointer high byte	BAPH3		R/W
00011B _H	DMA3 - DMA control register	DMACS3		R/W
00011C _H	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
00011D _H	DMA3 - I/O register address pointer high byte	IOAH3		R/W
00011E _H	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
00011F _H	DMA3 - Data counter high byte	DCTH3		R/W
000120 _H - 00017F _H	Reserved			-
000180 _H - 00037F _H	CPU - General Purpose registers (RAM access)	GPR_RAM		R/W
000380 _H	DMA0 - Interrupt select	DISEL0		R/W
000381 _H	DMA1 - Interrupt select	DISEL1		R/W
000382 _H	DMA2 - Interrupt select	DISEL2		R/W
000383 _H	DMA3 - Interrupt select	DISEL3		R/W
000384 _H - 00038F _H	Reserved			-
000390 _H	DMA - Status register low byte	DSRL	DSR	R/W
000391 _H	DMA - Status register high byte	DSRH		R/W

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I/O map MB96(F)35x (15 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004DA _H	Peripheral Resource Relocation Register 4	PRRR4		R/W
0004DB _H	Peripheral Resource Relocation Register 5	PRRR5		R/W
0004DC _H	Peripheral Resource Relocation Register 6	PRRR6		R/W
0004DD _H	Peripheral Resource Relocation Register 7	PRRR7		R/W
0004DE _H	Peripheral Resource Relocation Register 8	PRRR8		R/W
0004DF _H	Peripheral Resource Relocation Register 9	PRRR9		R/W
0004E0 _H	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
0004E1 _H	RTC - Sub Second Register M	WTBRH0		R/W
0004E2 _H	RTC - Sub-Second Register H	WTBR1		R/W
0004E3 _H	RTC - Second Register	WTSR		R/W
0004E4 _H	RTC - Minutes	WTMR		R/W
0004E5 _H	RTC - Hour	WTHR		R/W
0004E6 _H	RTC - Timer Control Extended Register	WTCER		R/W
0004E7 _H	RTC - Clock select register	WTCKSR		R/W
0004E8 _H	RTC - Timer Control Register Low	WTCRL	WTCR	R/W
0004E9 _H	RTC - Timer Control Register High	WTCRH		R/W
0004EA _H	CAL - Calibration unit Control register	CUCR		R/W
0004EB _H	Reserved			-
0004EC _H	CAL - Duration Timer Data Register Low	CUTDL	CUTD	R/W
0004ED _H	CAL - Duration Timer Data Register High	CUTDH		R/W
0004EE _H	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
0004EF _H	CAL - Calibration Timer Register 2 High	CUTR2H		R
0004F0 _H	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
0004F1 _H	CAL - Calibration Timer Register 1 High	CUTR1H		R
0004F2 _H - 0004F9 _H	Reserved			-
0004FA _H	RLT - Timer input select (for Cascading)	TMISR		R/W
0004FB _H - 0004FF _H	Reserved			-
000500 _H	FRT2 - Data register of free-running timer		TCDT2	R/W
000501 _H	FRT2 - Data register of free-running timer			R/W

MB96350 Series

I/O map MB96(F)35x (16 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000502 _H	FRT2 - Control status register of free-running timer Low	TCCSL2	TCCS2	R/W
000503 _H	FRT2 - Control status register of free-running timer High	TCCSH2		R/W
000504 _H	FRT3 - Data register of free-running timer		TCDT3	R/W
000505 _H	FRT3 - Data register of free-running timer			R/W
000506 _H	FRT3 - Control status register of free-running timer Low	TCCSL3	TCCS3	R/W
000507 _H	FRT3 - Control status register of free-running timer High	TCCSH3		R/W
000508 _H - 000513 _H	Reserved			-
000514 _H	ICU8/ICU9 - Control Status Register	ICS89		R/W
000515 _H	ICU8/ICU9 - Edge Register	ICE89		R/W
000516 _H	ICU8 - Capture Register Low	IPCPL8	IPCP8	R
000517 _H	ICU8 - Capture Register High	IPCPH8		R
000518 _H	ICU9 - Capture Register Low	IPCPL9	IPCP9	R
000519 _H	ICU9 - Capture Register High	IPCPH9		R
00051A _H	ICU10/ICU11 - Control Status Register	ICS1011		R/W
00051B _H	ICU10/ICU11 - Edge Register	ICE1011		R/W
00051C _H	ICU10 - Capture Register Low	IPCPL10	IPCP10	R
00051D _H	ICU10 - Capture Register High	IPCPH10		R
00051E _H	ICU11 - Capture Register Low	IPCPL11	IPCP11	R
00051F _H	ICU11 - Capture Register High	IPCPH11		R
000520 _H - 00053D _H	Reserved			-
00053E _H	USART7 - Serial Mode Register	SMR7		R/W
00053F _H	USART7 - Serial Control Register	SCR7		R/W
000540 _H	USART7 - Serial TX Register	TDR7		W
000540 _H	USART7 - Serial RX Register	RDR7		R
000541 _H	USART7 - Serial Status Register	SSR7		R/W
000542 _H	USART7 - Ext. Control/Com. Register	ECCR7		R/W

MB96350 Series

I/O map MB96(F)35x (19 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00058F _H	PPG10 - Control status register High	PCNH10		R/W
000590 _H	PPG11 - Timer register		PTMR11	R
000591 _H	PPG11 - Timer register			R
000592 _H	PPG11 - Period setting register		PCSR11	W
000593 _H	PPG11 - Period setting register			W
000594 _H	PPG11 - Duty cycle register		PDUT11	W
000595 _H	PPG11 - Duty cycle register			W
000596 _H	PPG11 - Control status register Low	PCNL11	PCN11	R/W
000597 _H	PPG11 - Control status register High	PCNH11		R/W
000598 _H	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599 _H	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
00059A _H	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
00059B _H	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
00059C _H	PPG12 - Timer register		PTMR12	R
00059D _H	PPG12 - Timer register			R
00059E _H	PPG12 - Period setting register		PCSR12	W
00059F _H	PPG12 - Period setting register			W
0005A0 _H	PPG12 - Duty cycle register		PDUT12	W
0005A1 _H	PPG12 - Duty cycle register			W
0005A2 _H	PPG12 - Control status register Low	PCNL12	PCN12	R/W
0005A3 _H	PPG12 - Control status register High	PCNH12		R/W
0005A4 _H	PPG13 - Timer register		PTMR13	R
0005A5 _H	PPG13 - Timer register			R
0005A6 _H	PPG13 - Period setting register		PCSR13	W
0005A7 _H	PPG13 - Period setting register			W
0005A8 _H	PPG13 - Duty cycle register		PDUT13	W
0005A9 _H	PPG13 - Duty cycle register			W
0005AA _H	PPG13 - Control status register Low	PCNL13	PCN13	R/W
0005AB _H	PPG13 - Control status register High	PCNH13		R/W
0005AC _H	PPG14 - Timer register		PTMR14	R

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I/O map MB96(F)35x (23 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000808 _H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809 _H	CAN1 - Interrupt Register High	INTRH1		R
00080A _H	CAN1 - Test Register Low	TESTRL1	TESTR1	R/W
00080B _H	CAN1 - Test Register High (reserved)	TESTRH1		R
00080C _H	CAN1 - BRP Extension register Low	BRPERL1	BRPER1	R/W
00080D _H	CAN1 - BRP Extension register High (reserved)	BRPERH1		R
00080E _H - 00080F _H	Reserved			-
000810 _H	CAN1 - IF1 Command request register Low	IF1CREQL1	IF1CREQ1	R/W
000811 _H	CAN1 - IF1 Command request register High	IF1CREQH1		R/W
000812 _H	CAN1 - IF1 Command Mask register Low	IF1CMSKL1	IF1CMSK1	R/W
000813 _H	CAN1 - IF1 Command Mask register High (re- served)	IF1CMSKH1		R
000814 _H	CAN1 - IF1 Mask 1 Register Low	IF1MSK1L1	IF1MSK11	R/W
000815 _H	CAN1 - IF1 Mask 1 Register High	IF1MSK1H1		R/W
000816 _H	CAN1 - IF1 Mask 2 Register Low	IF1MSK2L1	IF1MSK21	R/W
000817 _H	CAN1 - IF1 Mask 2 Register High	IF1MSK2H1		R/W
000818 _H	CAN1 - IF1 Arbitration 1 Register Low	IF1ARB1L1	IF1ARB11	R/W
000819 _H	CAN1 - IF1 Arbitration 1 Register High	IF1ARB1H1		R/W
00081A _H	CAN1 - IF1 Arbitration 2 Register Low	IF1ARB2L1	IF1ARB21	R/W
00081B _H	CAN1 - IF1 Arbitration 2 Register High	IF1ARB2H1		R/W
00081C _H	CAN1 - IF1 Message Control Register Low	IF1MCTRL1	IF1MCTR1	R/W
00081D _H	CAN1 - IF1 Message Control Register High	IF1MCTRH1		R/W
00081E _H	CAN1 - IF1 Data A1 Low	IF1DTA1L1	IF1DTA11	R/W
00081F _H	CAN1 - IF1 Data A1 High	IF1DTA1H1		R/W
000820 _H	CAN1 - IF1 Data A2 Low	IF1DTA2L1	IF1DTA21	R/W
000821 _H	CAN1 - IF1 Data A2 High	IF1DTA2H1		R/W
000822 _H	CAN1 - IF1 Data B1 Low	IF1DTB1L1	IF1DTB11	R/W
000823 _H	CAN1 - IF1 Data B1 High	IF1DTB1H1		R/W
000824 _H	CAN1 - IF1 Data B2 Low	IF1DTB2L1	IF1DTB21	R/W
000825 _H	CAN1 - IF1 Data B2 High	IF1DTB2H1		R/W

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I/O map MB96(F)35x (26 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000909 _H	CAN2 - Interrupt Register High	INTRH2		R
00090A _H	CAN2 - Test Register Low	TESTRL2	TESTR2	R/W
00090B _H	CAN2 - Test Register High (reserved)	TESTRH2		R
00090C _H	CAN2 - BRP Extension register Low	BRPERL2	BRPER2	R/W
00090D _H	CAN2 - BRP Extension register High (reserved)	BRPERH2		R
00090E _H - 00090F _H	Reserved			-
000910 _H	CAN2 - IF1 Command request register Low	IF1CREQL2	IF1CREQ2	R/W
000911 _H	CAN2 - IF1 Command request register High	IF1CREQH2		R/W
000912 _H	CAN2 - IF1 Command Mask register Low	IF1CMSKL2	IF1CMSK2	R/W
000913 _H	CAN2 - IF1 Command Mask register High (re- served)	IF1CMSKH2		R
000914 _H	CAN2 - IF1 Mask 1 Register Low	IF1MSK1L2	IF1MSK12	R/W
000915 _H	CAN2 - IF1 Mask 1 Register High	IF1MSK1H2		R/W
000916 _H	CAN2 - IF1 Mask 2 Register Low	IF1MSK2L2	IF1MSK22	R/W
000917 _H	CAN2 - IF1 Mask 2 Register High	IF1MSK2H2		R/W
000918 _H	CAN2 - IF1 Arbitration 1 Register Low	IF1ARB1L2	IF1ARB12	R/W
000919 _H	CAN2 - IF1 Arbitration 1 Register High	IF1ARB1H2		R/W
00091A _H	CAN2 - IF1 Arbitration 2 Register Low	IF1ARB2L2	IF1ARB22	R/W
00091B _H	CAN2 - IF1 Arbitration 2 Register High	IF1ARB2H2		R/W
00091C _H	CAN2 - IF1 Message Control Register Low	IF1MCTRL2	IF1MCTR2	R/W
00091D _H	CAN2 - IF1 Message Control Register High	IF1MCTRH2		R/W
00091E _H	CAN2 - IF1 Data A1 Low	IF1DTA1L2	IF1DTA12	R/W
00091F _H	CAN2 - IF1 Data A1 High	IF1DTA1H2		R/W
000920 _H	CAN2 - IF1 Data A2 Low	IF1DTA2L2	IF1DTA22	R/W
000921 _H	CAN2 - IF1 Data A2 High	IF1DTA2H2		R/W
000922 _H	CAN2 - IF1 Data B1 Low	IF1DTB1L2	IF1DTB12	R/W
000923 _H	CAN2 - IF1 Data B1 High	IF1DTB1H2		R/W
000924 _H	CAN2 - IF1 Data B2 Low	IF1DTB2L2	IF1DTB22	R/W
000925 _H	CAN2 - IF1 Data B2 High	IF1DTB2H2		R/W

MB96350 Series

I/O map MB96(F)35x (28 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000984 _H - 00098F _H	Reserved			-
000990 _H	CAN2 - New Data 1 Register Low	NEWDT1L2	NEWDT12	R
000991 _H	CAN2 - New Data 1 Register High	NEWDT1H2		R
000992 _H	CAN2 - New Data 2 Register Low	NEWDT2L2	NEWDT22	R
000993 _H	CAN2 - New Data 2 Register High	NEWDT2H2		R
000994 _H - 00099F _H	Reserved			-
0009A0 _H	CAN2 - Interrupt Pending 1 Register Low	INTPND1L2	INTPND12	R
0009A1 _H	CAN2 - Interrupt Pending 1 Register High	INTPND1H2		R
0009A2 _H	CAN2 - Interrupt Pending 2 Register Low	INTPND2L2	INTPND22	R
0009A3 _H	CAN2 - Interrupt Pending 2 Register High	INTPND2H2		R
0009A4 _H - 0009AF _H	Reserved			-
0009B0 _H	CAN2 - Message Valid 1 Register Low	MSGVAL1L2	MSGVAL12	R
0009B1 _H	CAN2 - Message Valid 1 Register High	MSGVAL1H2		R
0009B2 _H	CAN2 - Message Valid 2 Register Low	MSGVAL2L2	MSGVAL22	R
0009B3 _H	CAN2 - Message Valid 2 Register High	MSGVAL2H2		R
0009B4 _H - 0009CD _H	Reserved			-
0009CE _H	CAN2 - Output enable register	COER2		R/W
0009CF _H - 000BFF _H	Reserved			-

Note: Any write access to reserved addresses in the I/O map should not be performed. A read access to a reserved address results in reading 'X'.
Registers of resources which are described in this table, but which are not supported by the device, should also be handled as "Reserved".

■ HANDLING DEVICES

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Serial communication

1. Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

2. Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register $PIER = 0$).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 k Ω .

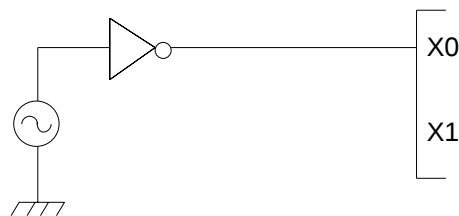
Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

3. External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

1. Single phase external clock

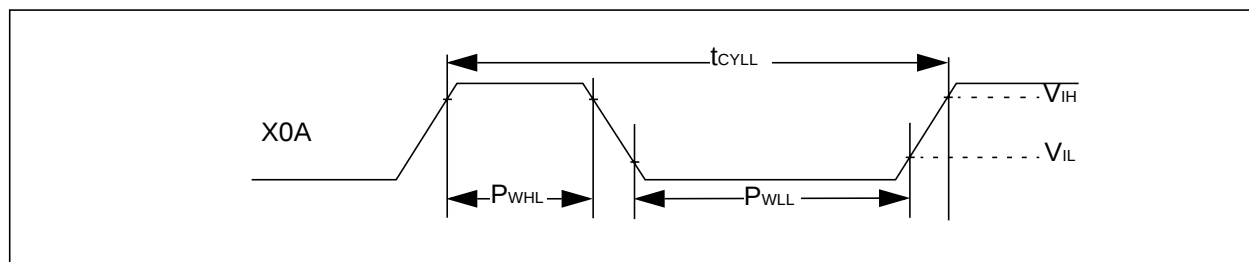
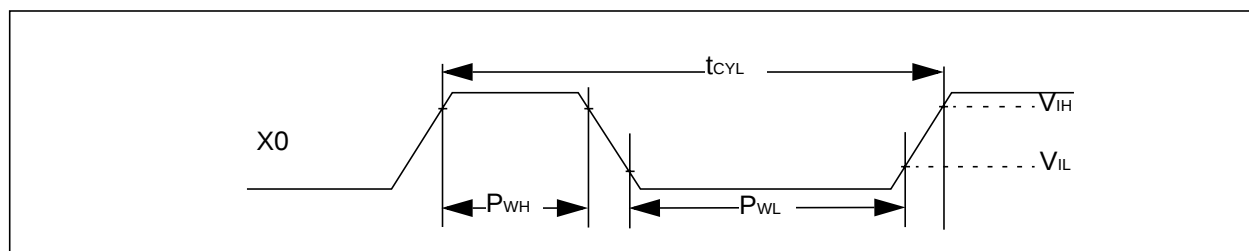
- When using a single phase external clock, X0 (X0A) pin must be driven and X1 (X1A) pin left open.



MB96350 Series

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T _A)		Value			Remarks	
				Typ	Max	Unit		
Power supply current in Run modes*	I _{CCMAIN}	Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz	+25°C	4	5	mA	MB96F353/F355	
			+125°C	4.7	8			
		1 Flash/ROM wait state (CLKPLL, CLKSC and CLKRC stopped)	+25°C	4.2	5.2	mA	MB96F356	
			+125°C	4.9	8.2			
	I _{CCRCH}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 2MHz	+25°C	2.5	3.5	mA	MB96F353/F355	
			+125°C	3.2	6.5			
		1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped)	+25°C	2.7	3.7	mA	MB96F356	
			+125°C	3.4	6.7			
	I _{CCRCL}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 0	+25°C	0.18	0.3	mA	MB96F353/F355	
			+125°C	0.73	3.1			
		1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.4	0.6	mA	MB96F356	
			+125°C	0.95	3.4			
		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 1	+25°C	0.15	0.25	mA	MB96F353/F355/ F356	
			+125°C	0.7	3.05			
		I _{CCSUB}	Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz	+25°C	0.1	0.2	mA	MB96F353/F355/ F356
				+125°C	0.65	3		
		1 Flash/ROM wait state (CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing al- lowed)	+25°C			mA		
			+125°C					

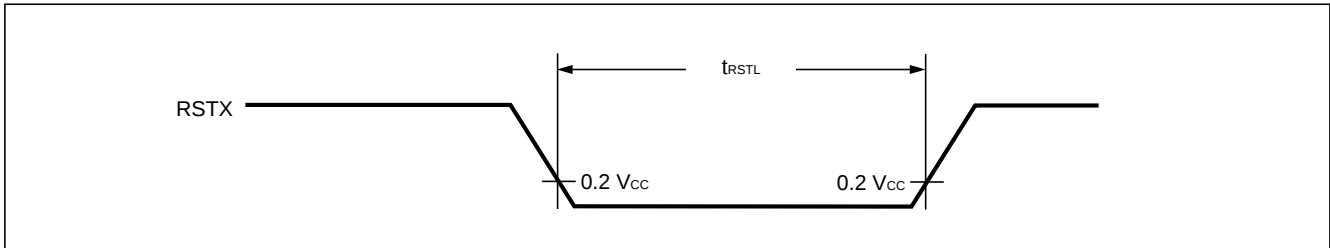


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External Reset timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Reset input time	t _{RSTL}	RSTX	500	-	-	ns	



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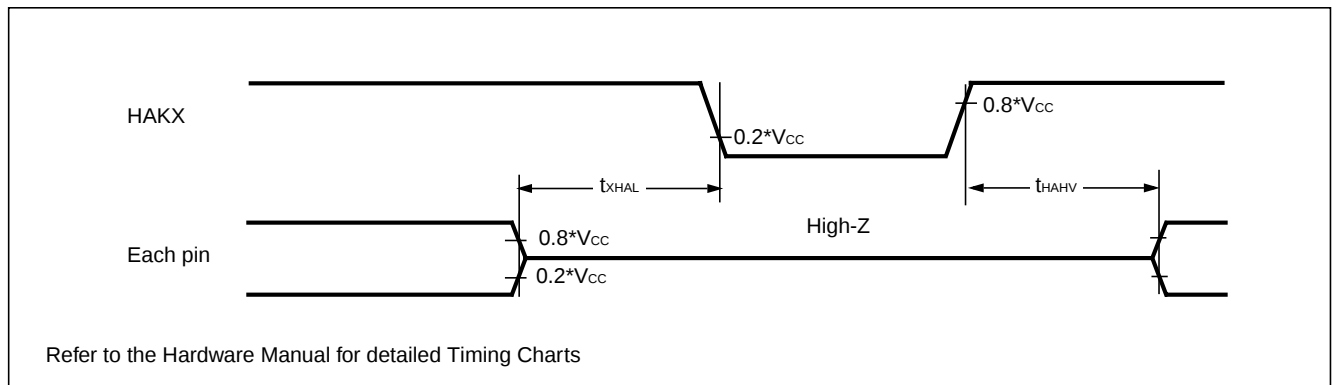
($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{ mA}$, $C_L = 50\text{ pF}$)

Parameter	Sym- bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Address valid $\Rightarrow$ Data hold time	t_{AXDX}	A[23:16], AD[15:0]	—	0	—	ns	
RDX $\uparrow \Rightarrow$ ALE $\uparrow$ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 10$	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 10$	—		
Valid address $\Rightarrow$ ECLK $\uparrow$ time	t_{AVCH}	A[23:16], ECLK	—	$t_{CYC} - 15$	—	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 15$	—		
RDX $\downarrow \Rightarrow$ ECLK $\uparrow$ time	t_{RLCH}	RDX, ECLK	—	$t_{CYC}/2 - 10$	—	ns	
ALE $\downarrow \Rightarrow$ RDX $\downarrow$ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 10$	—	ns	
			EACL:STS=1	- 10	—		
ECLK $\uparrow \Rightarrow$ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	$t_{CYC} - 50$	ns	

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5 V , $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{ mA}$, $C_L = 50\text{ pF}$)

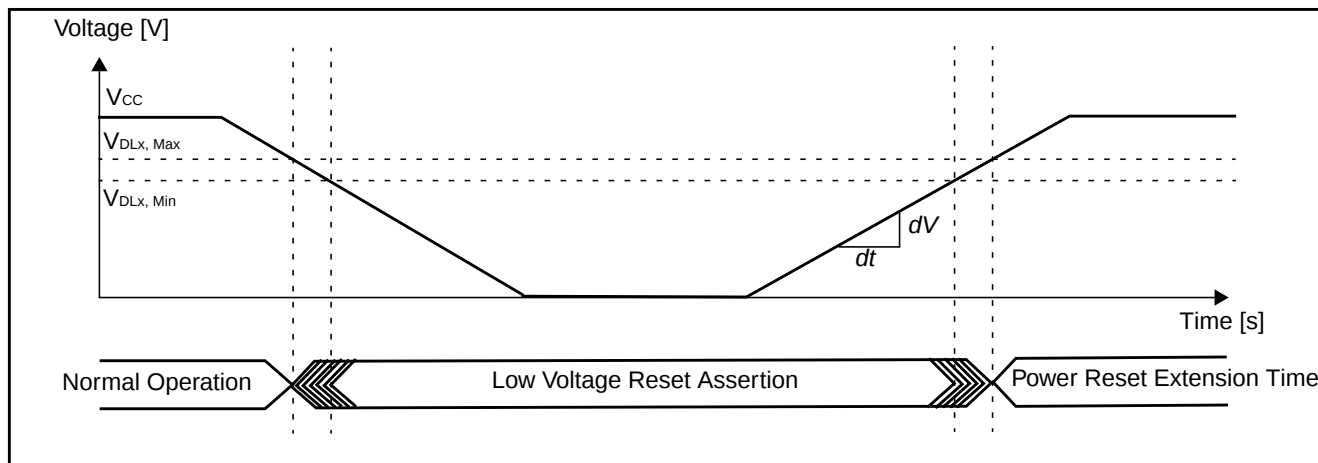
Parameter	Sym- bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t _{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	t _{CYC} /2 – 8	—	ns	
			EACL:STS=1	t _{CYC} – 8	—		
			EACL:STS=0 and EACL:ACE=1	3t _{CYC} /2 – 8	—		
Valid address ⇒ ALE ↓ time	t _{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	t _{CYC} – 20	—	ns	
			EACL:STS=1 and EACL:ACE=0	3t _{CYC} /2 – 20	—		
			EACL:STS=0 and EACL:ACE=1	2t _{CYC} – 20	—		
			EACL:STS=1 and EACL:ACE=1	5t _{CYC} /2 – 20	—		
	t _{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	t _{CYC} /2 – 20	—	ns	
			EACL:STS=1 and EACL:ACE=0	t _{CYC} – 20	—		
			EACL:STS=0 and EACL:ACE=1	3t _{CYC} /2 – 20	—		
			EACL:STS=1 and EACL:ACE=1	2t _{CYC} – 20	—		
ALE ↓ ⇒ Address valid time	t _{LLAX}	ALE, AD[15:0]	EACL:STS=0	t _{CYC} /2 – 20	—	ns	
			EACL:STS=1	-20	—		

MB96350 Series



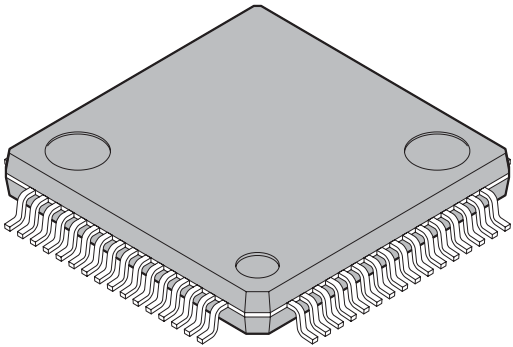
Low Voltage Detector Operation

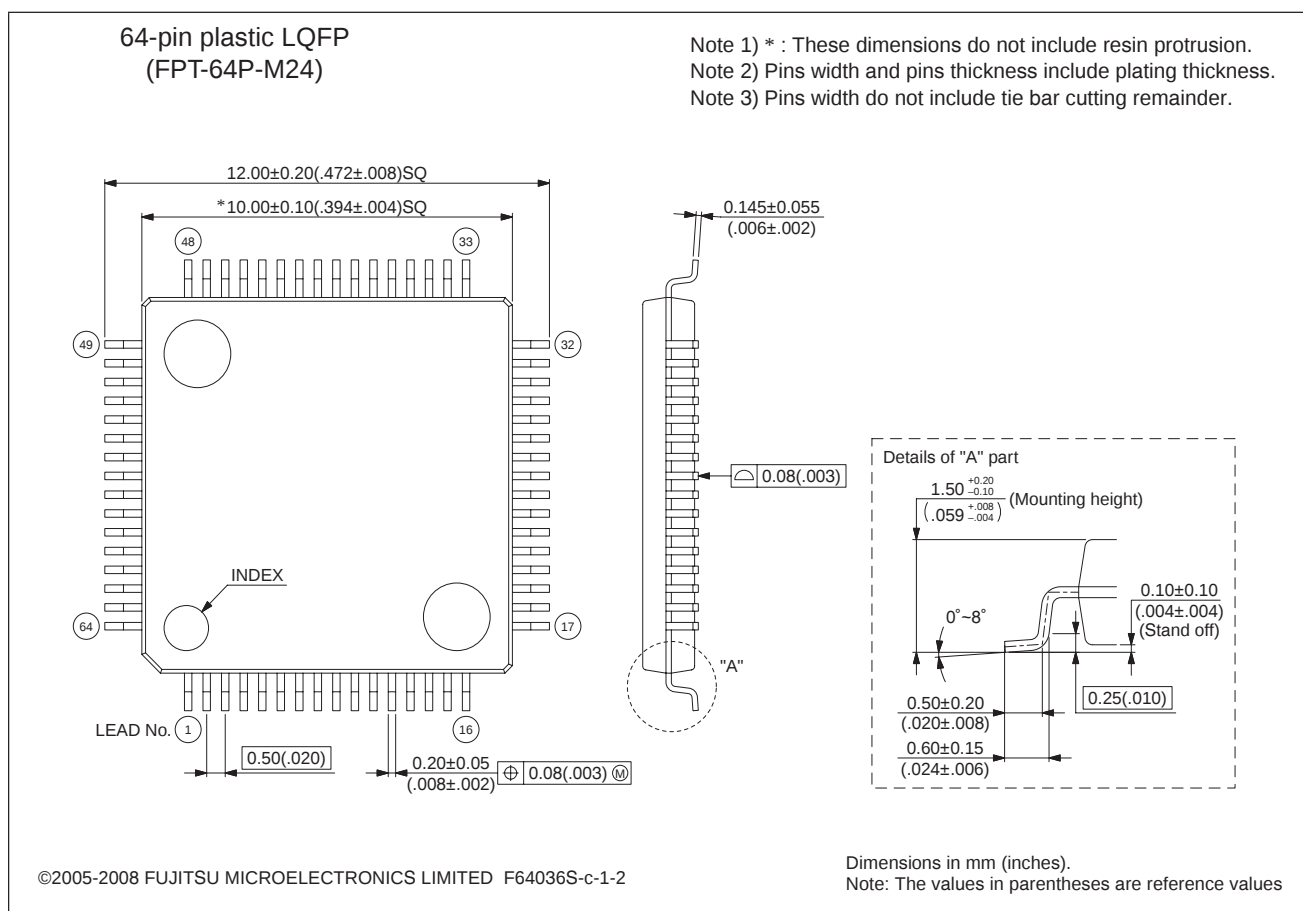
In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.



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■ PACKAGE DIMENSION MB96(F)35x LQFP 64 - M24

 64-pin plastic LQFP (FPT-64P-M24)	Lead pitch	0.50 mm
	Package width × package length	10.0 × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
	Code (Reference)	P-LFQFP64-10×10-0.50



Please check the latest package dimension at the following URL.
<http://edevic.fujitsu.com/package/en-search/>