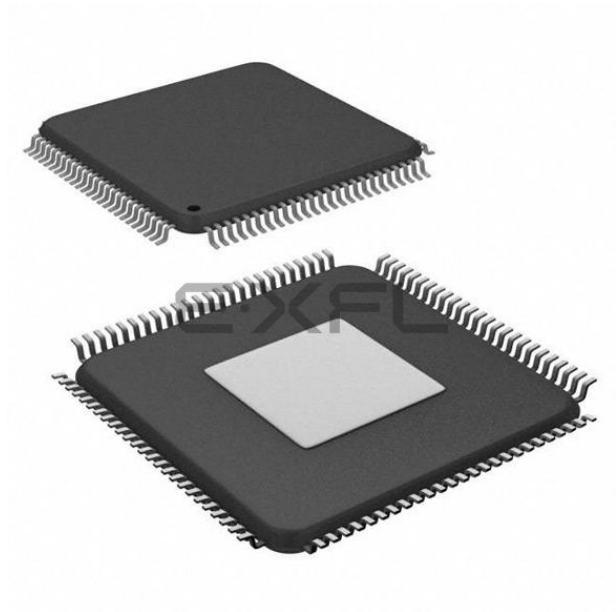

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	18K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xc2364b-24f40l

16/32-Bit Single-Chip Microcontroller
with 32-Bit Performance

XC236xB (XC2000 Family)

1 Summary of Features

For a quick overview and easy reference, the features of the XC236xB are summarized here.

- High-performance CPU with five-stage pipeline and MPU
  - 12.5 ns instruction cycle @ 80 MHz CPU clock (single-cycle execution)
  - One-cycle 32-bit addition and subtraction with 40-bit result
  - One-cycle multiplication (16 × 16 bit)
  - Background division (32 / 16 bit) in 21 cycles
  - One-cycle multiply-and-accumulate (MAC) instructions
  - Enhanced Boolean bit manipulation facilities
  - Zero-cycle jump execution
  - Additional instructions to support HLL and operating systems
  - Register-based design with multiple variable register banks
  - Fast context switching support with two additional local register banks
  - 16 Mbytes total linear address space for code and data
  - 1,024 Bytes on-chip special function register area (C166 Family compatible)
  - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels providing 96 interrupt nodes
  - Selectable external inputs for interrupt generation and wake-up
  - Fastest sample-rate 12.5 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
  - 8 Kbytes on-chip stand-by RAM (SBRAM)
  - 2 Kbytes on-chip dual-port RAM (DPRAM)
  - Up to 16 Kbytes on-chip data SRAM (DSRAM)
  - Up to 16 Kbytes on-chip program/data SRAM (PSRAM)
  - Up to 320 Kbytes on-chip program memory (Flash memory)
  - Memory content protection through Error Correction Code (ECC)

3.17 Clock Generation

The Clock Generation Unit can generate the system clock signal f_{SYS} for the XC236xB from a number of external or internal clock sources:

- External clock signals with pad voltage or core voltage levels
- External crystal or resonator using the on-chip oscillator
- On-chip clock source for operation without crystal/resonator
- Wake-up clock (ultra-low-power) to further reduce power consumption

The programmable on-chip PLL with multiple prescalers generates a clock signal for maximum system performance from standard crystals, a clock input signal, or from the on-chip clock source. See also Section 4.7.2 .

The Oscillator Watchdog (OWD) generates an interrupt if the crystal oscillator frequency falls below a certain limit or stops completely. In this case, the system can be supplied with an emergency clock to enable operation even after an external clock failure.

All available clock signals can be output on one of two selectable pins.

4.1.1 Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XC236xB. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Note: Typical parameter values refer to room temperature and nominal supply voltage, minimum/maximum parameter values also include conditions of minimum/maximum temperature and minimum/maximum supply voltage. Additional details are described where applicable.

Table 13 Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage Regulator Buffer Capacitance for DMP_M	C_{EVRM} SR	1.0		4.7	nF	1)
Voltage Regulator Buffer Capacitance for DMP_1	C_{EVR1} SR	0.47		2.2	nF	2)1)
External Load Capacitance	C_L SR		20[3)]		pF	pin out driver= default 4)
System frequency	f_{SYS} SR			80	MHz	5)
Overload current for analog inputs[6)]	I_{OVA} SR	-2		5	mA	not subject to production test
Overload current for digital inputs[6)]	I_{OVD} SR	-5		5	mA	not subject to production test
Overload current coupling factor for analog inputs[7)]	K_{OVA} CC		2.5×10^{-4}	1.5×10^{-3}	-	I_{OV}< 0 mA; not subject to production test
			1.0×10^{-6}	1.0×10^{-4}	-	I_{OV}> 0 mA; not subject to production test

Table 13 Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload current coupling factor for digital I/O pins	K_{OVD} CC		1.0×10^{-2}	3.0×10^{-2}	-	$I_{OV} < 0$ mA; not subject to production test
			1.0×10^{-4}	5.0×10^{-3}	-	$I_{OV} > 0$ mA; not subject to production test
Absolute sum of overload currents	$\sum\lvert I_{OV}\rvert$ SR			50	mA	not subject to production test
Digital core supply voltage for domain M[8)]	V_{DDIM} CC		1.5			
Digital core supply voltage for domain 1[8)]	V_{DDI1} CC		1.5			
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	3.0		5.5	V	
Digital ground voltage	V_{SS} SR		0		V	

1) To ensure the stability of the voltage regulators the EVRs must be buffered with ceramic capacitors. Separate buffer capacitors with the recomended values shall be connected as close as possible to each V_{DDIM} and V_{DDI1} pin to keep the resistance of the board tracks below 2 Ohm. Connect all V_{DDI1} pins together. The minimum capacitance value is required for proper operation under all conditions (e.g. temperature). Higher values slightly increase the startup time.

2) Use one Capacitor for each pin.

3) This is the reference load. For bigger capacitive loads, use the derating factors listed in the pad properties section.

4) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).

5) The operating frequency range may be reduced for specific device types. This is indicated in the device designation (...FxxL). 80 MHz devices are marked ...F80L.

6) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{IHmax}$ ($I_{OV} > 0$) or $V_{OV} < V_{ILmin}$ ($(I_{OV} < 0)$. The absolute sum of input overload currents on all pins may not exceed 50 mA. The supply voltages must remain within the specified limits. Proper operation under overload conditions depends on the application. Overload conditions must not occur on pin XTAL1 (powered by V_{DDIM}).

7) An overload current (I_{OV}) through a pin injects a certain error current (I_{INJ}) into the adjacent pins. This error current adds to the respective pins leakage current (I_{OZ}). The amount of error current depends on the overload current and is defined by the overload coupling factor K_{OV}. The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it.The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \ K_{OV})$. The additional error current may distort the input voltage on analog inputs.

8) Value is controlled by on-chip regulator

4.2 Voltage Range definitions

The XC236xB timing depends on the supply voltage. If such a dependency exists the timing values are given for 2 voltage areas commonly used. The voltage areas are defined in the following tables.

Table 14 Upper Voltage Range Definition

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	4.5	5	5.5	V	

Table 15 Lower Voltage Range Definition

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	3.0	3.3	4.5	V	

4.2.1 Parameter Interpretation

The parameters listed in the following include both the characteristics of the XC236xB and its demands on the system. To aid in correctly interpreting the parameters when evaluating them for a design, they are marked accordingly in the column “Symbol”:

CC (Controller Characteristics):
The logic of the XC236xB provides signals with the specified characteristics.

SR (System Requirement):
The external system must provide signals with the specified characteristics to the XC236xB.

4.3.2 DC Parameters for Lower Voltage Area

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Note: Operating Conditions apply.

Table 17 is valid under the following conditions: V_{DDP} t 3.0 V; V_{DDP}typ. 3.3 V; V_{DDP} d4.5 V

Table 17 DC Characteristics for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs). To be doubled for double bond pins.[1)]	C_{IO} CC			10	pF	not subject to production test
Input Hysteresis[2)]	HYS CC	0.07 x V_{DDP}			V	R_S= 0 Ohm
Absolute input leakage current on pins of analog ports[3)]	$\|I_{OZ1}\|$ CC		10	200	nA	V_{IN}> V_{SS} ; V_{IN}< V_{DDP}
Absolute input leakage current for all other pins. To be doubled for double bond pins.[3)1)4)]	$\|I_{OZ2}\|$ CC		0.2	2.5	µA	T_J d110 °C; V_{IN}> V_{SS} ; V_{IN}< V_{DDP}
			0.2	8	µA	T_J d150 °C; V_{IN}> V_{SS} ; V_{IN}< V_{DDP}
Pull Level Force Current[5)]	$\|I_{PLF}\|$ SR	150			A	V_{IN} t V_{IHmin}(pull P down); V_{IN} dV_{ILmax}(pull up)
Pull Level Keep Current[6)]	$\|I_{PLK}\|$ SR			10	µA	V_{IN} t V_{IHmin}(pull up) ; V_{IN} dV_{ILmax}(pull down)
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 x V_{DDP}		V_{DDP} + 0.3	V	
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3		0.3 x V_{DDP}	V	

Table 18 Switching Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power supply current (active) with all peripherals active and EVVRs on	I_{SACT} CC		6 + 0.6 x f_{SYS} [1]	8 + 1.0 x f_{SYS} [1]	mA	power_mode= active ; voltage_range= both [2][3][4]
Power supply current in stopover mode, EVVRs on	I_{SSO} CC		0.7	2.0	mA	power_mode= stopover ; voltage_range= both [4]

1) f_{SYS} in MHz

2) The pad supply voltage pins (V_{DDPB}) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers input stages are switched. In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to 3 + 0.6 x f_{SYS}.

3) Please consider the additional conditions described in section "Active Mode Power Supply Current".

4) The pad supply voltage has only a minor influence on this parameter.

Active Mode Power Supply Current

The actual power supply current in active mode not only depends on the system frequency but also on the configuration of the XC236xB's subsystem.

Besides the power consumed by the device logic the power supply pins also provide the current that flows through the pin output drivers.
A small current is consumed because the drivers' input stages are switched.

The IO power domains can be supplied separately. Power domain A (V_{DDPA}) supplies the A/D converters and Port 6. Power domain B (V_{DDPB}) supplies the on-chip EVVRs and all other ports.
During operation domain A draws a maximum current of 1.5 mA for each active A/D converter module from V_{DDPA}.

In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to 3 + 0.6 ƒ$_{SYS}$ mA.

4.6 Flash Memory Parameters

The XC236xB is delivered with all Flash sectors erased and with no protection installed.

The data retention time of the XC236xB's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 25 Flash Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Parallel Flash module program/erase limit depending on Flash read activity	N_{PP} SR					

4.7 AC Parameters

These parameters describe the dynamic behavior of the XC236xB.

4.7.1 Testing Waveforms

These values are used for characterization and production testing (except pin XTAL1).

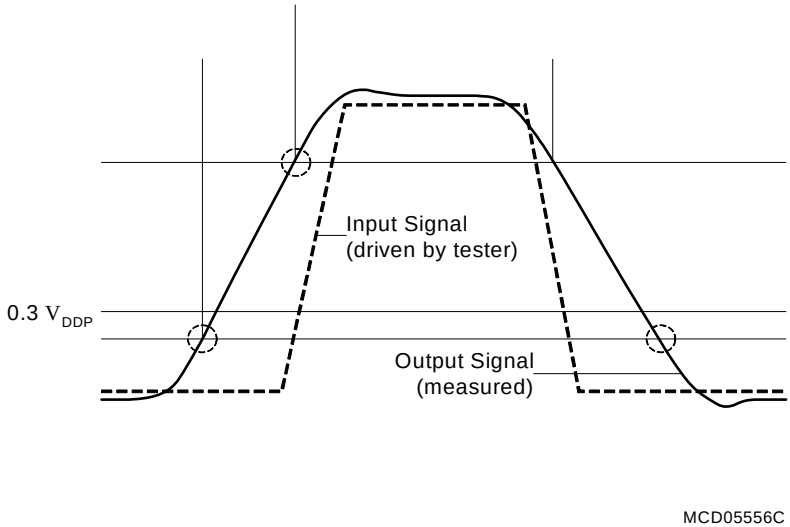

Figure 17 Input Output Waveforms

Figure 18 Floating Waveforms