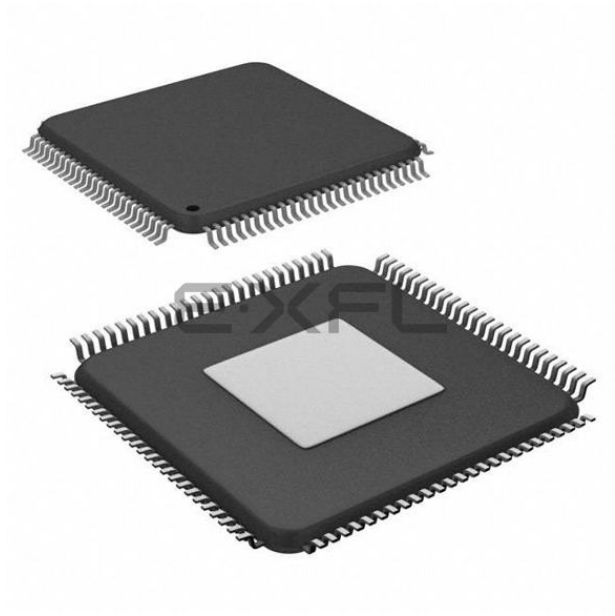
Infineon Technologies - XC2361B24F66LAAHXUMA1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 110°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2361b24f66laahxuma1

Table of Contents

- On-Chip Peripheral Modules
  - Two synchronizable A/D Converters with up to 16 channels, 10-bit resolution, conversion time below 1 µs, optional data preprocessing (data reduction, range check), broken wire detection
  - 16-channel general purpose capture/compare unit (CC2)
  - Two capture/compare units for flexible PWM signal generation (CCU6x)
  - Multi-functional general purpose timer unit with 5 timers
  - Up to 6 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
  - On-chip MultiCAN interface (Rev. 2.0B active) with 64 message objects (Full CAN/Basic CAN) on up to 3 CAN nodes and gateway functionality
  - On-chip system timer and on-chip real time clock
- Up to 12 Mbytes external address space for code and data
  - Programmable external bus characteristics for different address ranges
  - Multiplexed or demultiplexed external address/data buses
  - Selectable address bus width
  - 16-bit or 8-bit data bus width
  - Four programmable chip-select signals
- Single power supply from 3.0 V to 5.5 V
- Power reduction and wake-up modes
- Programmable watchdog timer and oscillator watchdog
- Up to 76 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via Device Access Port (DAP) or JTAG interface
- 100-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

1.3 Definition of Feature Variants

The XC236xB types are offered with several Flash memory sizes. **Table 3** and **Table 4** describe the location of the available Flash memory.

Table 3 Continuous Flash Memory Ranges

Total Flash Size	1st Range[1)]	2nd Range	3rd Range
320 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C4'FFFF_H$	n.a.
192 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C1'FFFF_H$	$C4'0000_H$ … $C4'FFFF_H$

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

Table 4 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0[1)]	Flash 1
320	256	64
192	128	64

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XC236xB types are offered with different interface options. **Table 5** lists the available channels for each option.

Table 5 Interface Channel Association

Total Number	Available Channels / Message Objects
11 ADC0 channels	CH0, CH2 … CH5, CH8 … CH11, CH13, CH15
4 ADC0 channels	CH0, CH2 … CH4
5 ADC1 channels	CH0, CH2, CH4 … CH6
4 ADC1 channels	CH0, CH2, CH4, CH5
2 CAN nodes	CAN0, CAN1 64 message objects
3 CAN nodes	CAN0, CAN1, CAN2 64 message objects
2 serial channels	U0C0, U0C1
4 serial channels	U0C0, U0C1, U1C0, U1C1
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
42	P4.0	O0 / I	St/B	**Bit 0 of Port 4, General Purpose Input/Output**
	CC2_CC24	O3 / I	St/B	**CAPCOM2 CC24IO Capture Inp./ Compare Out.**
	$\overline{\text{CS0}}$	OH	St/B	**External Bus Interface Chip Select 0 Output**
43	P2.3	O0 / I	St/B	**Bit 3 of Port 2, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CC2_CC16	O3 / I	St/B	**CAPCOM2 CC16IO Capture Inp./ Compare Out.**
	A16	OH	St/B	**External Bus Interface Address Line 16**
	ESR2_0	I	St/B	**ESR2 Trigger Input 0**
	U0C0_DX0E	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0D	I	St/B	**USIC0 Channel 1 Shift Data Input**
	RxDC0A	I	St/B	**CAN Node 0 Receive Data Input**
44	P4.1	O0 / I	St/B	**Bit 1 of Port 4, General Purpose Input/Output**
	TxDC2	O2	St/B	**CAN Node 2 Transmit Data Output**
	CC2_CC25	O3 / I	St/B	**CAPCOM2 CC25IO Capture Inp./ Compare Out.**
	$\overline{\text{CS1}}$	OH	St/B	**External Bus Interface Chip Select 1 Output**
	T4EUDB	I	St/B	**GPT12E Timer T4 External Up/Down Control Input**
	ESR1_8	I	St/B	**ESR1 Trigger Input 8**
45	P2.4	O0 / I	St/B	**Bit 4 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CC2_CC17	O3 / I	St/B	**CAPCOM2 CC17IO Capture Inp./ Compare Out.**
	A17	OH	St/B	**External Bus Interface Address Line 17**
	ESR1_0	I	St/B	**ESR1 Trigger Input 0**
	U0C0_DX0F	I	St/B	**USIC0 Channel 0 Shift Data Input**
	RxDC1A	I	St/B	**CAN Node 1 Receive Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
67	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COUT60	O2	St/B	**CCU60 Channel 0 Output**
	AD3	OH / IH	St/B	**External Bus Interface Address/Data Line 3**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
68	P0.5	O0 / I	St/B	**Bit 5 of Port 0, General Purpose Input/Output**
	U1C1_SCLKOUT	O1	St/B	**USIC1 Channel 1 Shift Clock Output**
	U1C0_SELO2	O2	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	CCU61_COUT62	O3	St/B	**CCU61 Channel 2 Output**
	A5	OH	St/B	**External Bus Interface Address Line 5**
	U1C1_DX1A	I	St/B	**USIC1 Channel 1 Shift Clock Input**
	U1C0_DX1C	I	St/B	**USIC1 Channel 0 Shift Clock Input**
69	P10.4	O0 / I	St/B	**Bit 4 of Port 10, General Purpose Input/Output**
	U0C0_SELO3	O1	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CCU60_COUT61	O2	St/B	**CCU60 Channel 1 Output**
	AD4	OH / IH	St/B	**External Bus Interface Address/Data Line 4**
	U0C0_DX2B	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2B	I	St/B	**USIC0 Channel 1 Shift Control Input**
	ESR1_9	I	St/B	**ESR1 Trigger Input 9**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
87	P1.3	O0 / I	St/B	**Bit 3 of Port 1, General Purpose Input/Output**
	U1C0_SELO 7	O2	St/B	**USIC1 Channel 0 Select/Control 7 Output**
	U2C0_SELO 4	O3	St/B	**USIC2 Channel 0 Select/Control 4 Output**
	A11	OH	St/B	**External Bus Interface Address Line 11**
	ESR2_4	I	St/B	**ESR2 Trigger Input 4**
89	P10.14	O0 / I	St/B	**Bit 14 of Port 10, General Purpose Input/Output**
	U1C0_SELO 1	O1	St/B	**USIC1 Channel 0 Select/Control 1 Output**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	$\overline{RD}$	OH	St/B	**External Bus Interface Read Strobe Output**
	ESR2_2	I	St/B	**ESR2 Trigger Input 2**
	U0C1_DX0C	I	St/B	**USIC0 Channel 1 Shift Data Input**
90	P1.4	O0 / I	St/B	**Bit 4 of Port 1, General Purpose Input/Output**
	U1C1_SELO 4	O2	St/B	**USIC1 Channel 1 Select/Control 4 Output**
	U2C0_SELO 5	O3	St/B	**USIC2 Channel 0 Select/Control 5 Output**
	A12	OH	St/B	**External Bus Interface Address Line 12**
	U2C0_DX2B	I	St/B	**USIC2 Channel 0 Shift Control Input**
91	P10.15	O0 / I	St/B	**Bit 15 of Port 10, General Purpose Input/Output**
	U1C0_SELO 2	O1	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U1C0_DOUT	O3	St/B	**USIC1 Channel 0 Shift Data Output**
	ALE	OH	St/B	**External Bus Interf. Addr. Latch Enable Output**
	U0C1_DX1C	I	St/B	**USIC0 Channel 1 Shift Clock Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
98	$\overline{\text{ESR1}}$	O0 / I	St/B	**External Service Request 1** After power-up, an internal weak pull-up device holds this pin high when nothing is driving it.
	RxDC0E	I	St/B	**CAN Node 0 Receive Data Input**
	U1C0_DX0F	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2C	I	St/B	**USIC1 Channel 0 Shift Control Input**
	U1C1_DX0C	I	St/B	**USIC1 Channel 1 Shift Data Input**
	U1C1_DX2B	I	St/B	**USIC1 Channel 1 Shift Control Input**
	U2C1_DX2C	I	St/B	**USIC2 Channel 1 Shift Control Input**
99	$\overline{\text{ESR0}}$	O0 / I	St/B	**External Service Request 0** After power-up, $\overline{\text{ESR0}}$ operates as open-drain bidirectional reset with a weak pull-up.
	U1C0_DX0E	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2B	I	St/B	**USIC1 Channel 0 Shift Control Input**
10	V_{DDIM}	-	PS/M	**Digital Core Supply Voltage for Domain M** Decouple with a ceramic capacitor, see Data Sheet for details.
38, 64, 88	V_{DDI1}	-	PS/1	**Digital Core Supply Voltage for Domain 1** Decouple with a ceramic capacitor, see Data Sheet for details. All V_{DDI1} pins must be connected to each other.
14	V_{DDPA}	-	PS/A	**Digital Pad Supply Voltage for Domain A** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The A/D_Converters and ports P5, P6 and P15 are fed from supply voltage V_{DDPA}.*

3 Functional Description

The architecture of the XC236xB combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources. This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XC236xB.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XC236xB.

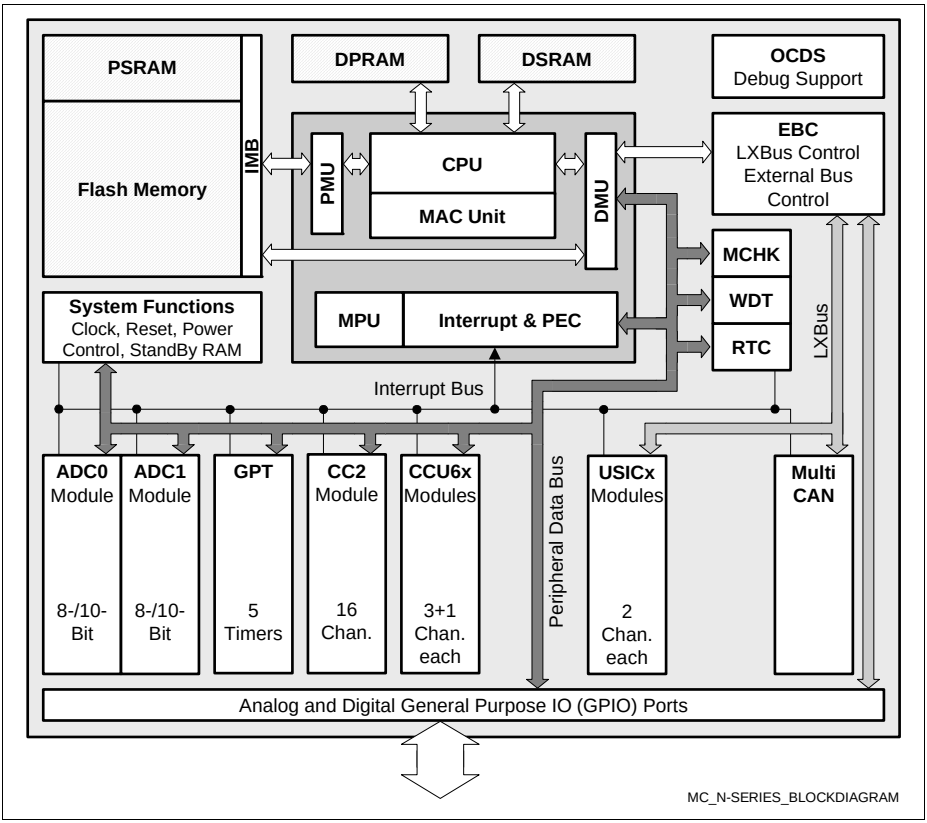

Figure 4 Block Diagram

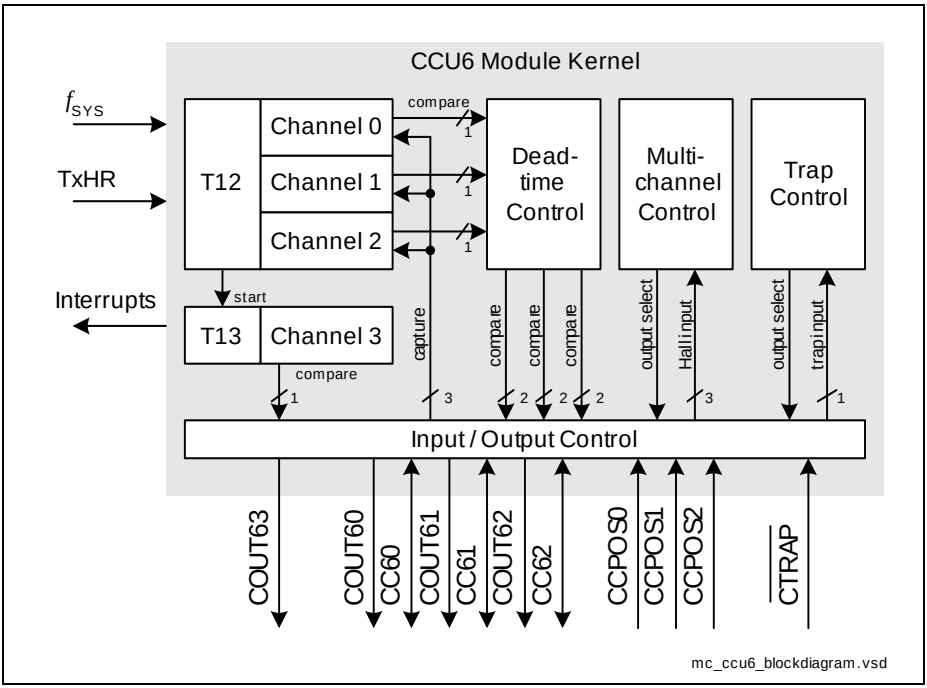

Figure 7 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

3.10 General Purpose Timer (GPT12E) Unit

The GPT12E unit is a very flexible multifunctional timer/counter structure which can be used for many different timing tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers organized in two separate modules, GPT1 and GPT2. Each timer in each module may either operate independently in a number of different modes or be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation: Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock and divided by a programmable prescaler. Counter Mode allows timer clocking in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes each timer has one associated port pin (TxIN) which serves as a gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The counting direction (up/down) for each timer can be programmed by software or altered dynamically by an external signal on a port pin (TxEUD), e.g. to facilitate position tracking.

In Incremental Interface Mode the GPT1 timers can be directly connected to the incremental position sensor signals A and B through their respective inputs TxIN and TxEUD. Direction and counting signals are internally derived from these two input signals, so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to the basic operating modes, T2 and T4 may be configured as reload or capture register for timer T3. A timer used as capture or reload register is stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at the associated input pin (TxIN). Timer T3 is reloaded with the contents of T2 or T4, triggered either by an external signal or a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be continuously generated without software intervention.

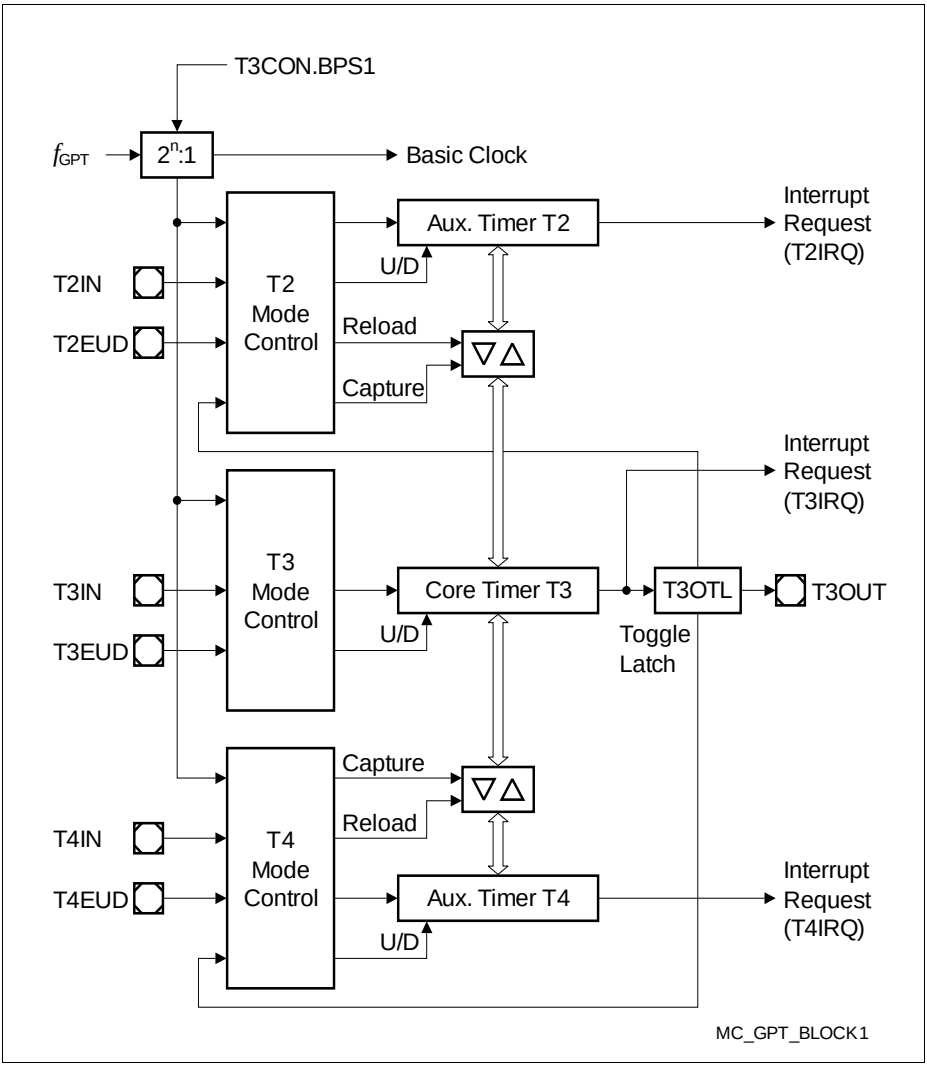

Figure 8 Block Diagram of GPT1

MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Independent CAN nodes
- Set of independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

3.15 System Timer

The System Timer consists of a programmable prescaler and two concatenated timers (10 bits and 6 bits). Both timers can generate interrupt requests. The clock source can be selected and the timers can also run during power reduction modes.

Therefore, the System Timer enables the software to maintain the current time for scheduling functions or for the implementation of a clock.

3.16 Watchdog Timer

The Watchdog Timer is one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after an application reset of the chip. It can be disabled and enabled at any time by executing the instructions DISWDT and ENWDT respectively. The software has to service the Watchdog Timer before it overflows. If this is not the case because of a hardware or software failure, the Watchdog Timer overflows, generating a prewarning interrupt and then a reset request.

The Watchdog Timer is a 16-bit timer clocked with the system clock divided by 16,384 or 256. The Watchdog Timer register is set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the Watchdog Timer is reloaded and the prescaler is cleared.

Time intervals between 3.2 µs and 13.4 s can be monitored (@ 80 MHz).

The default Watchdog Timer interval after power-up is 6.5 ms (@ 10 MHz).

Table 13 Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload current coupling factor for digital I/O pins	K_{OVD} CC	–	1.0 x 10^{-2}	3.0 x 10^{-2}	-	I_{OV}< 0 mA; not subject to production test
		–	1.0 x 10^{-4}	5.0 x 10^{-3}	-	I_{OV}> 0 mA; not subject to production test
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$ SR	–	–	50	mA	not subject to production test
Digital core supply voltage for domain M[8)]	V_{DDIM} CC	–	1.5	–		
Digital core supply voltage for domain 1[8)]	V_{DDI1} CC	–	1.5	–		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	3.0	–	5.5	V	
Digital ground voltage	V_{SS} SR	–	0	–	V	

1) To ensure the stability of the voltage regulators the EVRs must be buffered with ceramic capacitors. Separate buffer capacitors with the recomended values shall be connected as close as possible to each V_{DDIM} and V_{DDI1} pin to keep the resistance of the board tracks below 2 Ohm. Connect all V_{DDI1} pins together. The minimum capacitance value is required for proper operation under all conditions (e.g. temperature). Higher values slightly increase the startup time.

2) Use one Capacitor for each pin.

3) This is the reference load. For bigger capacitive loads, use the derating factors listed in the pad properties section.

4) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).

5) The operating frequency range may be reduced for specific device types. This is indicated in the device designation (...FxxL). 80 MHz devices are marked ...F80L.

6) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{IHmax}$ ($I_{OV} > 0$) or $V_{OV} < V_{ILmin}$ (($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed 50 mA. The supply voltages must remain within the specified limits. Proper operation under overload conditions depends on the application. Overload conditions must not occur on pin XTAL1 (powered by V_{DDIM}).

Pullup/Pulldown Device Behavior

Most pins of the XC236xB feature pullup or pulldown devices. For some special pins these are fixed; for the port pins they can be selected by the application.

The specified current values indicate how to load the respective pin depending on the intended signal level. **Figure 13** shows the current paths.

The shaded resistors shown in the figure may be required to compensate system pull currents that do not match the given limit values.

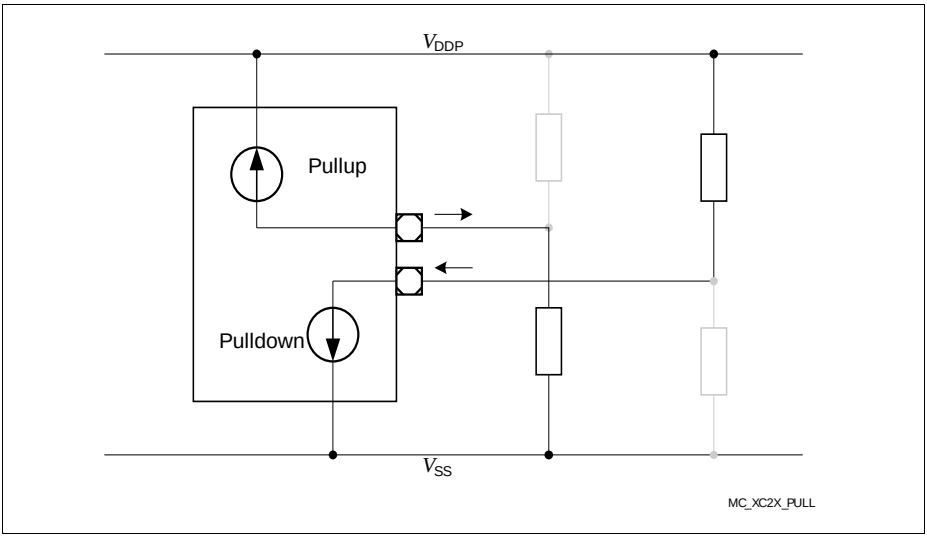

Figure 13 Pullup/Pulldown Current Definition

Table 17 DC Characteristics for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output High voltage[7]	V_{OH} CC	V_{DDP} - 1.0	–	–	V	$I_{OH} \geq I_{OHmax}$
		V_{DDP} - 0.4	–	–	V	$I_{OH} \geq I_{OHnom}$ [8]
Output Low Voltage[7]	V_{OL} CC	–	–	0.4	V	$I_{OL} \leq I_{OLnom}$ [8]
		–	–	1.0	V	$I_{OL} \leq I_{OLmax}$

1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{IN} < V_{SS}$) or supply ripple ($V_{IN} > V_{DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.

4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature (T_J = junction temperature [°C]): I_{OZ} = 0.05 x $e^{(1.5 + 0.028 \times TJ>)}$ [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]): I_{OZ} = $I_{OZtempmax}$ - (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.

5) Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} <= V_{IL}$ for a pullup; $V_{PIN} >= V_{IH}$ for a pulldown.

6) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} >= V_{IH}$ for a pullup; $V_{PIN} <= V_{IL}$ for a pulldown.

7) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.

8) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL}->V_{SS}, V_{OH}->V_{DDP}). However, only the levels for nominal output currents are verified.

The timing in the AC Characteristics refers to TCSs. Timing must be calculated using the minimum TCS possible under the given circumstances.
The actual minimum value for TCS depends on the jitter of the PLL. Because the PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or oscillator), the accumulated jitter is limited. This means that the relative deviation for periods of more than one TCS is lower than for a single TCS (see formulas and **Figure 20**).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler K2 to generate the system clock signal f_{SYS}. The number of VCO cycles is K2 × **T**, where **T** is the number of consecutive f_{SYS} cycles (TCS).

The maximum accumulated jitter (long-term jitter) D_{Tmax} is defined by:

D_{Tmax} [ns] = $\pm(220 / (K2 \times f_{SYS}) + 4.3)$

This maximum value is applicable, if either the number of clock cycles T > (f_{SYS} / 1.2) or the prescaler value K2 > 17.

In all other cases for a timeframe of **T** × TCS the accumulated jitter D_T is determined by:

D_T [ns] = $D_{Tmax} \times [(1 - 0.058 \times K2) \times (T - 1) / (0.83 \times f_{SYS} - 1) + 0.058 \times K2]$

f_{SYS} in [MHz] in all formulas.

Example, for a period of 3 TCSs @ 33 MHz and K2 = 4:

$D_{max} = \pm(220 / (4 \times 33) + 4.3) = 5.97$ ns (Not applicable directly in this case!)

$D_3 = 5.97 \times [(1 - 0.058 \times 4) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 4]$
$= 5.97 \times [0.768 \times 2 / 26.39 + 0.232]$
$= 1.7$ ns

Example, for a period of 3 TCSs @ 33 MHz and K2 = 2:

$D_{max} = \pm(220 / (2 \times 33) + 4.3) = 7.63$ ns (Not applicable directly in this case!)

$D_3 = 7.63 \times [(1 - 0.058 \times 2) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 2]$
$= 7.63 \times [0.884 \times 2 / 26.39 + 0.116]$
$= 1.4$ ns

4.7.4 Pad Properties

The output pad drivers of the XC236xB can operate in several user-selectable modes. Strong driver mode allows controlling external components requiring higher currents such as power bridges or LEDs. Reducing the driving power of an output pad reduces electromagnetic emissions (EME). In strong driver mode, selecting a slower edge reduces EME.

The dynamic behavior, i.e. the rise time and fall time, depends on the applied external capacitance that must be charged and discharged. Timing values are given for a capacitance of 20 pF, unless otherwise noted.

In general, the performance of a pad driver depends on the available supply voltage V_{DDP}. Therefore the following tables list the pad parameters for the upper voltage range and the lower voltage range, respectively.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 28 is valid under the following conditions: $V_{DDP} \leq$ 5.5 V; V_{DDP}typ. 5 V; $V_{DDP} \geq$ 4.5 V

Table 28 Standard Pad Parameters for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output driver current (absolute value)[1)]	I_{Omax} CC	–	–	4.0	mA	Driver_Strength = Medium
		–	–	10	mA	Driver_Strength = Strong
		–	–	0.5	mA	Driver_Strength = Weak
Nominal output driver current (absolute value)	I_{Onom} CC	–	–	1.0	mA	Driver_Strength = Medium
		–	–	2.5	mA	Driver_Strength = Strong
		–	–	0.1	mA	Driver_Strength = Weak

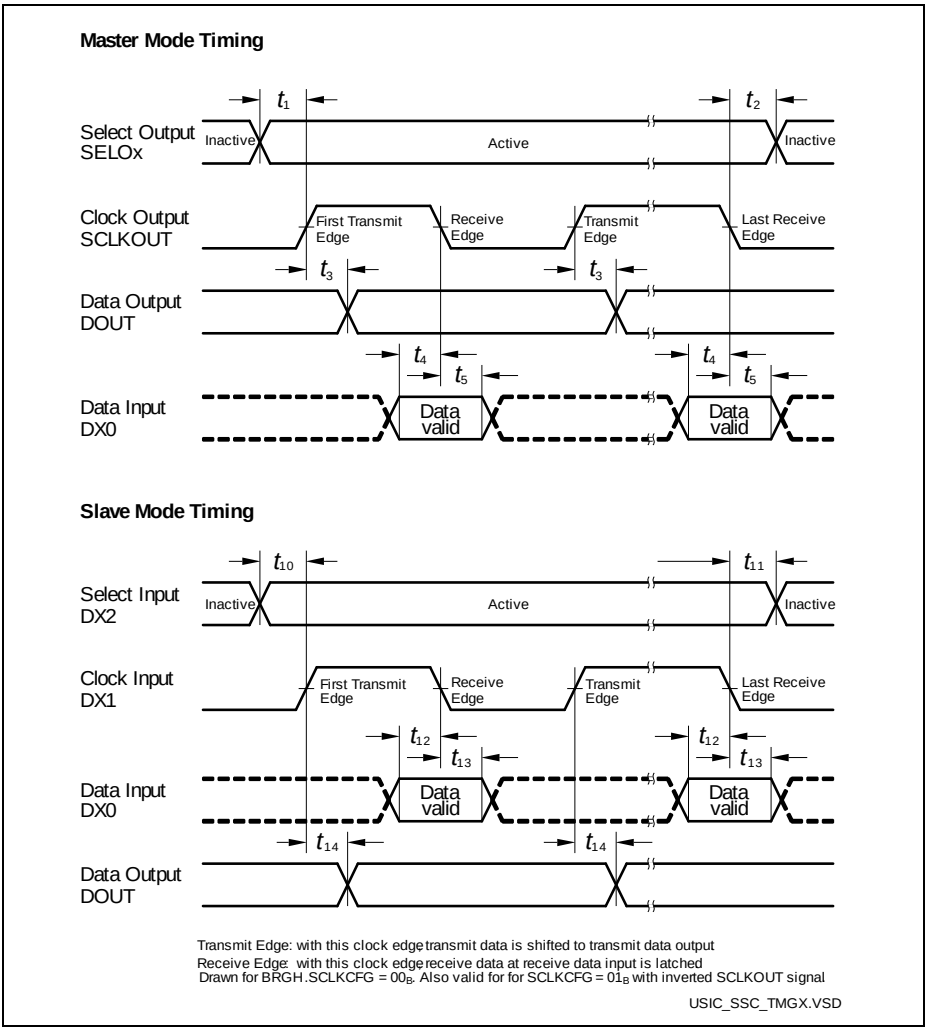

Figure 26 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.

Table 41 JTAG Interface Timing for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	
TDO valid from TCK falling edge (propagation delay)[1]	t_8 CC	–	32	36	ns	
TDO high impedance to valid output from TCK falling edge[2][1]	t_9 CC	–	32	36	ns	
TDO valid output to high impedance from TCK falling edge[1]	t_{10} CC	–	32	36	ns	
TDO hold after TCK falling edge[1]	t_{18} CC	5	–	–	ns	

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

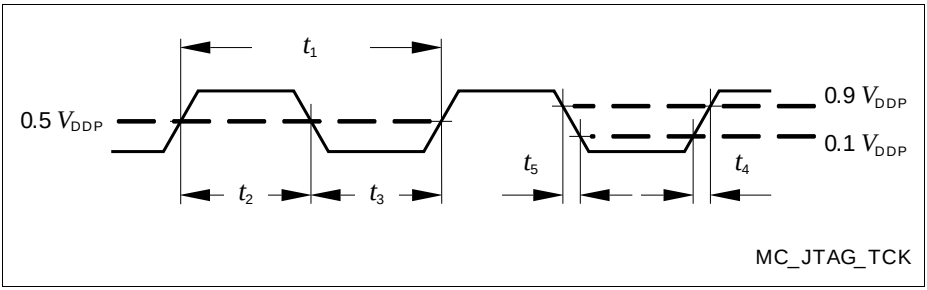

Figure 30 Test Clock Timing (TCK)

Package Outlines

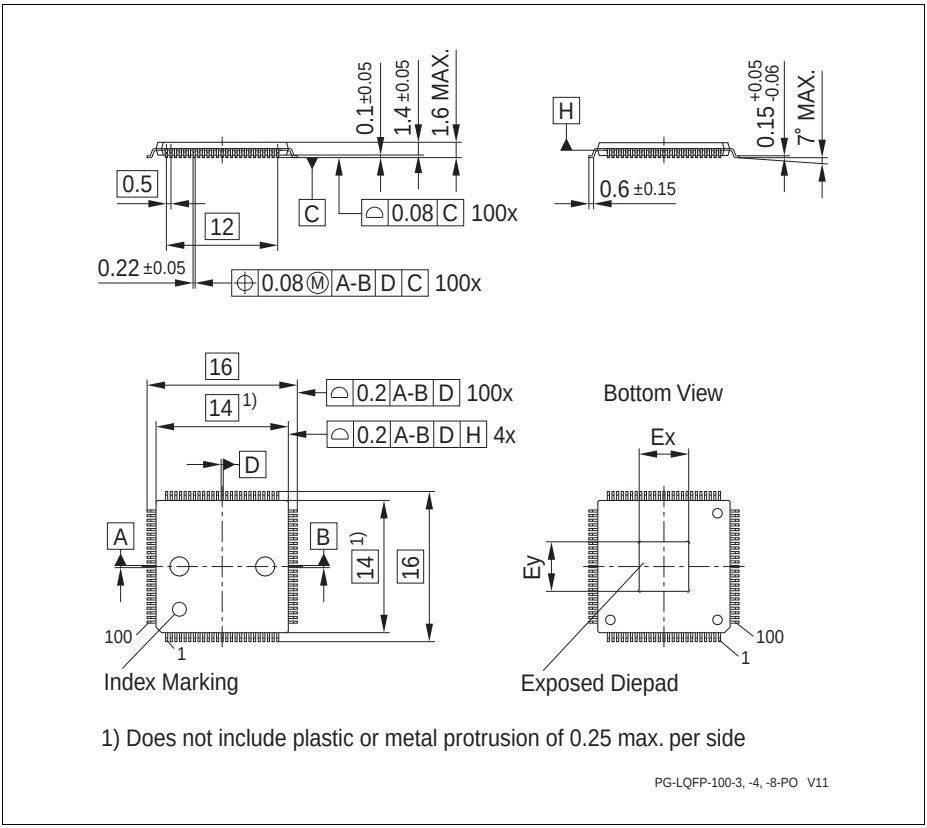

Figure 32 PG-LQFP-100-8/-15 (Plastic Green Thin Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages**