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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 27x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-FQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk20dx64vlk7

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/ pulldown current	10	130	μA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	_	7	pF

K20 Sub-Family Data Sheet, Rev. 3, 11/2012.

5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	3.6	V	
V _{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V _{DD} -to-V _{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V _{SS} -to-V _{SSA} differential voltage	-0.1	0.1	V	
V _{BAT}	RTC battery supply voltage	1.71	3.6	V	
VIH	Input high voltage				
	• $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}$	$0.7 \times V_{DD}$	—	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$	$0.75 \times V_{DD}$	_	V	
V _{IL}	Input low voltage				
	• 2.7 V \leq V _{DD} \leq 3.6 V	_	$0.35 \times V_{DD}$	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$	_	$0.3 \times V_{DD}$	V	
V _{HYS}	Input hysteresis	$0.06 \times V_{DD}$	_	V	
I _{ICDIO}	Digital pin negative DC injection current — single pin	_		_	1
	• V _{IN} < V _{SS} -0.3V	-5	_	mA	
I _{ICAIO}	Analog ² , EXTAL, and XTAL pin DC injection current —				3
	single pin			mA	
	 V_{IN} < V_{SS}-0.3V (Negative current injection) 	-5	—		
	 V_{IN} > V_{DD}+0.3V (Positive current injection) 	—	+5		
I _{ICcont}	Contiguous pin DC injection current —regional limit,				
	positive injection currents of 16 contiguous pins				
	Negative current injection	-25	—	mA	
	Positive current injection	—	+25		
V _{RAM}	V _{DD} voltage required to retain RAM	1.2		V	
V _{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V _{POR_VBAT}		V	

- All 5 V tolerant digital I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than V_{DIO_MIN} (=V_{SS}-0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=(V_{DIO_MIN}-V_{IN})/II_{IC}I.
- 2. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
- 3. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is greater than V_{AIO_MIN} (=V_{SS}-0.3V) and V_{IN} is less than V_{AIO_MAX}(=V_{DD}+0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=(V_{AIO_MIN}-V_{IN})/II_{IC}I. The positive injection current limiting resistor is calculated as R=(V_{IN}-V_{AIO_MAX})/II_{IC}I. Select the larger of these two calculated resistances.



Figure 8. Test Access Port timing





6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

Peripheral operating requirements and behaviors

6.3.1 MCG specifications Table 14. MCG specifications

Symbol	Description		Min.	Тур.	Max.	Unit	Notes
f _{ints_ft}	Internal reference factory trimmed at	frequency (slow clock) — nominal VDD and 25 °C	_	32.768	—	kHz	
f _{ints_t}	Internal reference trimmed	31.25	_	39.0625	kHz		
$\Delta_{fdco_res_t}$	Resolution of trimr frequency at fixed using SCTRIM and	ned average DCO output voltage and temperature — d SCFTRIM	_	± 0.3	± 0.6	%f _{dco}	1
$\Delta f_{dco_res_t}$	Resolution of trimr frequency at fixed using SCTRIM onl	ned average DCO output voltage and temperature — y	_	± 0.2	± 0.5	%f _{dco}	1
Δf_{dco_t}	Total deviation of t frequency over vol	rimmed average DCO output tage and temperature	_	+0.5/-0.7	—	%f _{dco}	1
Δf _{dco_t}	Total deviation of t frequency over fixe range of 0–70°C	_	± 0.3	± 0.3	%f _{dco}	1	
f _{intf_ft}	Internal reference factory trimmed at	_	4	—	MHz		
f _{intf_t}	Internal reference trimmed at nomina	3	_	5	MHz		
f _{loc_low}	Loss of external cl RANGE = 00	(3/5) x f _{ints_t}	_	—	kHz		
f _{loc_high}	Loss of external cl RANGE = 01, 10,	(16/5) x f _{ints_t}	_	—	kHz		
		FI	L	•			
f _{fll_ref}	FLL reference frec	uency range	31.25	—	39.0625	kHz	
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fll ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f _{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f _{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fll_ref}	80	83.89	100	MHz	
f _{dco_t_DMX32}	DCO output frequency	Low range (DRS=00) 732 × f _{fll_ref}	_	23.99	_	MHz	4, 5
		Mid range (DRS=01) 1464 × f _{fll ref}	_	47.97	_	MHz	
		Mid-high range (DRS=10)	_	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}		95.98		MHz	

Table continues on the next page...

K20 Sub-Family Data Sheet, Rev. 3, 11/2012.

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	—	3.6	V	
I _{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	_	200	_	μΑ	
	• 8 MHz (RANGE=01)	_	300	_	μΑ	
	• 16 MHz	_	950	_	μΑ	
	• 24 MHz	_	1.2	_	mA	
	• 32 MHz	_	1.5	_	mA	
I _{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	_	25	_	μΑ	
	• 4 MHz	_	400	_	μA	
	• 8 MHz (RANGE=01)	_	500	_	μA	
	• 16 MHz	_	2.5	_	mA	
	• 24 MHz	_	3	_	mA	
	• 32 MHz	_	4	_	mA	
C _x	EXTAL load capacitance	_	—	_		2, 3
Cy	XTAL load capacitance		—			2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	_	_		MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	_	10	_	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	_	_	_	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	_	1		MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)	_	_		kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	_	—		kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
		_	0	_	kΩ	

6.3.2.1 Oscillator DC electrical specifications Table 15. Oscillator DC electrical specifications

Table continues on the next page...

6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
t _{hvpgm4}	Longword Program high-voltage time	—	7.5	18	μs	
t _{hversscr}	Sector Erase high-voltage time	_	13	113	ms	1
t _{hversblk32k}	Erase Block high-voltage time for 32 KB	_	52	452	ms	1
t _{hversblk256k}	Erase Block high-voltage time for 256 KB	—	104	904	ms	1

Table 19. NVM program/erase timing specifications

1. Maximum time based on expectations at cycling end-of-life.

6.4.1.2 Flash timing specifications — commands Table 20. Flash command timing specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
	Read 1s Block execution time					
t _{rd1blk32k}	• 32 KB data flash	—	—	0.5	ms	
t _{rd1blk256k}	• 256 KB program flash	_	—	1.7	ms	
t _{rd1sec1k}	Read 1s Section execution time (data flash sector)	_	_	60	μs	1
t _{rd1sec2k}	Read 1s Section execution time (program flash sector)	_		60	μs	1
t _{pgmchk}	Program Check execution time	_	_	45	μs	1
t _{rdrsrc}	Read Resource execution time	_	_	30	μs	1
t _{pgm4}	Program Longword execution time		65	145	μs	
	Erase Flash Block execution time					2
t _{ersblk32k}	32 KB data flash	—	55	465	ms	
t _{ersblk256k}	• 256 KB program flash	—	122	985	ms	
t _{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
	Program Section execution time					
t _{pgmsec512p}	• 512 B program flash	_	2.4	—	ms	
t _{pgmsec512d}	• 512 B data flash	_	4.7	_	ms	
t _{pgmsec1kp}	 1 KB program flash 	_	4.7	_	ms	
t _{pgmsec1kd}	• 1 KB data flash	_	9.3		ms	
t _{rd1all}	Read 1s All Blocks execution time	_	—	1.8	ms	
t _{rdonce}	Read Once execution time			25	μs	1
t _{pgmonce}	Program Once execution time		65		μs	
t _{ersall}	Erase All Blocks execution time	—	175	1500	ms	2

Table continues on the next page...

Peripheral operating requirements and behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
t _{vfykey}	Verify Backdoor Access Key execution time	_	—	30	μs	1
	Swap Control execution time					
t _{swapx01}	control code 0x01	_	200	_	μs	
t _{swapx02}	control code 0x02	_	70	150	μs	
t _{swapx04}	control code 0x04	_	70	150	μs	
t _{swapx08}	control code 0x08	_	—	30	μs	
	Program Partition for EEPROM execution time					
t _{pgmpart32k}	• 32 KB FlexNVM	_	70	_	ms	
	Set FlexRAM Function execution time:					
t _{setramff}	Control Code 0xFF	_	50	_	μs	
t _{setram8k}	8 KB EEPROM backup	_	0.3	0.5	ms	
t _{setram32k}	32 KB EEPROM backup	_	0.7	1.0	ms	
	Byte-write to FlexRAM	for EEPROM	1 operation			<u> </u>
t _{eewr8bers}	Byte-write to erased FlexRAM location execution time		175	260	μs	3
	Byte-write to FlexRAM execution time:					
t _{eewr8b8k}	8 KB EEPROM backup	_	340	1700	μs	
t _{eewr8b16k}	16 KB EEPROM backup	_	385	1800	μs	
t _{eewr8b32k}	32 KB EEPROM backup	_	475	2000	μs	
	Word-write to FlexRAM	for EEPRON	I operation	I	1	
t _{eewr16bers}	Word-write to erased FlexRAM location execution time	_	175	260	μs	
	Word-write to FlexRAM execution time:					
t _{eewr16b8k}	8 KB EEPROM backup	_	340	1700	μs	
t _{eewr16b16k}	16 KB EEPROM backup	_	385	1800	μs	
t _{eewr16b32k}	32 KB EEPROM backup	_	475	2000	μs	
	Longword-write to FlexRA	M for EEPR	OM operation	1		
t _{eewr32bers}	Longword-write to erased FlexRAM location execution time	_	360	540	μs	
	Longword-write to FlexRAM execution time:					
t _{eewr32b8k}	8 KB EEPROM backup	_	545	1950	μs	
t _{eewr32b16k}	16 KB EEPROM backup	_	630	2050	μs	
t _{eewr32b32k}	32 KB EEPROM backup	_	810	2250	μs	

Table 20. Flash command timing specifications (continued)

1. Assumes 25 MHz flash clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

Peripheral operating requirements and behaviors

The bytes not assigned to data flash via the FlexNVM partition code are used by the flash memory module to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

Writes_subsystem = $\frac{EEPROM - 2 \times EEESPLIT \times EEESIZE}{EEESPLIT \times EEESIZE} \times Write_efficiency \times n_{nvmcycd}$

where

- Writes_subsystem minimum number of writes to each FlexRAM location for subsystem (each subsystem can have different endurance)
- EEPROM allocated FlexNVM for each EEPROM subsystem based on DEPART; entered with the Program Partition command
- EEESPLIT FlexRAM split factor for subsystem; entered with the Program Partition command
- EEESIZE allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write_efficiency
 - 0.25 for 8-bit writes to FlexRAM
 - 0.50 for 16-bit or 32-bit writes to FlexRAM
- n_{nvmcycd} data flash cycling endurance (the following graph assumes 10,000 cycles)

Peripheral operating requirements and behaviors



Figure 10. EEPROM backup writes to FlexRAM

6.4.2 EzPort Switching Specifications Table 23. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	f _{SYS} /2	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	f _{SYS} /8	MHz
EP2	EZP_CS negation to next EZP_CS assertion	2 x t _{EZP_CK}		ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5		ns
EP4	EZP_CK high to EZP_CS input invalid (hold)	5		ns
EP5	EZP_D input valid to EZP_CK high (setup)	2		ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5		ns
EP7	EZP_CK low to EZP_Q output valid	—	16	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	_	ns
EP9	EZP_CS negation to EZP_Q tri-state	—	12	ns

Peripheral operating requirements and behaviors



Figure 13. FlexBus write timing diagram

6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

6.6 Analog

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
	ADC	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	t _{ADACK} = 1/
	asynchronous clock source	• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	f _{ADACK}
f _{ADACK}		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter	for sample t	imes			
TUE	Total unadjusted	12-bit modes		±4	±6.8	LSB ⁴	5
	error	 <12-bit modes 	—	±1.4	±2.1		
DNL	Differential non-	12-bit modes		±0.7	-1.1 to +1.9	LSB ⁴	5
	linearity				-0.3 to 0.5		
		 <12-bit modes 	—	±0.2			
INL	Integral non-	12-bit modes		±1.0	-2.7 to +1.9	LSB ⁴	5
	linearity				-0.7 to +0.5		
		 <12-bit modes 	—	±0.5			
E _{FS}	Full-scale error	12-bit modes	—	-4	-5.4	LSB ⁴	V _{ADIN} =
		 <12-bit modes 	—	-1.4	-1.8		V _{DDA}
Eo	Quantization	16-bit modes		-1 to 0		LSB ⁴	
	error	• ≤13-bit modes	—		±0.5		
ENOB	Effective number	16-bit differential mode					6
	of bits	• Avg = 32	12.8	14.5	_	bits	
		• Avg = 4	11.9	13.8	—	bits	
		16-bit single-ended mode					
		• Avg = 32	10.0	10.0			
		• Avg = 4	12.2	13.9	_	bits	
			11.4	13.1	_	bits	
SINAD	plus distortion	See ENOB	6.02	2 × ENOB +	1.76	dB	
THD	Total harmonic	16-bit differential mode					7
	distortion	• Avg = 32	—	-94	—	dB	
		16-bit single-ended mode					
		• Avg = 32	—	-85	_	dB	
SEDB	Sourious free	16-bit differential mode					7
	dynamic range	• Δvg = 32	82	05		dB	'
	-	- Avy = 52	02	90		uD	
		16-bit single-ended mode	70	00		AD	
		• Avg = 32	70	30		UD	

Table 27. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Table continues on the next page ...

Symbol	Description	Conditions ¹	Min. Typ. ² Max.			Unit	Notes
E _{IL}	Input leakage error			I _{In} × R _{AS}		mV	I _{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device		1.715		mV/°C	
V _{TEMP25}	Temp sensor voltage	25 °C	_	719	_	mV	

Table 27. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

- 1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
- Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit must be set, the HSC bit must be clear with 1 MHz ADC conversion clock speed.
- 4. 1 LSB = $(V_{REFH} V_{REFL})/2^N$
- 5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- 6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- 7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.







Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
C _{rate}	ADC conversion	≤ 13 bit modes	18.484	—	450	Ksps	7
	rate	No ADC hardware averaging					
		Continuous conversions enabled					
		Peripheral clock = 50 MHz					
		16 bit modes	37.037	_	250	Ksps	8
		No ADC hardware averaging					
		Continuous conversions enabled					
		Peripheral clock = 50 MHz					

Table 28. 16-bit ADC with PGA operating conditions (continued)

- 1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- 2. ADC must be configured to use the internal voltage reference (VREF_OUT)
- 3. PGA reference is internally connected to the VREF_OUT pin. If the user wishes to drive VREF_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
- 4. For single ended configurations the input impedance of the driven input is R_{PGAD}/2
- 5. The analog source resistance (R_{AS}), external to MCU, should be kept as minimum as possible. Increased R_{AS} causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
- 6. The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25µs time should be allowed for Fin=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
- 7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
- 8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1

6.6.1.4 16-bit ADC with PGA characteristics with Chop enabled (ADC PGA[PGACHPb] =0)

Table 29. 16-bit ADC with PGA characteristics

Symbol	Description	Conditions	Min.	Typ. ¹	Unit	Notes	
I _{DDA_PGA}	Supply current	Low power (ADC_PGA[PGALPb]=0)	_	420	μA	2	
I _{DC_PGA}	Input DC current		$\frac{2}{R_{\text{PGAD}}} \left(\frac{1}{2}\right)$	V _{REFPGA} ×0.5 (Gain+	$\frac{83-V_{CM}}{1}$	A	3
		Gain =1, V_{REFPGA} =1.2V, V_{CM} =0.5V	_	1.54	μA		
		Gain =64, V_{REFPGA} =1.2V, V_{CM} =0.1V		0.57	_	μA	

Table continues on the next page ...

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{out}	Voltage reference output with factory trim at nominal V _{DDA} and temperature=25C	1.1915	1.195	1.1977	V	
V _{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	
V _{out}	Voltage reference output — user trim	1.193	—	1.197	V	
V _{step}	Voltage reference trim step	—	0.5	—	mV	
V _{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range)	_	_	80	mV	
I _{bg}	Bandgap only current	—	—	80	μA	1
I _{lp}	Low-power buffer current	—	—	360	uA	1
I _{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation				μV	1, 2
	• current = ± 1.0 mA	_	200	_		
T _{stup}	Buffer startup time	_	_	100	μs	
V _{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	_	2	_	mV	1

Table 34. VREF full-range operating behaviors

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.

2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 35. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T _A	Temperature	0	50	°C	

Table 36. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V _{out}	Voltage reference output with factory trim	1.173	1.225	V	

6.7 Timers

See General switching specifications.

6.8 Communication interfaces

Peripheral operating requirements and behaviors



Figure 26. I2S/SAI timing — slave modes

6.8.9.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 45.I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes
(full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	_	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	-	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	53	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	_	ns

Peripheral operating requirements and behaviors



Figure 27. I2S/SAI timing — master modes

Table 46. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	_	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	7.6	-	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	_	67	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	6.5	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	_	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

Peripheral operating requirements and behaviors



Figure 28. I2S/SAI timing — slave modes

6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 47. TSI electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{DDTSI}	Operating voltage	1.71	—	3.6	V	
C _{ELE}	Target electrode capacitance range	1	20	500	pF	1
f _{REFmax}	Reference oscillator frequency	_	8	15	MHz	2, 3
f _{ELEmax}	Electrode oscillator frequency	—	1	1.8	MHz	2, 4
C _{REF}	Internal reference capacitor	_	1	_	pF	
V _{DELTA}	Oscillator delta voltage	_	500	_	mV	2, 5
I _{REF}	Reference oscillator current source base current • 2 μA setting (REFCHRG = 0)		2	3	μΑ	2, 6
	• 32 µA setting (REFCHRG = 15)	_	36	50		
I _{ELE}	Electrode oscillator current source base current • 2 µA setting (EXTCHRG = 0)	_	2	3	μA	2, 7
	 32 µA setting (EXTCHRG = 15) 		36	50		
Pres5	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	8
Pres20	Electrode capacitance measurement precision	_	8.3333	38400	fF/count	9
Pres100	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	10
MaxSens	Maximum sensitivity	0.008	1.46	—	fF/count	11
Res	Resolution	_	_	16	bits	
T _{Con20}	Response time @ 20 pF	8	15	25	μs	12
I _{TSI_RUN}	Current added in run mode		55	—	μA	
I _{TSI_LP}	Low power mode current adder	_	1.3	2.5	μΑ	13

Dimensions

- 1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
- 2. Fixed external capacitance of 20 pF.
- 3. REFCHRG = 2, EXTCHRG=0.
- 4. REFCHRG = 0, EXTCHRG = 10.
- 5. $V_{DD} = 3.0 V.$
- 6. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
- 7. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
- 8. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; lext = 16.
- 9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; lext = 16.
- 10. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; lext = 16.
- 11. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes. Sensitivity depends on the configuration used. The documented values are provided as examples calculated for a specific configuration of operating conditions using the following equation: (C_{ref} * I_{ext})/(I_{ref} * PS * NSCN)

The typical value is calculated with the following configuration:

I_{ext} = 6 μA (EXTCHRG = 2), PS = 128, NSCN = 2, I_{ref} = 16 μA (REFCHRG = 7), C_{ref} = 1.0 pF

The minimum value is calculated with the following configuration:

I_{ext} = 2 μA (EXTCHRG = 0), PS = 128, NSCN = 32, I_{ref} = 32 μA (REFCHRG = 15), C_{ref} = 0.5 pF

The highest possible sensitivity is the minimum value because it represents the smallest possible capacitance that can be measured by a single count.

- 12. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, EXTCHRG = 7.
- 13. REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
80-pin LQFP	98ASS23174W

8 Pinout

80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
78	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_ b/ UART0_COL_b	FTM0_CH5	FB_AD1	EWM_OUT_b		
79	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0		
80	PTD7	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		

8.2 K20 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

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Document Number: K20P81M72SF1 Rev. 3, 11/2012