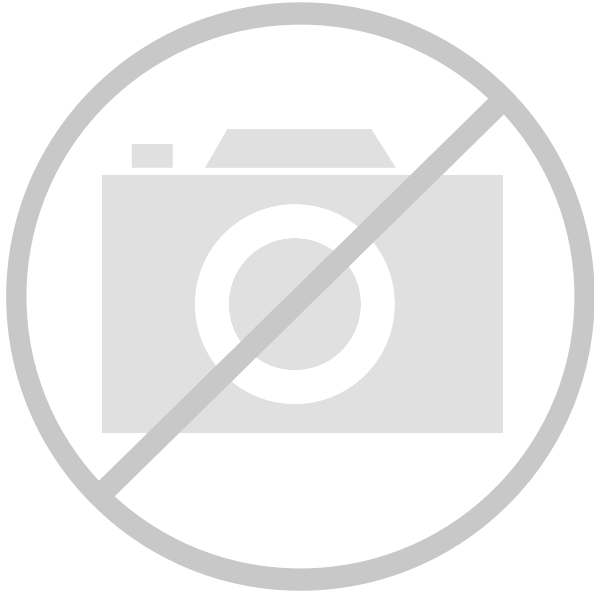

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1), 10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	784-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=kmpc8540cvt667jb

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- 256 Kbyte L2 cache/SRAM
  - Can be configured as follows
    - Full cache mode (256-Kbyte cache).
    - Full memory-mapped SRAM mode (256-Kbyte SRAM mapped as a single 256-Kbyte block or two 128-Kbyte blocks)
    - Half SRAM and half cache mode (128-Kbyte cache and 128-Kbyte memory-mapped SRAM)
  - Full ECC support on 64-bit boundary in both cache and SRAM modes
  - Cache mode supports instruction caching, data caching, or both
  - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing)
  - Eight-way set-associative cache organization (1024 sets of 32-byte cache lines)
  - Supports locking the entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions
  - Global locking and flash clearing done through writes to L2 configuration registers
  - Instruction and data locks can be flash cleared separately
  - Read and write buffering for internal bus accesses
  - SRAM features include the following:
    - I/O devices access SRAM regions by marking transactions as snoopable (global)
    - Regions can reside at any aligned location in the memory map
    - Byte accessible ECC is protected using read-modify-write transactions accesses for smaller than cache-line accesses.
- Address translation and mapping unit (ATMU)
  - Eight local access windows define mapping within local 32-bit address space
  - Inbound and outbound ATMUs map to larger external address spaces
    - Three inbound windows plus a configuration window on PCI/PCI-X
    - Four inbound windows plus a default and configuration window on RapidIO
    - Four outbound windows plus default translation for PCI
    - Eight outbound windows plus default translation for RapidIO
- DDR memory controller
  - Programmable timing supporting DDR-1 SDRAM
  - 64-bit data interface, up to 333-MHz data rate
  - Four banks of memory supported, each up to 1 Gbyte
  - DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
  - Full ECC support
  - Page mode support (up to 16 simultaneous open pages)
  - Contiguous or discontiguous memory mapping

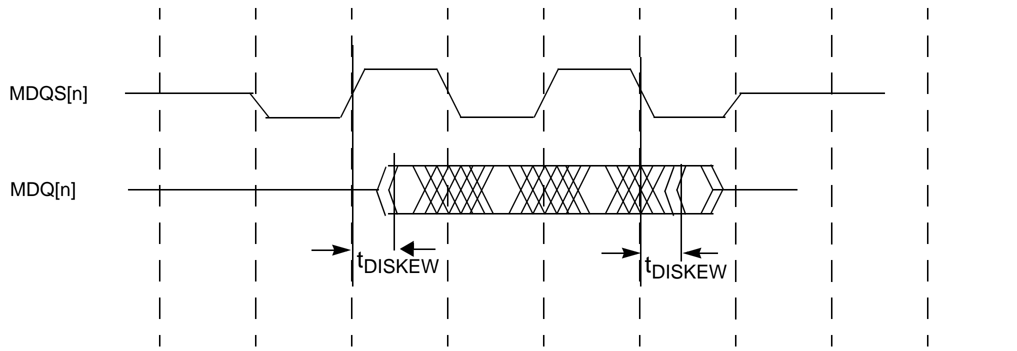

Figure 4. DDR SDRAM Interface Input Timing

6.2.2 DDR SDRAM Output AC Timing Specifications

For chip selects $\overline{MCS1}$ and $\overline{MCS2}$, there will always be at least 200 DDR memory clocks coming out of self-refresh after an $\overline{HRESET}$ before a precharge occurs. This will not necessarily be the case for chip selects $\overline{MCS0}$ and $\overline{MCS3}$.

6.2.2.1 DLL Enabled Mode

Table 16 and Table 17 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface with the DDR DLL enabled.

Table 16. DDR SDRAM Output AC Timing Specifications–DLL Mode

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/$\overline{MCK}$[n] crossing)	t_{MCK}	6	10	ns	2
On chip Clock Skew	$t_{MCKSKEW}$	—	150	ps	3, 8
MCK[n] duty cycle	t_{MCKH}/t_{MCK}	45	55	%	8
ADDR/CMD output valid	t_{DDKHOV}	—	3	ns	4, 9
ADDR/CMD output invalid	t_{DDKHOX}	1	—	ns	4, 9
Write CMD to first MDQS capture edge	t_{DDSHMH}	t_{MCK} + 1.5	t_{MCK} + 4.0	ns	5
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 900 1100 1200	—	ps	6, 9
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 900 1100 1200	—	ps	6, 9
MDQS preamble start	t_{DDSHMP}	0.75 × t_{MCK} + 1.5	0.75 × t_{MCK} + 4.0	ns	7, 8

Table 16. DDR SDRAM Output AC Timing Specifications–DLL Mode (continued)

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDSHME}	1.5	4.0	ns	7, 8

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (OX or DX). For example, t_{DDKHOV} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (O) are valid (V) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. Maximum possible clock skew between a clock MCK[n] and its relative inverse clock $\overline{\text{MCK}}$[n], or between a clock MCK[n] and a relative clock MCK[m] or MSYNC_OUT. Skew measured between complementary signals at $GV_{DD}/2$.
4. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$ and MDQ/MECC/MDM/MDQS.
5. Note that t_{DDSHMH} follows the symbol conventions described in note 1. For example, t_{DDSHMH} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) until the MDQS signal is valid (MH). t_{DDSHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. These controls allow the relationship between the synchronous clock control timing and the source-synchronous DQS domain to be modified by the user. For best turnaround times, these may need to be set to delay t_{DDSHMH} an additional $0.25t_{MCK}$. This will also affect t_{DDSHMP} and t_{DDSHME} accordingly. See the *MPC8540 PowerQUICC III Integrated Host Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8540.
7. All outputs are referenced to the rising edge of MSYNC_IN (S) at the pins of the MPC8540. Note that t_{DDSHMP} follows the symbol conventions described in note 1. For example, t_{DDSHMP} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) for the duration of the MDQS signal precharge period (MP).
8. Guaranteed by design.
9. Guaranteed by characterization.

Figure 5 provides the AC test load for the DDR bus.

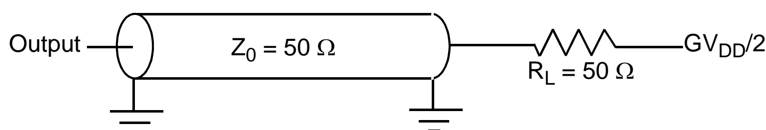

Figure 5. DDR AC Test Load

Table 17. DDR SDRAM Measurement Conditions

Symbol	DDR	Unit	Notes
V_{TH}	MV_{REF} ± 0.31 V	V	1
V_{OUT}	0.5 × GV_{DD}	V	2

Notes:

1. Data input threshold measurement point.
2. Data output measurement point.

Table 22. GMII, MII, RGMII, RTBI, and TBI DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	2.37	2.63	V
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V
Input high voltage	V_{IH}	1.70	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	–0.3	0.70	V
Input high current (V_{IN} [1] = LV_{DD})	I_{IH}	—	10	μA
Input low current (V_{IN} [1] = GND)	I_{IL}	–15	—	μA

Note:

1.Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1and Table 2.

8.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.1.1 GMII Transmit AC Timing Specifications

Table 23 provides the GMII transmit AC timing specifications.

Table 23. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	40	—	60	%
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX} [3]	0.5	—	5.0	ns

Table 23. GMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK data clock rise and fall time	t_{GTXR}, t_{GTXF} [2,4]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by characterization.
4. Guaranteed by design.

Figure 7 shows the GMII transmit AC timing diagram.

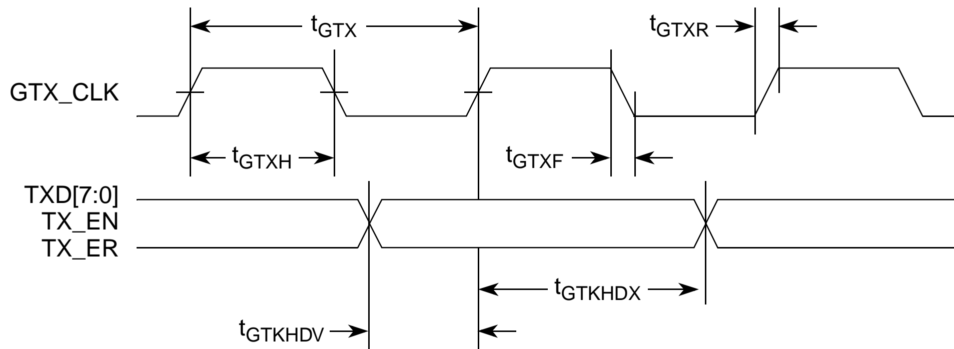

Figure 7. GMII Transmit AC Timing Diagram

8.2.1.2 GMII Receive AC Timing Specifications

Table 24 provides the GMII receive AC timing specifications.

Table 24. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns

Table 24. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock rise and fall time	t_{GRXR}, t_{GRXF} [2,3]	—	—	1.0	ns

Note:

1.The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2.Signal timings are measured at 0.7 V and 1.9 V voltage levels.

3.Guaranteed by design.

Figure 8 provides the AC test load for TSEC.

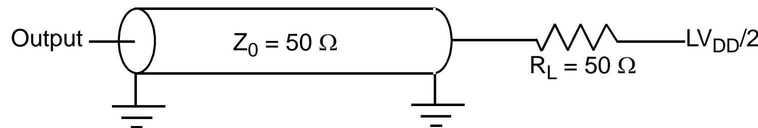

Figure 8. TSEC AC Test Load

Figure 9 shows the GMII receive AC timing diagram.

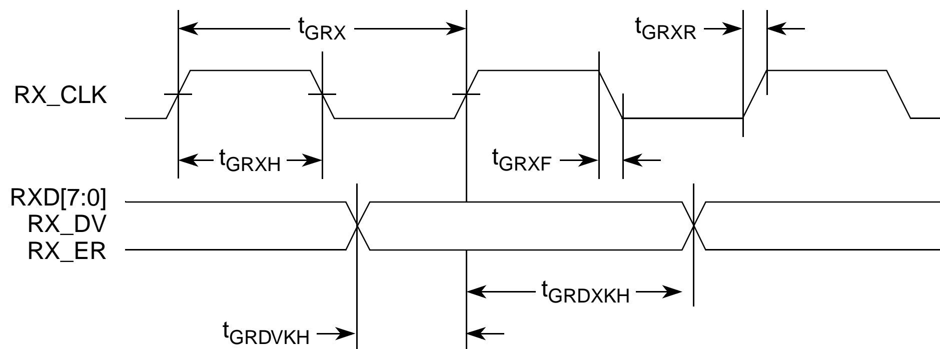

Figure 9. GMII Receive AC Timing Diagram

Figure 15 shows the MII transmit AC timing diagram.

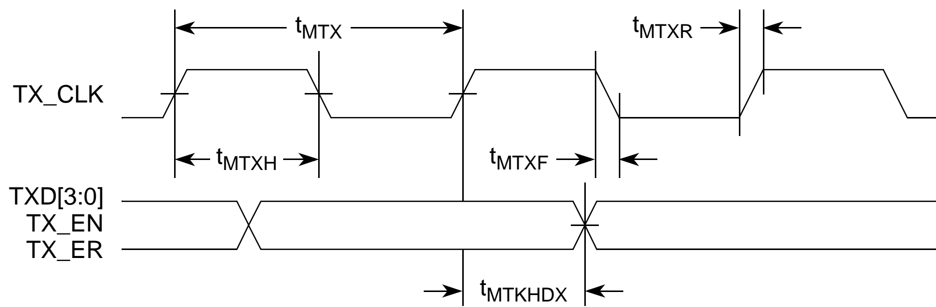

Figure 15. MII Transmit AC Timing Diagram

8.3.2.2 MII Receive AC Timing Specifications

Table 32 provides the MII receive AC timing specifications.

Table 32. MII Receive AC Timing Specifications

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[7:0], TX_DV, TX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[7:0], TX_DV, TX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise and fall time	t_{MRXR}, t_{MRXF} [2,3]	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKH} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the high (H) state or hold time. Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8540.

9.1 Local Bus DC Electrical Characteristics

Table 35 provides the DC electrical characteristics for the local bus interface.

Table 35. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	OV_{DD} - 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.2	V

Note:

1.Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2 Local Bus AC Electrical Specifications

Table 36 describes the general timing parameters of the local bus interface of the MPC8540 with the DLL enabled.

Table 36. Local Bus General Timing Parameters - DLL Enabled

Parameter	POR Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time		t_{LBK}	6.0	—	ns	2
LCLK[n] skew to LCLK[m] or LSYNC_OUT		$t_{LBKSKEW}$	—	150	ps	3, 9
Input setup to local bus clock (except LUPWAIT)		$t_{LBIVKH1}$	1.8	—	ns	4, 5, 8
LUPWAIT input setup to local bus clock		$t_{LBIVKH2}$	1.7	—	ns	4, 5
Input hold from local bus clock (except LUPWAIT)		$t_{LBIXKH1}$	0.5	—	ns	4, 5, 8
LUPWAIT input hold from local bus clock		$t_{LBIXKH2}$	1.0	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)		t_{LBOTOT}	1.5	—	ns	6

Figure 18 provides the AC test load for PCI and PCI-X.

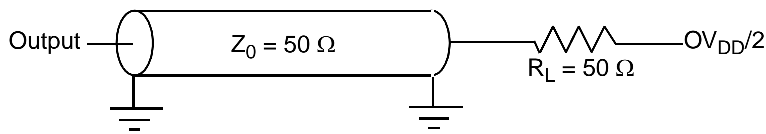

Figure 32. PCI/PCI-X AC Test Load

Figure 33 shows the PCI/PCI-X input AC timing conditions.

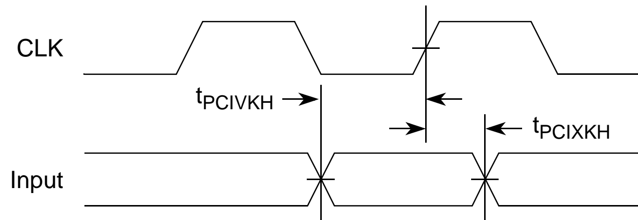

Figure 33. PCI-PCI-X Input AC Timing Measurement Conditions

Figure 34 shows the PCI/PCI-X output AC timing conditions.

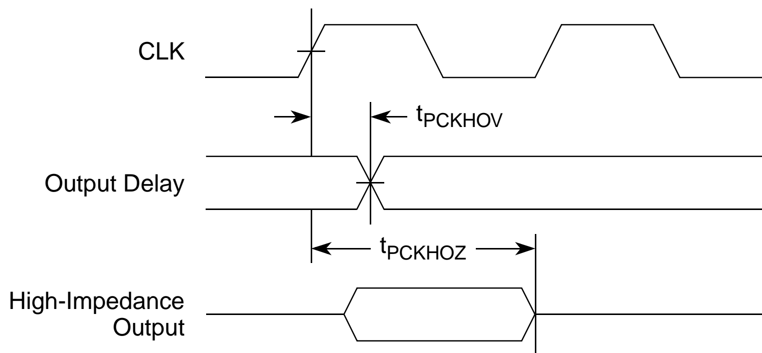

Figure 34. PCI-PCI-X Output AC Timing Measurement Condition

Table 43 provides the PCI-X AC timing specifications at 66 MHz.

Table 43. PCI-X AC Timing Specifications at 66 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	—	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t_{PCKHOX}	0.7	—	ns	1, 10
SYSCLK to output high impedance	t_{PCKHOZ}	—	7	ns	1, 4, 8, 11
Input setup time to SYSCLK	t_{PCIVKH}	1.7	—	ns	3, 5
Input hold time from SYSCLK	t_{PCIXKH}	0.5	—	ns	10
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time	t_{PCRVRH}	10	—	clocks	11
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	11
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	9, 11

Table 44. PCI-X AC Timing Specifications at 133 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time	t_{PCRHIX}	0	50	ns	6, 12

Notes:

1. See the timing measurement conditions in the *PCI-X 1.0a Specification*.
2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
3. Setup time for point-to-point signals applies to $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ only. All other signals are bused.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
6. Maximum value is also limited by delay to the first transaction (time for $\overline{\text{HRESET}}$ high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of $\overline{\text{HRESET}}$ must be negated no later than two clocks before the first $\overline{\text{FRAME}}$ and must be floated no later than one clock before $\overline{\text{FRAME}}$ is asserted.
7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
8. Device must meet this specification independent of how many outputs switch simultaneously.
9. The timing parameter t_{PCIVKH} is a minimum of 1.4 ns rather than the minimum of 1.2 ns in the *PCI-X 1.0a Specification.*
10. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*
11. Guaranteed by characterization.
12. Guaranteed by design.

13 RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8540.

13.1 RapidIO DC Electrical Characteristics

RapidIO driver and receiver DC electrical characteristics are provided in Table 45 and Table 46, respectively.

Table 45. RapidIO 8/16 LP-LVDS Driver DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Characteristic	Symbol	Min	Max	Unit	Notes
Differential output high voltage	V_{OHD}	247	454	mV	1, 2
Differential output low voltage	V_{OLD}	–454	–247	mV	1, 2
Differential offset voltage	ΔV_{OSD}	—	50	mV	1,3
Output high common mode voltage	V_{OHCM}	1.125	1.375	V	1, 4
Output low common mode voltage	V_{OLCM}	1.125	1.375	V	1, 5

Table 49. RapidIO Driver AC Timing Specifications—1 Gbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential output high voltage	V_{OHD}	200	540	mV	1
Differential output low voltage	V_{OLD}	–540	–200	mV	1
Duty cycle	DC	48	52	%	2, 6
V_{OD} rise time, 20%–80% of peak to peak differential signal swing	t_{FALL}	100	—	ps	3, 6
V_{OD} fall time, 20%–80% of peak to peak differential signal swing	t_{RISE}	100	—	ps	6
Data valid	DV	575	—	ps	6
Skew of any two data outputs	t_{DPAIR}	—	100	ps	4, 6
Skew of single data outputs to associated clock	$t_{SKEW,PAIR}$	–100	100	ps	5, 6

Notes:

1.See Figure 38.

2.Requires ±100 ppm long term frequency stability.

3.Measured at V_{OD} = 0 V.

4.Measured using the RapidIO transmit mask shown in Figure 38.

5.See Figure 43.

6.Guaranteed by design.

The compliance of driver output signals TD[0:15] and TFRAME with their minimum data valid window (DV) specification shall be determined by generating an eye pattern for each of the data signals and comparing the eye pattern of each data signal with the RapidIO transmit mask shown in Figure 38. The value of X2 used to construct the mask shall be $(1 – DV_{min})/2$. A signal is compliant with the data valid window specification if the transmit mask can be positioned on the signal's eye pattern such that the eye pattern falls entirely within the unshaded portion of the mask.

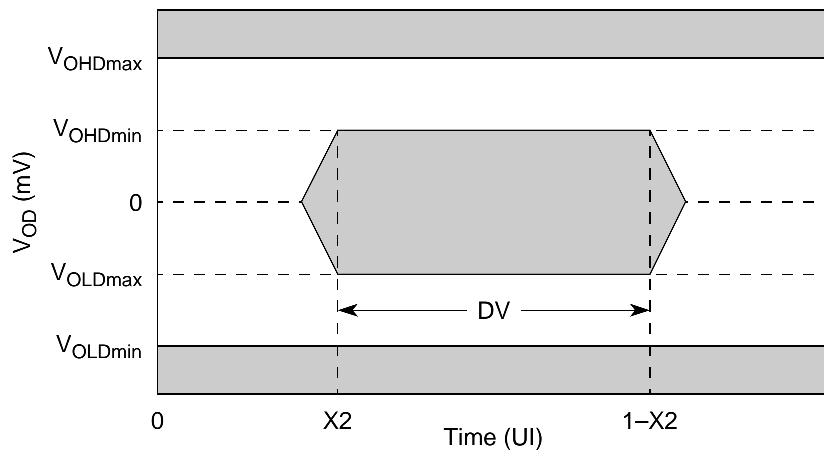

Figure 38. RapidIO Transmit Mask

enough that increasing the length of the sequence does not cause the resulting eye pattern to change from one that complies with the RapidIO receive mask to one that does not comply with the mask. The data carried by any given data signal in the interface may not be correlated with the data carried by any other data signal in the interface. The zero-crossings of the clock associated with a data signal shall be used as the timing reference for aligning the multiple recordings of the data signal when the recordings are overlaid.

While the method used to make the recordings and overlay them to form the eye pattern is not specified, the method used shall be demonstrably equivalent to the following method. The signal under test is repeatedly recorded with a digital oscilloscope in infinite persistence mode. Each recording is triggered by a zero-crossing of the clock associated with the data signal under test. Roughly half of the recordings are triggered by positive-going clock zero-crossings and roughly half are triggered by negative-going clock zero-crossings. Each recording is at least 1.9 UI in length (to ensure that at least one complete eye is formed) and begins 0.5 UI before the trigger point (0.5 UI before the associated clock zero-crossing). Depending on the length of the individual recordings used to generate the eye pattern, one or more complete eyes will be formed. Regardless of the number of eyes, the eye whose center is immediately to the right of the trigger point is the eye used for compliance testing.

An example of an eye pattern generated using the above method with recordings 3 UI in length is shown in Figure 41. In this example, there is no skew between the signal under test and the associated clock used to trigger the recordings. If skew was present, the eye pattern would be shifted to the left or right relative to the oscilloscope trigger point.

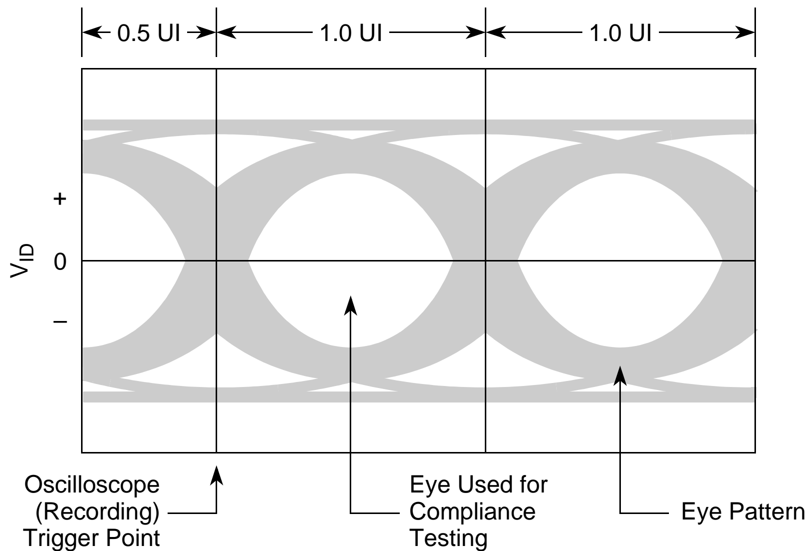

Figure 41. Example Receiver Input Eye Pattern

14 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions.

14.1 Package Parameters for the MPC8540 FC-PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip plastic ball grid array (FC-PBGA).

Die size	12.2 mm × 9.5 mm
Package outline	29 mm × 29 mm
Interconnects	783
Pitch	1 mm
Minimum module height	3.07 mm
Maximum module height	3.75 mm
Solder Balls	62 Sn/36 Pb/2 Ag
Ball diameter (typical)	0.5 mm

Table 53. MPC8540 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Power Management				
ASLEEP	AG18	I/O		9, 19
Power and Ground Signals				
$AV_{DD}1$	AH19	Power for e500 PLL (1.2 V)	$AV_{DD}1$	
$AV_{DD}2$	AH18	Power for CCB PLL (1.2 V)	$AV_{DD}2$	
GND	A12, A17, B3, B14, B20, B26, B27, C2, C4, C11,C17, C19, C22, C27, D8, E3, E12, E24, F11, F18, F23, G9, G12, G25, H4, H12, H14, H17, H20, H22, H27, J19, J24, K5, K9, K18, K23, K28, L6, L20, L25, M4, M12, M14, M16, M22, M27, N2, N13, N15, N17, P12, P14, P16, P23, R13, R15, R17, R20, R26, T3, T8, T10, T12, T14, T16, U6, U13, U15, U16, U17, U21, V7, V10, V26, W5, W18, W23, Y8, Y16, AA6, AA13, AB4, AB11, AB19, AC6, AC9, AD3, AD8, AD17, AF2, AF4, AF10, AF13, AF15, AF27, AG3, AG7, AG26	—	—	
GV_{DD}	A14, A20, A25, A26, A27, A28, B17, B22, B28, C12, C28, D16, D19, D21, D24, D28, E17, E22, F12, F15, F19, F25, G13, G18, G20, G23, G28, H19, H24, J12, J17, J22, J27, K15, K20, K25, L13, L23, L28, M25, N21	Power for DDR DRAM I/O Voltage (2.5 V)	GV_{DD}	
LV_{DD}	A4, C5, E7, H10	Reference Voltage; Three-Speed Ethernet I/O (2.5 V, 3.3 V)	LV_{DD}	
MV_{REF}	N27	Reference Voltage Signal; DDR	MV_{REF}	
No Connects	AH26, AH27, AH28, AG28, AF28, AE28, AH1, AG1, AH2, B1, B2, A2, A3, AH25, H1, H2, J1, J2, J3, J4, J5, J6, J7, J8, K8, K7, K6, K3, K2, K1, L1, L2, L3, L4, L5, L8, L9, L10, L11, M10, M9, M8, M7, M6, M3, M2, P7, P6, P5, P4, P3, P2, P1, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, T9, T6, T5, T4, T1, U1, U2, U3, U4, U8, U10, V5, V4, V3, V2, V1, W1, W2, W3, W6, W7, W8, W9, Y1, Y2, Y3, Y4, Y5, Y6, Y9, AA8, AA7, AA4, AA3, AA2, AA1, AB1, AB2, AB3, AB5, AB6, AC7, AC4, AC3, AC2, AC1	—	—	16
OV_{DD}	D1, E4, H3, K4, K10, L7, M5, N3, P22, R19, R25, T2, T7, U5, U20, U26, V8, W4, W13, W19, W21, Y7, Y23, AA5, AA12, AA16, AA20, AB7, AB9, AB26, AC5, AC11, AC17, AD4, AE1, AE8, AE10, AE15, AF7, AF12, AG27, AH4	PCI/PCI-X, RapidIO, 10/100 Ethernet, and other Standard (3.3 V)	OV_{DD}	

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16.2.4 Heat Sink Selection Examples

The following section provides a heat sink selection example using one of the commercially available heat sinks.

16.2.4.1 Case 1

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_I + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

where

T_J is the die-junction temperature

T_I is the inlet cabinet ambient temperature

T_R is the air temperature rise within the computer cabinet

θ_{JC} is the junction-to-case thermal resistance

θ_{INT} is the adhesive or interface material thermal resistance

θ_{SA} is the heat sink base-to-ambient thermal resistance

P_D is the power dissipated by the device

During operation the die-junction temperatures (T_J) should be maintained within the range specified in Table 2. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_A) may range from 30° to 40°C. The air temperature rise within a cabinet (T_R) may be in the range of 5° to 10°C. The thermal resistance of some thermal interface material (θ_{INT}) may be about 1°C/W. Assuming a T_I of 30 C, a T_R of 5 C, a FC-PBGA package θ_{JC} = 0.8, and a power consumption (P_D) of 7.0 W, the following expression for T_J is obtained:

$$\text{Die-junction temperature: } T_J = 30°C + 5°C + (0.8°C/W + 1.0°C/W + \theta_{SA}) \times 7.0\ W$$

The heat sink-to-ambient thermal resistance (θ_{SA}) versus airflow velocity for a Thermalloy heat sink #2328B is shown in Figure 49.

Assuming an air velocity of 2 m/s, we have an effective θ_{SA+} of about 3.3 C/W, thus

$$T_J = 30\ C + 5\ C + (0.8\ C/W + 1.0\ C/W + 3.3\ C/W) \times 7.0\ W,$$

resulting in a die-junction temperature of approximately 71 C which is well within the maximum operating temperature of the component.

17.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8540 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8540 system, and the MPC8540 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pins of the MPC8540. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

17.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}, GV_{DD}, or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and GND pins of the MPC8540.

17.5 Output Buffer DC Impedance

The MPC8540 drivers are characterized over process, voltage, and temperature. There are two driver types: a push-pull single-ended driver (open drain for I^2C) for all buses except RapidIO, and a current-steering differential driver for the RapidIO port.

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 53). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

18 Document Revision History

Table 61 provides a revision history for this hardware specification.

Table 61. Document Revision History

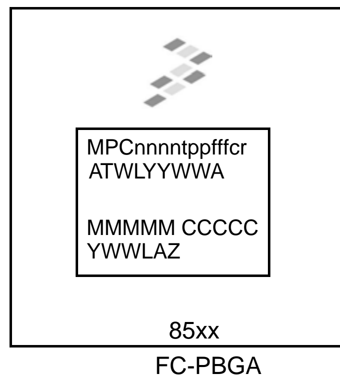
Rev. No.	Substantive Change(s)
4.1	Inserted Figure 3 and paragraph above it. Added PCI/PCI-X row to Input Voltage characteristic and added footnote 6 to Table 1.
4	Updated Note in Section 2.1.2, “Power Sequencing.” Updated back page information.
3.5	Updated Section 2.1.2, “Power Sequencing.” Replaced Section 17.8, “JTAG Configuration Signals.”
3.4	Corrected MV_{REF} Max Value in Table 1. Corrected MV_{REF} Max Value in Table 2. Added new revision level information to Table 62
3.3	Updated MV_{REF} Max Value in Table 1. Removed Figure 3. In Table 4, replaced TBD with power numbers and added footnote. Updated specs and footnotes in Table 8. Corrected max number for MV_{REF} in Table 13. Changed parameter “Clock cycle duration” to “Clock period” in Table 29. Added note 4 to $t_{LBKHOV1}$ and removed LALE reference from $t_{LBKHOV3}$ in Table 36 and Table 37. Updated LALE signal in Figure 19 and Figure 20. Modified Figure 23. Modified Figure 55.

Table 61. Document Revision History (continued)

Rev. No.	Substantive Change(s)
2.0	Section 1.1—Updated features list to coincide with latest version of the reference manual Table 1 and Table 2—Addition of SYSCLK to OV_{IN} Table 2—Addition of notes 1 and 2 Table 3—Addition of note 1 Table 5—New Section 4—New Table 13—Addition of I_{VREF} Removed Figure 4 DDR SRAM Input TIming Diagram Table 15—Modified maximum values for t_{DISKEW} Table 16—Added MSYNC_OUT to tMCKSKEW2 Figure 5—New Section 6.2.1—Removed Figure 4, "DDR SDRAM Input Timing Diagram" Section 8.1—Removed references to 2.5 V from first paragraph Figure 8—New Table 21 and Table 22—Modified "conditions" for I_{IH} and I_{IL} Table 23—Addition of min and max for GTX_CLK125 reference clock duty cycle Table 27 —Addition of min and max for GTX_CLK125 reference clock duty cycle Table 29—Addition of min and max for GTX_CLK125 reference clock duty cycle Table 30—VOH min and conditions; I_{IH} and I_{IL} conditions Table 31—Min and max for t_{MTXR} and t_{MTXF} Table 32—Min and max for t_{MRXR} and t_{MRXF} Figure 23 and Figure 24—Changed LSYNC_IN to Internal clock at top of each figure Figure 18—New Figure 18—New Table 36—Removed row for tLBKHOX3 Table 43—New (AC timing of PCI-X at 66 MHz) Table 53—Addition of note 19 Figure 55—Addition of jumper and note at top of diagram Table 55: Changed max bus freq for 667 core to 166 Section 16.2.1—Modified first paragraph Figure 46—Modified Figure 47—New Table 59—Modified thermal resistance data Section 16.2.4.2—Modified first and second paragraphs

19.2 Part Marking

Parts are marked as the example shown in Figure 56.



Notes:

MMMMM is the 5-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.
YWWLAZ is the assembly traceability code.

Figure 56. Part Marking for FC-PBGA Device

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