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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

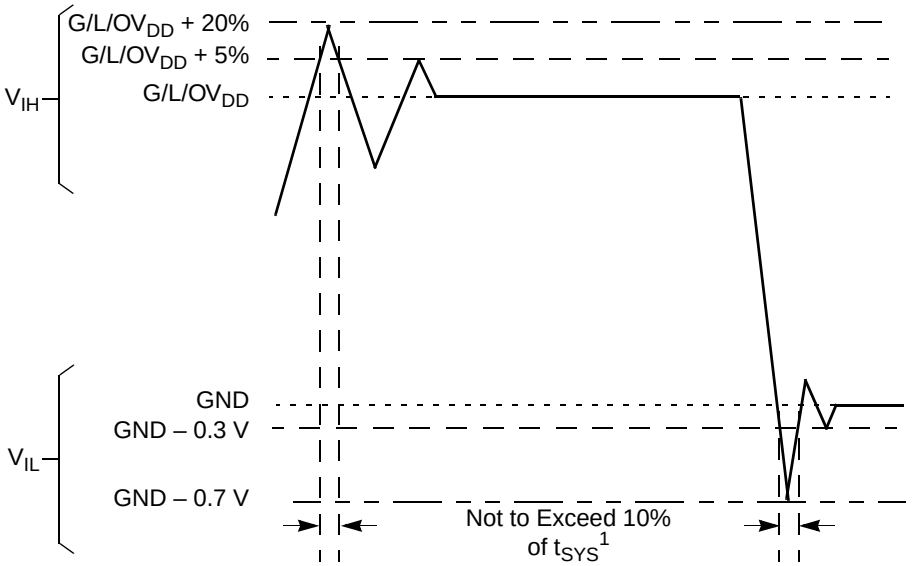
Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1), 10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8540px667lb

  - Interrupts can be routed to the e500 core's standard or critical interrupt inputs
  - Interrupt summary registers allow fast identification of interrupt source
- I^2C controller
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the I^2C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I^2C addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
  - Programming model compatible with the original 16450 UART and the PC16550D
- 10/100 fast Ethernet controller (FEC)
  - Operates at 10 to 100 megabits per second (Mbps) as a device debug and maintenance port
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 166 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
  - Three protocol engines available on a per chip select basis:
    - General purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-,16-, or 32-bit)
- Two three-speed (10/100/1Gb) Ethernet controllers (TSECs)
  - Dual IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab compliant controllers
  - Support for different Ethernet physical interfaces:
    - 10/100/1Gb Mbps IEEE 802.3 GMII
    - 10/100 Mbps IEEE 802.3 MII
    - 10 Mbps IEEE 802.3 MII
    - 1000 Mbps IEEE 802.3z TBI
    - 10/100/1Gb Mbps RGMII/RTBI
  - Full- and half-duplex support

Table 2. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit
Input voltage	DDR DRAM signals	MV_{IN}	GND to GV_{DD}	V
	DDR DRAM reference	MV_{REF}	GND to $GV_{DD/2}$	V
	Three-speed Ethernet signals	LV_{IN}	GND to LV_{DD}	V
	PCI/PCI-X, local bus, RapidIO, 10/100 Ethernet, MII management, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V
Die-junction temperature		T_j	0 to 105	•C

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8540.



Note:
t_{SYS} refers to the clock period associated with the SYSCLK signal.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

The MPC8540 core voltage must always be provided at nominal 1.2 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

Table 6 provides estimated I/O power numbers for each block: DDR, PCI, Local Bus, RapidIO, TSEC, and FEC.

Table 6. Estimated Typical I/O Power Consumption

Interface	Parameter	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Units	Notes
DDR I/O	CCB = 200 MHz	0.46				W	1
	CCB = 266 MHz	0.59					
	CCB = 300 MHz	0.66					
	CCB = 333 MHz	0.73					
PCI/PCI-X I/O	32-bit, 33 MHz		0.04			W	2
	32-bit 66 MHz		0.07				
	64-bit, 66 MHz		0.14				
	64-bit, 133 MHz		0.25				
Local Bus I/O	32-bit, 33 MHz		0.07			W	3
	32-bit, 66 MHz		0.13				
	32-bit, 133 MHz		0.24				
	32-bit, 167 MHz		0.30				
RapidIO I/O	500 MHz data rate		0.96			W	4
TSEC I/O	MII			10		mW	5, 6
	GMII, TBI (2.5 V)				40		
	GMII, TBI (3.3 V)			70			
	RGMII, RTBI				40		
FEC I/O	MII		10			mW	7

Notes:

1. GV_{DD}=2.5, ECC enabled, 66% bus utilization, 33% write cycles, 10pF load on data, 10pF load on address/command, 10pF load on clock
2. OV_{DD}=3.3, 30pF load per pin, 54% bus utilization, 33% write cycles
3. OV_{DD}=3.3, 25pF load per pin, 5pF load on clock, 40% bus utilization, 33% write cycles
4. V_{DD}=1.2, OV_{DD}=3.3
5. LVDD=2.5/3.3, 15pF load per pin, 25% bus utilization
6. Power dissipation for one TSEC only
7. OV_{DD}=3.3, 20pF load per pin, 25% bus utilization

Table 11. RESET Initialization Timing Specifications (continued)

Parameter/Condition	Min	Max	Unit	Notes
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Notes:
1.SYSCLK is identical to the PCI_CLK signal and is the primary clock input for the MPC8540. See the MPC8540 Integrated Processor Preliminary Reference Manual for more details.

Table 12 provides the PLL and DLL lock times.

Table 12. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	
DLL lock times	7680	122,880	CCB Clocks	1, 2

Notes:
1.DLL lock times are a function of the ratio between the output clock and the platform (or CCB) clock. A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The CCB clock is determined by the SYSCLK × platform PLL ratio.

6 DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8540.

6.1 DDR SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8540.

Table 13. DDR SDRAM DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	4
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.18$	V	4
Output leakage current	I_{OZ}	–10	10	μA	5
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–15.2	—	mA	
Output low current (V_{OUT} = 0.35 V)	I_{OL}	15.2	—	mA	

Table 16. DDR SDRAM Output AC Timing Specifications–DLL Mode (continued)

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDSHME}	1.5	4.0	ns	7, 8

Notes:

1.The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (OX or DX). For example, t_{DDKHOV} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (O) are valid (V) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.

2.All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.

3.Maximum possible clock skew between a clock MCK[n] and its relative inverse clock $\overline{\text{MCK}}$[n], or between a clock MCK[n] and a relative clock MCK[m] or MSYNC_OUT. Skew measured between complementary signals at $GV_{DD}/2$.

4.ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$ and MDQ/MECC/MDM/MDQS.

5.Note that t_{DDSHMH} follows the symbol conventions described in note 1. For example, t_{DDSHMH} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) until the MDQS signal is valid (MH). t_{DDSHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. These controls allow the relationship between the synchronous clock control timing and the source-synchronous DQS domain to be modified by the user. For best turnaround times, these may need to be set to delay t_{DDSHMH} an additional $0.25t_{MCK}$. This will also affect t_{DDSHMP} and t_{DDSHME} accordingly. See the *MPC8540 PowerQUICC III Integrated Host Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.

6.Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8540.

7.All outputs are referenced to the rising edge of MSYNC_IN (S) at the pins of the MPC8540. Note that t_{DDSHMP} follows the symbol conventions described in note 1. For example, t_{DDSHMP} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) for the duration of the MDQS signal precharge period (MP).

8.Guaranteed by design.

9.Guaranteed by characterization.

Figure 5 provides the AC test load for the DDR bus.

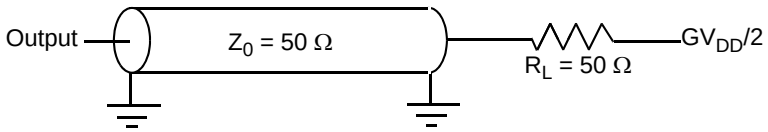


Figure 5. DDR AC Test Load

Table 17. DDR SDRAM Measurement Conditions

Symbol	DDR	Unit	Notes
V_{TH}	MV_{REF} ± 0.31 V	V	1
V_{OUT}	0.5 × GV_{DD}	V	2

Notes:

1.Data input threshold measurement point.

2.Data output measurement point.

Table 23. GMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK data clock rise and fall time	t_{GTXR}, t_{GTXF} [2,4]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by characterization.
4. Guaranteed by design.

Figure 7 shows the GMII transmit AC timing diagram.

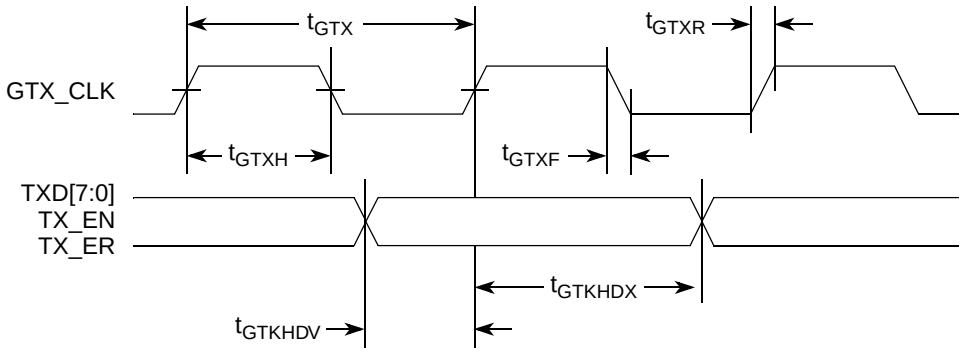


Figure 7. GMII Transmit AC Timing Diagram

8.2.1.2 GMII Receive AC Timing Specifications

Table 24 provides the GMII receive AC timing specifications.

Table 24. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns

8.2.4 RGMII and RTBI AC Timing Specifications

Table 29 presents the RGMII and RTBI AC timing specifications.

Table 29. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT} [5]	–500	0	500	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns
Clock period[3]	t_{RGT} [6]	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4]	t_{RGTH}/t_{RGT} [6]	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3]	t_{RGTH}/t_{RGT} [6]	40	50	60	%
Rise and fall time	t_{RGTR}, t_{RGTF} [6,7]	—	—	0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. The RGMII specification requires that PC board designer add 1.5 ns or greater in trace delay to the RX_CLK in order to meet this specification. However, as stated above, this device will function with only 1.0 ns of delay.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by characterization.
6. Guaranteed by design.
7. Signal timings are measured at 0.5 V and 2.0 V voltage levels.

Figure 14 shows the RGMII and RTBI AC timing and multiplexing diagrams.

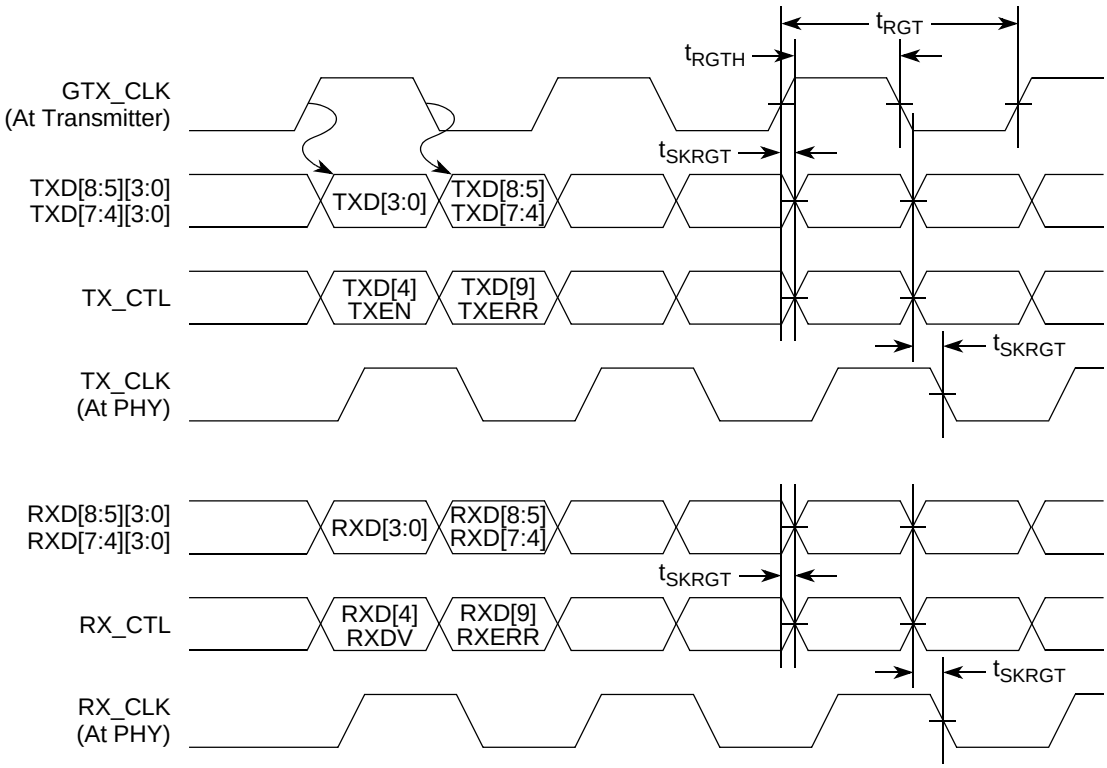


Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 10/100 Ethernet Controller (10/100 Mbps)—MII Electrical Characteristics

The electrical characteristics specified here apply to the MII (media independent interface) signals except MDIO (management data input/output) and MDC (management data clock). The MII interface can be operated at 3.3 or 2.5 V. Whether the MII interface is operated at 3.3 or 2.5 V, the timing is compliant with the IEEE 802.3 standard. The electrical characteristics for MDIO and MDC are specified in Section 2.1.3, "Recommended Operating Conditions."

8.3.1 MII DC Electrical Characteristics

All MII drivers and receivers comply with the DC parametric attributes specified in Table 30. The potential applied to the input of a MII receiver may exceed the potential of the receiver's power supply (that is, a MII driver powered from a 3.6-V supply driving V_{OH} into a MII receiver powered from a 2.5-V supply). Tolerance for dissimilar MII driver and receiver supply potentials is implicit in these specifications.

Figure 19 through Figure 24 show the local bus signals.

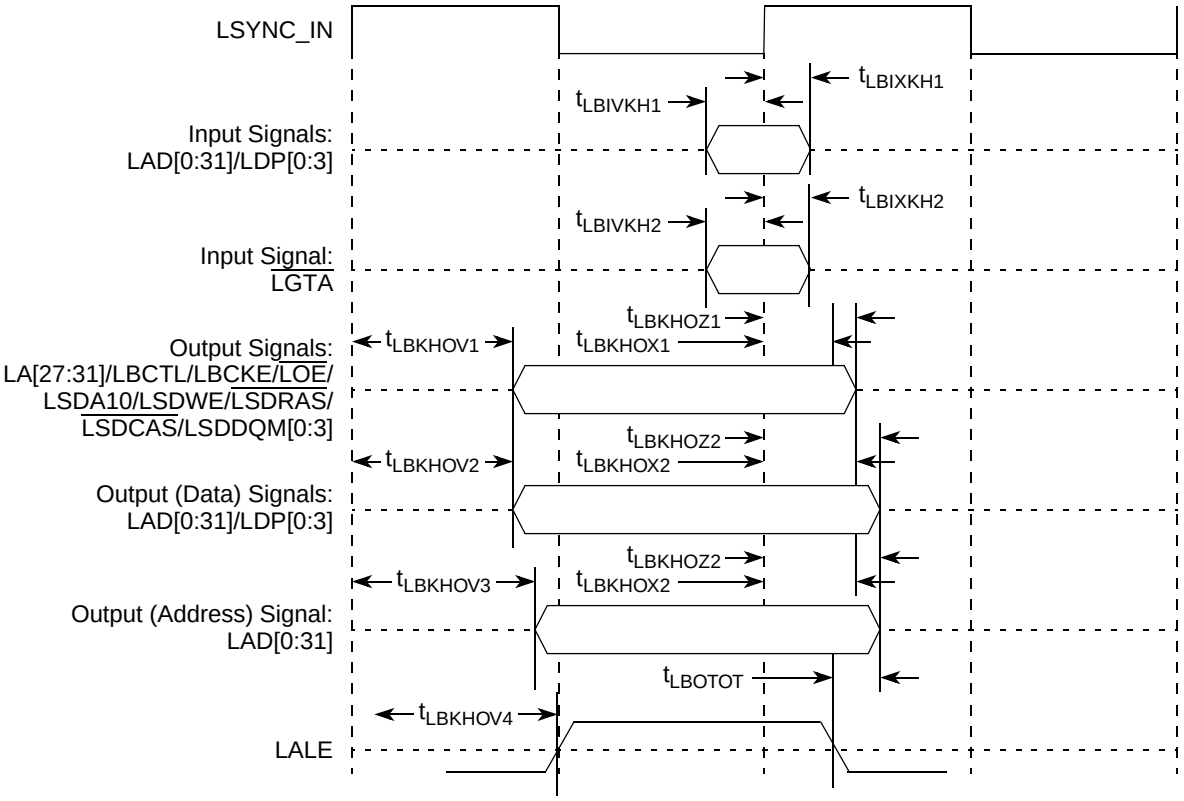


Figure 19. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

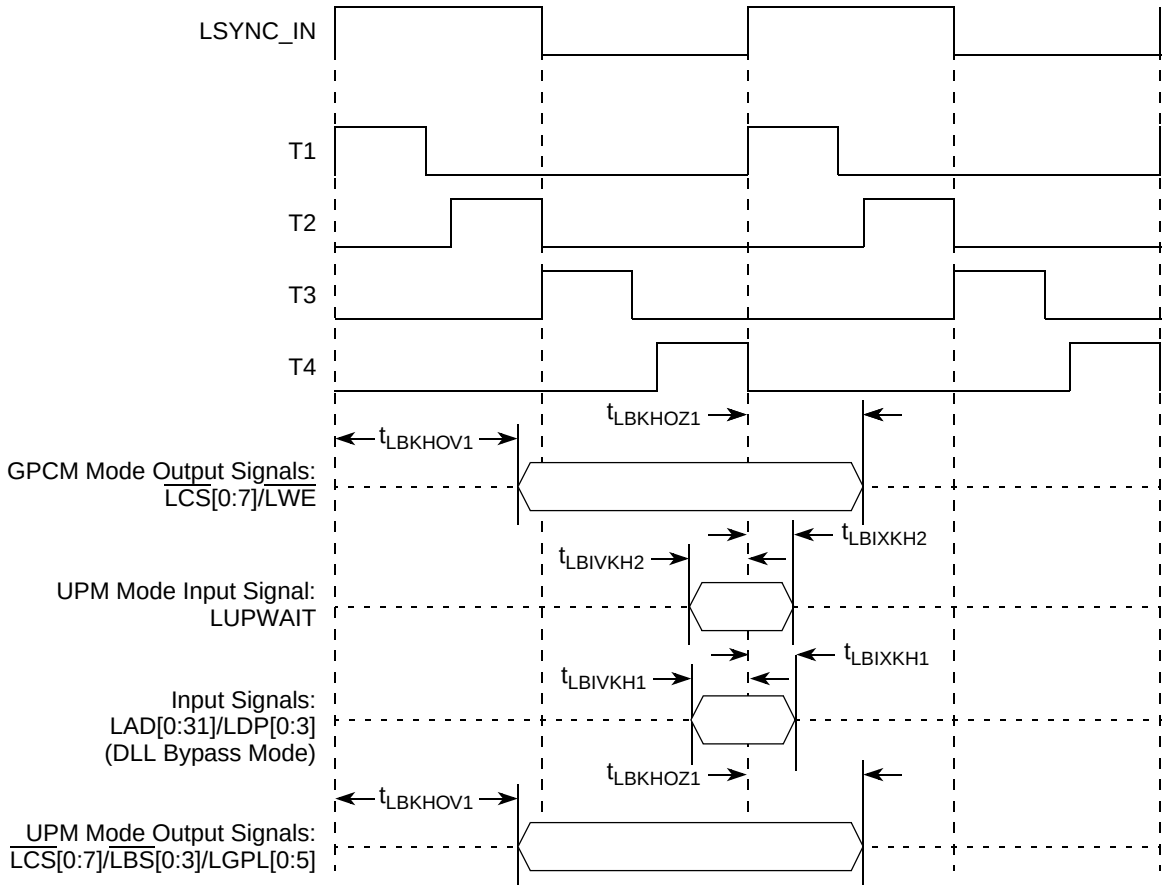


Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Enabled)

Figure 31 shows the AC timing diagram for the I^2C bus.

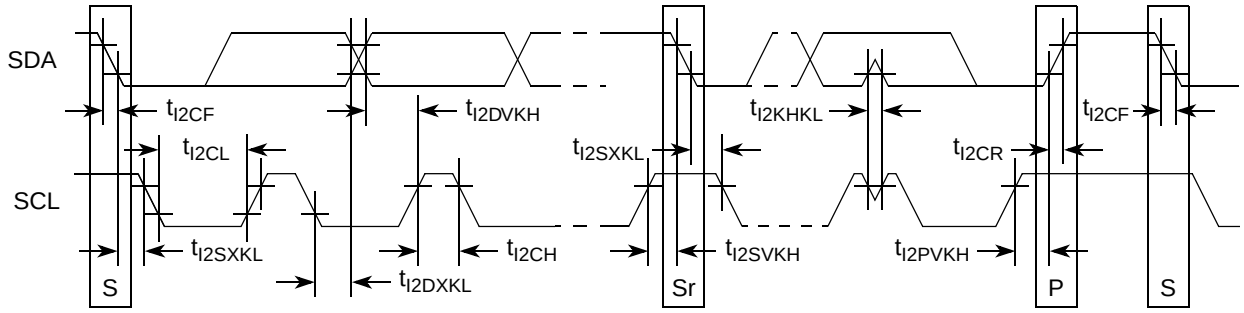


Figure 31. I^2C Bus AC Timing Diagram

12 PCI/PCI-X

This section describes the DC and AC electrical specifications for the PCI/PCI-X bus of the MPC8540.

12.1 PCI/PCI-X DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the PCI/PCI-X interface of the MPC8540.

Table 41. PCI/PCI-X DC Electrical Characteristics [1]

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [2] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Notes:

1.Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.

2.Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

Table 43. PCI-X AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	—	clocks	11
$\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time	t_{PCRHIX}	0	50	ns	6, 11

Notes:

1.See the timing measurement conditions in the *PCI-X 1.0a Specification*.

2.Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.

3.Setup time for point-to-point signals applies to $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ only. All other signals are bused.

4.For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

5.Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.

6.Maximum value is also limited by delay to the first transaction (time for $\overline{\text{HRESET}}$ high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of $\overline{\text{HRESET}}$ must be negated no later than two clocks before the first $\overline{\text{FRAME}}$ and must be floated no later than one clock before $\overline{\text{FRAME}}$ is asserted.

7.A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.

8.Device must meet this specification independent of how many outputs switch simultaneously.

9.The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*

10.Guaranteed by characterization.

11.Guaranteed by design.

Table 44 provides the PCI-X AC timing specifications at 133 MHz.

Table 44. PCI-X AC Timing Specifications at 133 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	—	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t_{PCKHOX}	0.7	—	ns	1, 11
SYSCLK to output high impedance	t_{PCKHOZ}	—	7	ns	1, 4, 8, 12
Input setup time to SYSCLK	t_{PCIVKH}	1.4	—	ns	3, 5, 9, 11
Input hold time from SYSCLK	t_{PCIXKH}	0.5	—	ns	11
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time	t_{PCRVRH}	10	—	clocks	12
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	12
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	10, 12
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	—	clocks	12

Table 44. PCI-X AC Timing Specifications at 133 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time	t_{PCRHIX}	0	50	ns	6, 12

Notes:

1. See the timing measurement conditions in the *PCI-X 1.0a Specification*.
2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
3. Setup time for point-to-point signals applies to $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ only. All other signals are bused.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
6. Maximum value is also limited by delay to the first transaction (time for $\overline{\text{HRESET}}$ high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of $\overline{\text{HRESET}}$ must be negated no later than two clocks before the first $\overline{\text{FRAME}}$ and must be floated no later than one clock before $\overline{\text{FRAME}}$ is asserted.
7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
8. Device must meet this specification independent of how many outputs switch simultaneously.
9. The timing parameter t_{PCIVKH} is a minimum of 1.4 ns rather than the minimum of 1.2 ns in the *PCI-X 1.0a Specification.*
10. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*
11. Guaranteed by characterization.
12. Guaranteed by design.

13 RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8540.

13.1 RapidIO DC Electrical Characteristics

RapidIO driver and receiver DC electrical characteristics are provided in Table 45 and Table 46, respectively.

Table 45. RapidIO 8/16 LP-LVDS Driver DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Characteristic	Symbol	Min	Max	Unit	Notes
Differential output high voltage	V_{OHD}	247	454	mV	1, 2
Differential output low voltage	V_{OLD}	–454	–247	mV	1, 2
Differential offset voltage	ΔV_{OSD}	—	50	mV	1,3
Output high common mode voltage	V_{OHCM}	1.125	1.375	V	1, 4
Output low common mode voltage	V_{OLCM}	1.125	1.375	V	1, 5

14.2 Mechanical Dimensions of the MPC8540 FC-PBGA

Figure 44 the mechanical dimensions and bottom surface nomenclature of the MPC8540, 783 FC-PBGA package.

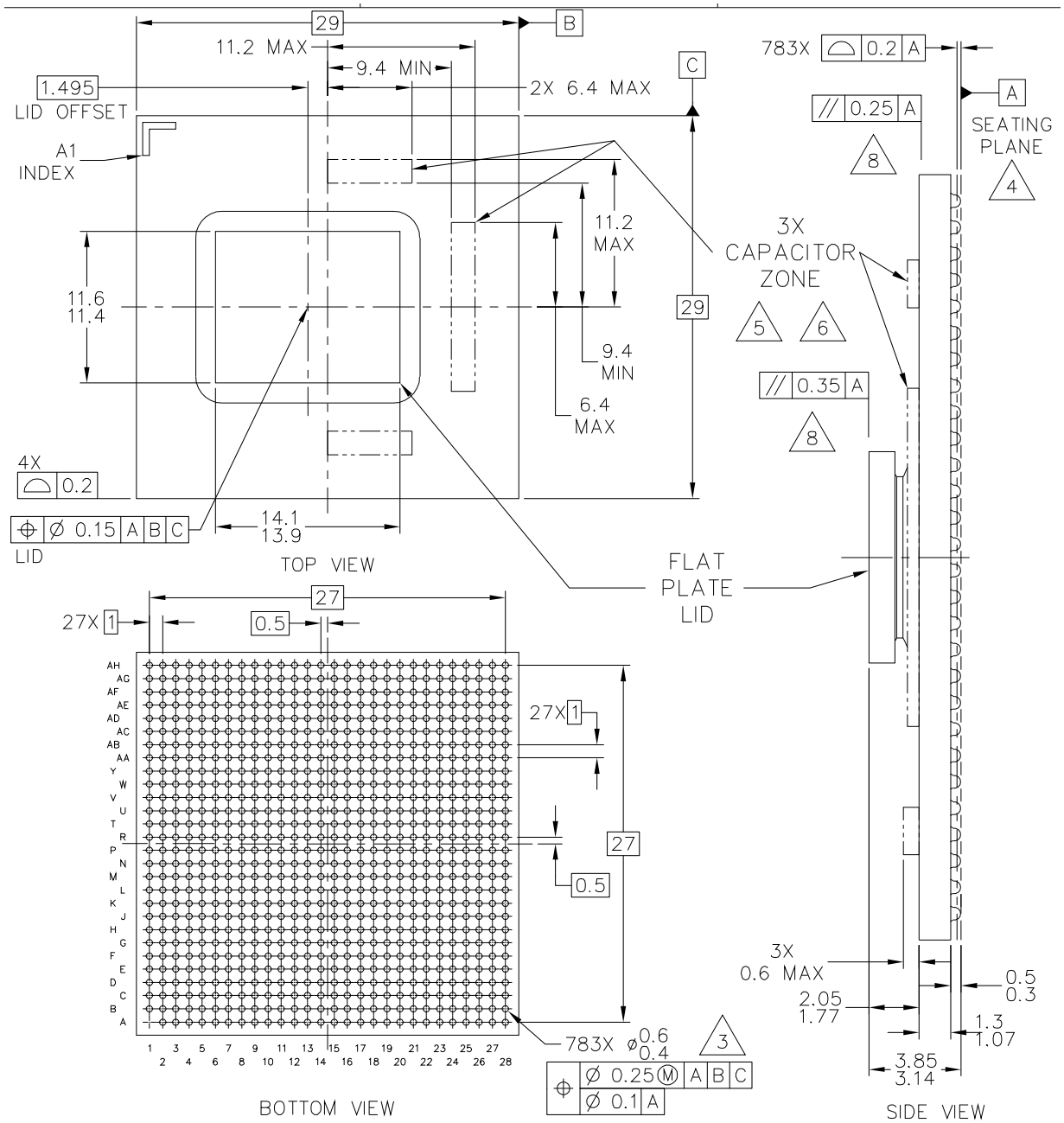


Figure 44. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8540 FC-PBGA

NOTES

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.

Table 53. MPC8540 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{IRQ\_OUT}}$	AB21	O	OV_{DD}	2, 4
Ethernet Management Interface				
EC_MDC	F1	O	OV_{DD}	5, 9
EC_MDIO	E1	I/O	OV_{DD}	
Gigabit Reference Clock				
EC_GTX_CLK125	E2	I	LV_{DD}	
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_TXD[7:4]	A6, F7, D7, C7	O	LV_{DD}	5, 9
TSEC1_TXD[3:0]	B7, A7, G8, E8	O	LV_{DD}	9, 19
TSEC1_TX_EN	C8	O	LV_{DD}	11
TSEC1_TX_ER	B8	O	LV_{DD}	
TSEC1_TX_CLK	C6	I	LV_{DD}	
TSEC1_GTX_CLK	B6	O	LV_{DD}	18
TSEC1_CRS	C3	I	LV_{DD}	
TSEC1_COL	G7	I	LV_{DD}	
TSEC1_RXD[7:0]	D4, B4, D3, D5, B5, A5, F6, E6	I	LV_{DD}	
TSEC1_RX_DV	D2	I	LV_{DD}	
TSEC1_RX_ER	E5	I	LV_{DD}	
TSEC1_RX_CLK	D6	I	LV_{DD}	
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_TXD[7:2]	B10, A10, J10, K11,J11, H11	O	LV_{DD}	5, 9
TSEC2_TXD[1:0]	G11, E11	O	LV_{DD}	
TSEC2_TX_EN	B11	O	LV_{DD}	11
TSEC2_TX_ER	D11	O	LV_{DD}	
TSEC2_TX_CLK	D10	I	LV_{DD}	
TSEC2_GTX_CLK	C10	O	LV_{DD}	18
TSEC2_CRS	D9	I	LV_{DD}	
TSEC2_COL	F8	I	LV_{DD}	
TSEC2_RXD[7:0]	F9, E9, C9, B9, A9, H9, G10, F10	I	LV_{DD}	
TSEC2_RX_DV	H8	I	LV_{DD}	
TSEC2_RX_ER	A8	I	LV_{DD}	

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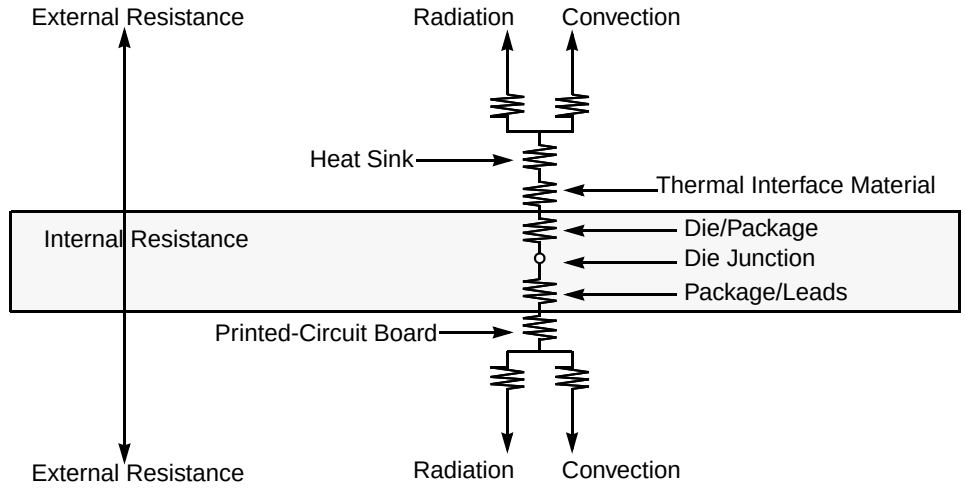
Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the MPC8540 to function in various environments.

16.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8540 thermal model is shown in Figure 46. Five cuboids are used to represent this device. To simplify the model, the solder balls and substrate are modeled as a single block 29x29x1.47 mm with the conductivity adjusted accordingly. For modeling, the planar dimensions of the die are rounded to the nearest mm, so the die is modeled as 10x12 mm at a thickness of 0.76 mm. The bump/underfill layer is modeled as a collapsed resistance between the die and substrate assuming a conductivity of 0.6 in-plane and 1.9 W/m•K in the thickness dimension of 0.76 mm. The lid attach adhesive is also modeled as a collapsed resistance with dimensions of 10x12x0.050 mm and the conductivity of 1 W/m•K. The nickel plated copper lid is modeled as 12x14x1 mm. Note that the die and lid are not centered on the substrate; there is a 1.5 mm offset documented in the case outline drawing in Figure 44.

Figure 47 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 47. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

16.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 48 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 45). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink, the heat sink should be slowly removed. Heating the heat sink to 40-50•C with an air gun can soften the interface material and make the removal easier. The use of an adhesive for heat sink attach is not recommended.

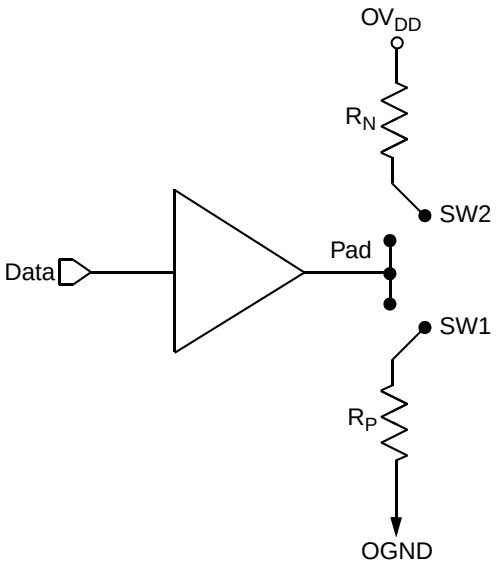


Figure 53. Driver Impedance Measurement

The output impedance of the RapidIO port drivers targets 200-Ω differential resistance. The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 60 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 60. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI/PCI-X	DDR DRAM	RapidIO	Symbol	Unit
R_N	43 Target	25 Target	20 Target	NA	Z_0	W
R_P	43 Target	25 Target	20 Target	NA	Z_0	W
Differential	NA	NA	NA	200 Target	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

18 Document Revision History

Table 61 provides a revision history for this hardware specification.

Table 61. Document Revision History

Rev. No.	Substantive Change(s)
4.1	Inserted Figure 3 and paragraph above it. Added PCI/PCI-X row to Input Voltage characteristic and added footnote 6 to Table 1.
4	Updated Note in Section 2.1.2, “Power Sequencing.” Updated back page information.
3.5	Updated Section 2.1.2, “Power Sequencing.” Replaced Section 17.8, “JTAG Configuration Signals.”
3.4	Corrected MV_{REF} Max Value in Table 1. Corrected MV_{REF} Max Value in Table 2. Added new revision level information to Table 62
3.3	Updated MV_{REF} Max Value in Table 1. Removed Figure 3. In Table 4, replaced TBD with power numbers and added footnote. Updated specs and footnotes in Table 8. Corrected max number for MV_{REF} in Table 13. Changed parameter “Clock cycle duration” to “Clock period” in Table 29. Added note 4 to $t_{LBKHOV1}$ and removed LALE reference from $t_{LBKHOV3}$ in Table 36 and Table 37. Updated LALE signal in Figure 19 and Figure 20. Modified Figure 23. Modified Figure 55.

Table 61. Document Revision History (continued)

Rev. No.	Substantive Change(s)
1.2	Section 1.1.1—Updated feature list. Section 1.2.1.1—Updated notes for Table 1. Section 1.2.1.2—Removed 5-V PCI interface overshoot and undershoot figure. Section 1.2.1.3—Added this section to summarize impedance driver settings for various interfaces. Section 1.4—Updated rows in Reset Initialization timing specifications table. Added a table with DLL and PLL timing specifications. Section 1.5.2.2—Updated note 6 of DDR SDRAM Output AC Timing Specifications table. Section 1.7—Changed the minimum input low current from -600 to -15 μA for the RGMII DC electrical characteristics. Section 1.8.2—Changed LCS[3:4] to TSEC1_TXD[6:5] in. Updated notes regarding LCS[3:4]. Section 1.13.2—Updated the mechanical dimensions diagram for the package. Section 1.13.3—Updated the notes for LBCTL, TRIG_OUT, and ASLEEP. Corrected pin assignments for IIC_SDA and IIC_SCL. Corrected reserved pin assignment of V11 to U11. V11 is actually $\overline{\text{PCI\_STOP}}$. Section 1.14.1—Updated the table for frequency options with respect to platform/CCB frequencies. Section 1.14.4—Edited Frequency options with respect to memory bus speeds.
1.1	Section 1.6.1—Added symbols and note for the GTX_CLK125 timing parameters. Section 1.11.3—Updated pin list table: LGPL5/LSDAMUX to LGPL5, LA[27:29] and LA[30:31] to LA[27:31], FEC_TXD[0:3] to FEC_TXD[3:0], FEC_RXD[0:3] to FEC_RXD[3:0], TRST to $\overline{\text{TRST}}$, added GBE Clocking section and EC_GTX_CLK125 signal. Updated thermal model information to match current offering.
1	Original Customer Version.