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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 667MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100Mbps (1), 10/100/1000Mbps (2) |
| SATA | - |
| USB | - |
| Voltage - I/O | 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 783-BFBGA, FCBGA |
| Supplier Device Package | 783-FCPBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8540px667lc |

  - Interrupts can be routed to the e500 core's standard or critical interrupt inputs
  - Interrupt summary registers allow fast identification of interrupt source
- $I^2C$ controller
  - Two-wire interface
  - Multiple master support
  - Master or slave $I^2C$ mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the $I^2C$ interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended $I^2C$ addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
  - Programming model compatible with the original 16450 UART and the PC16550D
- 10/100 fast Ethernet controller (FEC)
  - Operates at 10 to 100 megabits per second (Mbps) as a device debug and maintenance port
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 166 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
  - Three protocol engines available on a per chip select basis:
    - General purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-,16-, or 32-bit)
- Two three-speed (10/100/1Gb) Ethernet controllers (TSECs)
  - Dual IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab compliant controllers
  - Support for different Ethernet physical interfaces:
    - 10/100/1Gb Mbps IEEE 802.3 GMII
    - 10/100 Mbps IEEE 802.3 MII
    - 10 Mbps IEEE 802.3 MII
    - 1000 Mbps IEEE 802.3z TBI
    - 10/100/1Gb Mbps RGMII/RTBI
  - Full- and half-duplex support

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8540 for the 3.3-V signals, respectively.

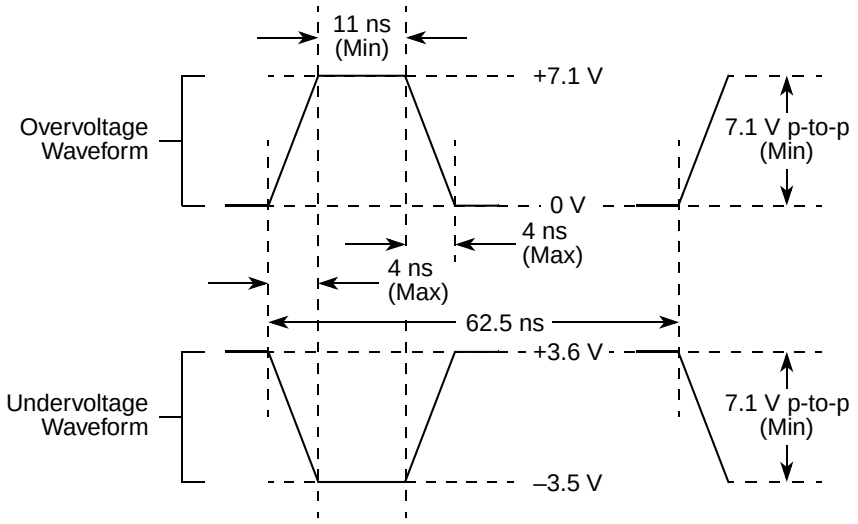



**Figure 3. Maximum AC Waveforms on PCI interface for 3.3-V Signaling**

## 2.1.4 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

**Table 3. Output Drive Capability**

| Driver Type | Programmable Output Impedance (Ω) | Supply Voltage | Notes |
|---|---|---|---|
| Local bus interface utilities signals | 25 | $OV_{DD}$ = 3.3 V | 1 |
| | 42 (default) | | |
| PCI signals | 25 | | 2 |
| | 42 (default) | | |
| DDR signal | 20 | $GV_{DD}$ = 2.5 V | |
| TSEC/10/100 signals | 42 | $LV_{DD}$ = 2.5/3.3 V | |
| DUART, system control, I2C, JTAG | 42 | $OV_{DD}$ = 3.3 V | |
| RapidIO N/A (LVDS signaling) | N/A | | |

**Notes:**

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the $\overline{\text{PCI\_GNT1}}$ signal at reset.

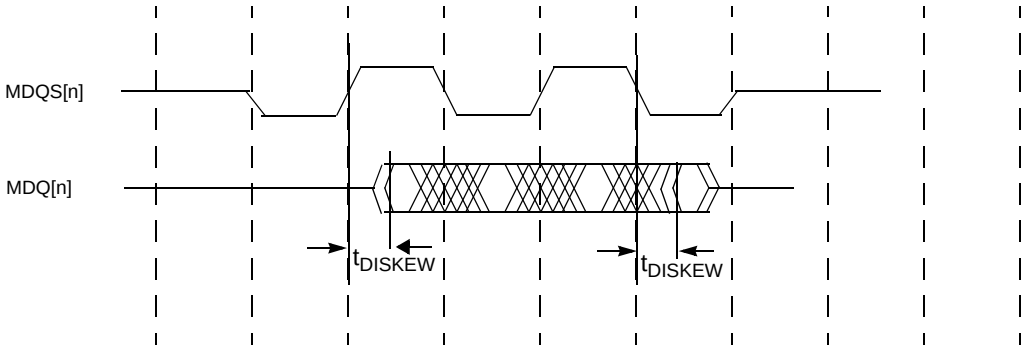



**Figure 4. DDR SDRAM Interface Input Timing**

## 6.2.2 DDR SDRAM Output AC Timing Specifications

For chip selects $\overline{\text{MCS1}}$ and $\overline{\text{MCS2}}$, there will always be at least 200 DDR memory clocks coming out of self-refresh after an $\overline{\text{HRESET}}$ before a precharge occurs. This will not necessarily be the case for chip selects $\overline{\text{MCS0}}$ and $\overline{\text{MCS3}}$.

### 6.2.2.1 DLL Enabled Mode

Table 16 and Table 17 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface with the DDR DLL enabled.

**Table 16. DDR SDRAM Output AC Timing Specifications–DLL Mode**

At recommended operating conditions with $GV_{DD}$ of 2.5 V ± 5%.

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing) | $t_{MCK}$ | 6 | 10 | ns | 2 |
| On chip Clock Skew | $t_{MCKSKEW}$ | — | 150 | ps | 3, 8 |
| MCK[n] duty cycle | $t_{MCKH}/t_{MCK}$ | 45 | 55 | % | 8 |
| ADDR/CMD output valid | $t_{DDKHOV}$ | — | 3 | ns | 4, 9 |
| ADDR/CMD output invalid | $t_{DDKHOX}$ | 1 | — | ns | 4, 9 |
| Write CMD to first MDQS capture edge | $t_{DDSHMH}$ | $t_{MCK}$ + 1.5 | $t_{MCK}$ + 4.0 | ns | 5 |
| MDQ/MECC/MDM output setup with respect to MDQS<br>333 MHz<br>266 MHz<br>200 MHz | $t_{DDKHDS}$,<br>$t_{DDKLDS}$ | <br>900<br>1100<br>1200 | — | ps | 6, 9 |
| MDQ/MECC/MDM output hold with respect to MDQS<br>333 MHz<br>266 MHz<br>200 MHz | $t_{DDKHDX}$,<br>$t_{DDKLDX}$ | <br>900<br>1100<br>1200 | — | ps | 6, 9 |
| MDQS preamble start | $t_{DDSHMP}$ | 0.75 × $t_{MCK}$ + 1.5 | 0.75 × $t_{MCK}$ + 4.0 | ns | 7, 8 |

Figure 16 shows the MII receive AC timing diagram.

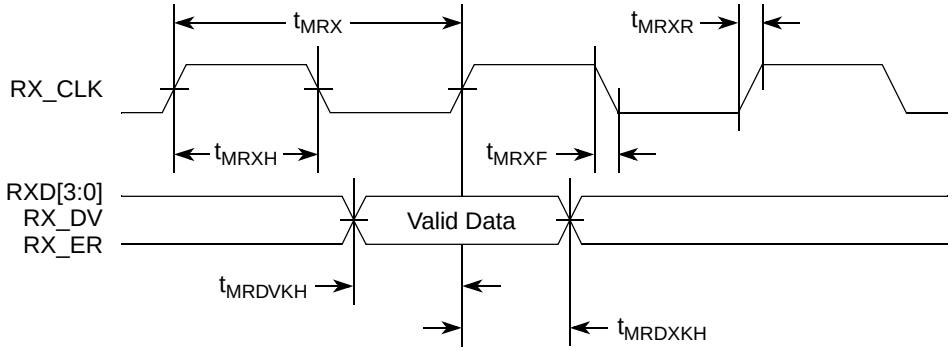



**Figure 16. MII Receive AC Timing Diagram**

# 8.4 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (TSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics."

## 8.4.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 33.

**Table 33. MII Management DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage (3.3 V) | $OV_{DD}$ | 3.13 | 3.47 | V |
| Output high voltage ($OV_{DD}$ = Min, $I_{OH}$ = –1.0 mA) | $V_{OH}$ | 2.10 | $OV_{DD}$ + 0.3 | V |
| Output low voltage ($OV_{DD}$ = Min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | GND | 0.50 | V |
| Input high voltage | $V_{IH}$ | 1.70 | — | V |
| Input low voltage | $V_{IL}$ | — | 0.90 | V |
| Input high current ($OV_{DD}$ = Max, $V_{IN}$ [1] = 2.1 V) | $I_{IH}$ | — | 40 | μA |
| Input low current ($OV_{DD}$ = Max, $V_{IN}$ = 0.5 V) | $I_{IL}$ | –600 | — | μA |

**Note:**

1.Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

# 9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8540.

## 9.1 Local Bus DC Electrical Characteristics

Table 35 provides the DC electrical characteristics for the local bus interface.

**Table 35. Local Bus DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($V_{IN}$ [1] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | $OV_{DD}$ - 0.2 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.2 | V |

**Note:**

1.Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 9.2 Local Bus AC Electrical Specifications

Table 36 describes the general timing parameters of the local bus interface of the MPC8540 with the DLL enabled.

**Table 36. Local Bus General Timing Parameters - DLL Enabled**

| Parameter | POR Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Local bus cycle time | | $t_{LBK}$ | 6.0 | — | ns | 2 |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | | $t_{LBKSKEW}$ | — | 150 | ps | 3, 9 |
| Input setup to local bus clock (except LUPWAIT) | | $t_{LBIVKH1}$ | 1.8 | — | ns | 4, 5, 8 |
| LUPWAIT input setup to local bus clock | | $t_{LBIVKH2}$ | 1.7 | — | ns | 4, 5 |
| Input hold from local bus clock (except LUPWAIT) | | $t_{LBIXKH1}$ | 0.5 | — | ns | 4, 5, 8 |
| LUPWAIT input hold from local bus clock | | $t_{LBIXKH2}$ | 1.0 | — | ns | 4, 5 |
| LALE output transition to LAD/LDP output transition (LATCH hold time) | | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |

**Table 36. Local Bus General Timing Parameters - DLL Enabled (continued)**

| Parameter | POR Configuration | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Local bus clock to output valid (except LAD/LDP and LALE) | TSEC2_TXD[6:5] = 00 | $t_{LBKHOV1}$ | — | 2.0 | ns | 4, 8 |
| | TSEC2_TXD[6:5] = 11 (default) | | | 3.5 | | |
| Local bus clock to data valid for LAD/LDP | TSEC2_TXD[6:5] = 00 | $t_{LBKHOV2}$ | — | 2.2 | ns | 4, 8 |
| | TSEC2_TXD[6:5] = 11 (default) | | | 3.7 | | |
| Local bus clock to address valid for LAD | TSEC2_TXD[6:5] = 00 | $t_{LBKHOV3}$ | — | 2.3 | ns | 4, 8 |
| | TSEC2_TXD[6:5] = 11 (default) | | | 3.8 | | |
| Local bus clock to LALE assertion | | $t_{LBKHOV4}$ | — | 2.3 | ns | 4, 8 |
| Output hold from local bus clock (except LAD/LDP and LALE) | TSEC2_TXD[6:5] = 00 | $t_{LBKHOX1}$ | 0.7 | — | ns | 4, 8 |
| | TSEC2_TXD[6:5] = 11 (default) | | 1.6 | | | |
| Output hold from local bus clock for LAD/LDP | TSEC2_TXD[6:5] = 00 | $t_{LBKHOX2}$ | 0.7 | — | ns | 4, 8 |
| | TSEC2_TXD[6:5] = 11 (default) | | 1.6 | | | |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | TSEC2_TXD[6:5] = 00 | $t_{LBKHOZ1}$ | — | 2.5 | ns | 7, 9 |
| | TSEC2_TXD[6:5] = 11 (default) | | | 3.8 | | |
| Local bus clock to output high impedance for LAD/LDP | TSEC2_TXD[6:5] = 00 | $t_{LBKHOZ2}$ | — | 2.5 | ns | 7, 9 |
| | TSEC2_TXD[6:5] = 11 (default) | | | 3.8 | | |

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for DLL enabled mode.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $OV_{DD}/2$.
4. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for DLL enabled to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of $t_{LBOTOT}$ is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins TSEC2_TXD[6:5].
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.
9. Guaranteed by design.

Figure 29 provides the test access port timing diagram.

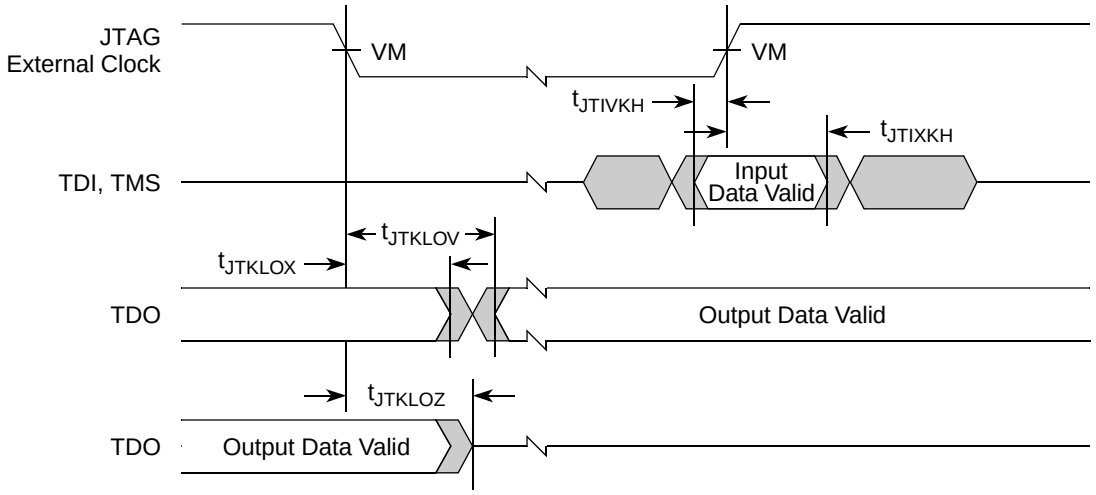



**Figure 29. Test Access Port Timing Diagram**

# 11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8540.

## 11.1 I²C DC Electrical Characteristics

Table 39 provides the DC electrical characteristics for the I²C interface of the MPC8540.

**Table 39. I²C DC Electrical Characteristics**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage level | $V_{IH}$ | $0.7 \times OV_{DD}$ | $OV_{DD}$+ 0.3 | V | |
| Input low voltage level | $V_{IL}$ | –0.3 | $0.3 \times OV_{DD}$ | V | |
| Low level output voltage | $V_{OL}$ | 0 | $0.2 \times OV_{DD}$ | V | 1 |
| Pulse width of spikes which must be suppressed by the input filter | $t_{I2KHKL}$ | 0 | 50 | ns | 2 |
| Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max) | $I_I$ | –10 | 10 | μA | 3 |
| Capacitance for each I/O pin | $C_I$ | — | 10 | pF | |

**Notes:**

1.Output voltage (open drain or open collector) condition = 3 mA sink current.

2.Refer to the *MPC8540 Integrated Processor Preliminary Reference Manual* for information on the digital filter used.

3.I/O pins will obstruct the SDA and SCL lines if $OV_{DD}$ is switched off.

**Table 44. PCI-X AC Timing Specifications at 133 MHz (continued)**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time | $t_{PCRHIX}$ | 0 | 50 | ns | 6, 12 |

**Notes:**

1. See the timing measurement conditions in the *PCI-X 1.0a Specification*.
2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
3. Setup time for point-to-point signals applies to $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ only. All other signals are bused.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
6. Maximum value is also limited by delay to the first transaction (time for $\overline{\text{HRESET}}$ high to first configuration access, $t_{PCRHFV}$). The PCI-X initialization pattern control signals after the rising edge of $\overline{\text{HRESET}}$ must be negated no later than two clocks before the first $\overline{\text{FRAME}}$ and must be floated no later than one clock before $\overline{\text{FRAME}}$ is asserted.
7. A PCI-X device is permitted to have the minimum values shown for $t_{PCKHOV}$ and $t_{CYC}$ only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
8. Device must meet this specification independent of how many outputs switch simultaneously.
9. The timing parameter $t_{PCIVKH}$ is a minimum of 1.4 ns rather than the minimum of 1.2 ns in the *PCI-X 1.0a Specification.*
10. The timing parameter $t_{PCRHFV}$ is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*
11. Guaranteed by characterization.
12. Guaranteed by design.

# 13 RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8540.

## 13.1 RapidIO DC Electrical Characteristics

RapidIO driver and receiver DC electrical characteristics are provided in Table 45 and Table 46, respectively.

**Table 45. RapidIO 8/16 LP-LVDS Driver DC Electrical Characteristics**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 5%.

| Characteristic | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Differential output high voltage | $V_{OHD}$ | 247 | 454 | mV | 1, 2 |
| Differential output low voltage | $V_{OLD}$ | –454 | –247 | mV | 1, 2 |
| Differential offset voltage | $\Delta V_{OSD}$ | — | 50 | mV | 1,3 |
| Output high common mode voltage | $V_{OHCM}$ | 1.125 | 1.375 | V | 1, 4 |
| Output low common mode voltage | $V_{OLCM}$ | 1.125 | 1.375 | V | 1, 5 |

**Table 45. RapidIO 8/16 LP-LVDS Driver DC Electrical Characteristics (continued)**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 5%.

| Characteristic | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Common mode offset voltage | $\Delta V_{OSCM}$ | — | 50 | mV | 1, 6 |
| Differential termination | $R_{TERM}$ | 90 | 220 | W | |
| Short circuit current (either output) | $\lvert I_{SS} \rvert$ | — | 24 | mA | 7 |
| Bridged short circuit current | $\lvert I_{SB} \rvert$ | — | 12 | mA | 8 |

**Notes:**

1.Bridged 100-Ω load.

2.See Figure 35(a).

3.Differential offset voltage = $\lvert V_{OHD}+V_{OLD} \rvert$. See Figure 35(b).

4.$V_{OHCM} = (V_{OA} + V_{OB})/2$ when measuring $V_{OHD}$.

5.$V_{OLCM} = (V_{OA} + V_{OB})/2$ when measuring $V_{OLD}$.

6.Common mode offset $\Delta V_{OSCM} = \lvert V_{OHCM} - V_{OLCM} \rvert$. See Figure 35(c).

7.Outputs shorted to $V_{DD}$ or GND.

8.Outputs shorted together.

**Table 46. RapidIO 8/16 LP-LVDS Receiver DC Electrical Characteristics**

| Characteristic | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Voltage at either input | $V_I$ | 0 | 2.4 | V | |
| Differential input high voltage | $V_{IHD}$ | 100 | 600 | mV | 1 |
| Differential input low voltage | $V_{ILD}$ | –600 | –100 | mV | 1 |
| Common mode input range (referenced to receiver ground) | $V_{ICM}$ | 0.050 | 2.350 | V | 2 |
| Input differential resistance | $R_{IN}$ | 90 | 110 | W | |

**Notes:**

1.Over the common mode range.

2.Limited by $V_I$. See Figure 42.

## 13.3.2 RapidIO Receiver AC Timing Specifications

The RapidIO receiver AC timing specifications are provided in Table 50. A receiver shall comply with the specifications for each data rate/frequency for which operation of the receiver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The specifications apply over the receiver common mode and differential input voltage ranges.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7])

**Table 50. RapidIO Receiver AC Timing Specifications—500 Mbps Data Rate**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Duty cycle of the clock input | DC | 47 | 53 | % | 1, 5 |
| Data valid | DV | 1080 | | ps | 2 |
| Allowable static skew between any two data inputs within a 8-/9-bit group | $t_{DPAIR}$ | — | 380 | ps | 3 |
| Allowable static skew of data inputs to associated clock | $t_{SKEW,PAIR}$ | –300 | 300 | ps | 4 |

**Notes:**
1.Measured at $V_{ID}$ = 0 V.
2.Measured using the RapidIO receive mask shown in Figure 40.
3.See Figure 43.
4.See Figure 42 and Figure 43.
5.Guaranteed by design.

**Table 51. RapidIO Receiver AC Timing Specifications—750 Mbps Data Rate**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Duty cycle of the clock input | DC | 47 | 53 | % | 1, 5 |
| Data valid | DV | 600 | — | ps | 2 |
| Allowable static skew between any two data inputs within a 8-/9-bit group | $t_{DPAIR}$ | — | 400 | ps | 3 |
| Allowable static skew of data inputs to associated clock | $t_{SKEW,PAIR}$ | –267 | 267 | ps | 4 |

**Notes:**
1.Measured at $V_{ID}$ = 0 V.
2.Measured using the RapidIO receive mask shown in Figure 40.
3.See Figure 43.
4.See Figure 42 and Figure 43.
5.Guaranteed by design.

**Table 52. RapidIO Receiver AC Timing Specifications—1 Gbps Data Rate**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Duty cycle of the clock input | DC | 47 | 53 | % | 1, 5 |
| Data valid | DV | 425 | — | ps | 2 |
| Allowable static skew between any two data inputs within a 8-/9-bit group | $t_{DPAIR}$ | — | 300 | ps | 3 |
| Allowable static skew of data inputs to associated clock | $t_{SKEW,PAIR}$ | –200 | 200 | ps | 4 |

**Notes:**
1.Measured at $V_{ID}$ = 0 V.
2.Measured using the RapidIO receive mask shown in Figure 40.
3.See Figure 43.
4.See Figure 42 and Figure 43.
5.Guaranteed by design.

The compliance of receiver input signals RD[0:15] and RFRAME with their minimum data valid window (DV) specification shall be determined by generating an eye pattern for each of the data signals and comparing the eye pattern of each data signal with the RapidIO receive mask shown in Figure 40. The value of X2 used to construct the mask shall be $(1 – DV_{min})/2$. The ±100 mV minimum data valid and ±600 mV maximum input voltage values are from the DC specification. A signal is compliant with the data valid window specification if and only if the receive mask can be positioned on the signal's eye pattern such that the eye pattern falls entirely within the unshaded portion of the mask.

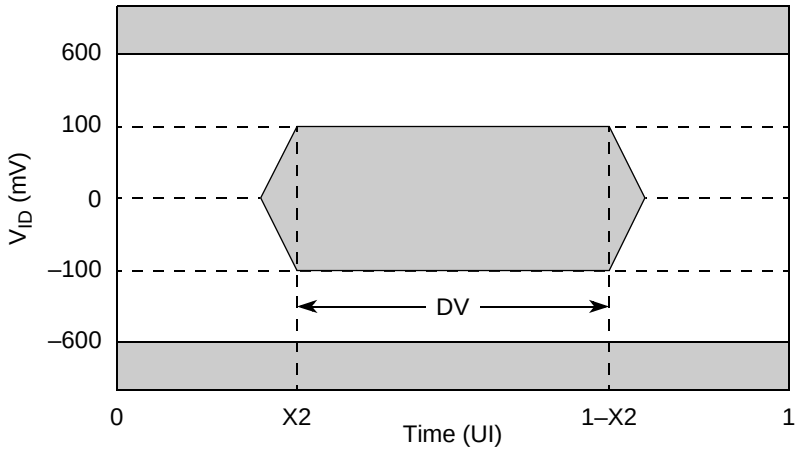



**Figure 40. RapidIO Receive Mask**

The eye pattern for a data signal is generated by making a large number of recordings of the signal and then overlaying the recordings. The number of recordings used to generate the eye shall be large enough that further increasing the number of recordings used does not cause the resulting eye pattern to change from one that complies with the RapidIO receive mask to one that does not. Each data signal in the interface shall be carrying random or pseudo-random data when the recordings are made. If pseudo-random data is used, the length of the pseudo-random sequence (repeat length) shall be long

# 14 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions.

## 14.1 Package Parameters for the MPC8540 FC-PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip plastic ball grid array (FC-PBGA).

| | |
|---|---|
| Die size | 12.2 mm × 9.5 mm |
| Package outline | 29 mm × 29 mm |
| Interconnects | 783 |
| Pitch | 1 mm |
| Minimum module height | 3.07 mm |
| Maximum module height | 3.75 mm |
| Solder Balls | 62 Sn/36 Pb/2 Ag |
| Ball diameter (typical) | 0.5 mm |

**Table 53. MPC8540 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $\overline{\text{IRQ\_OUT}}$ | AB21 | O | $OV_{DD}$ | 2, 4 |
| **Ethernet Management Interface** | | | | |
| EC_MDC | F1 | O | $OV_{DD}$ | 5, 9 |
| EC_MDIO | E1 | I/O | $OV_{DD}$ | |
| **Gigabit Reference Clock** | | | | |
| EC_GTX_CLK125 | E2 | I | $LV_{DD}$ | |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 1)** | | | | |
| TSEC1_TXD[7:4] | A6, F7, D7, C7 | O | $LV_{DD}$ | 5, 9 |
| TSEC1_TXD[3:0] | B7, A7, G8, E8 | O | $LV_{DD}$ | 9, 19 |
| TSEC1_TX_EN | C8 | O | $LV_{DD}$ | 11 |
| TSEC1_TX_ER | B8 | O | $LV_{DD}$ | |
| TSEC1_TX_CLK | C6 | I | $LV_{DD}$ | |
| TSEC1_GTX_CLK | B6 | O | $LV_{DD}$ | 18 |
| TSEC1_CRS | C3 | I | $LV_{DD}$ | |
| TSEC1_COL | G7 | I | $LV_{DD}$ | |
| TSEC1_RXD[7:0] | D4, B4, D3, D5, B5, A5, F6, E6 | I | $LV_{DD}$ | |
| TSEC1_RX_DV | D2 | I | $LV_{DD}$ | |
| TSEC1_RX_ER | E5 | I | $LV_{DD}$ | |
| TSEC1_RX_CLK | D6 | I | $LV_{DD}$ | |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 2)** | | | | |
| TSEC2_TXD[7:2] | B10, A10, J10, K11,J11, H11 | O | $LV_{DD}$ | 5, 9 |
| TSEC2_TXD[1:0] | G11, E11 | O | $LV_{DD}$ | |
| TSEC2_TX_EN | B11 | O | $LV_{DD}$ | 11 |
| TSEC2_TX_ER | D11 | O | $LV_{DD}$ | |
| TSEC2_TX_CLK | D10 | I | $LV_{DD}$ | |
| TSEC2_GTX_CLK | C10 | O | $LV_{DD}$ | 18 |
| TSEC2_CRS | D9 | I | $LV_{DD}$ | |
| TSEC2_COL | F8 | I | $LV_{DD}$ | |
| TSEC2_RXD[7:0] | F9, E9, C9, B9, A9, H9, G10, F10 | I | $LV_{DD}$ | |
| TSEC2_RX_DV | H8 | I | $LV_{DD}$ | |
| TSEC2_RX_ER | A8 | I | $LV_{DD}$ | |

# 15 Clocking

This section describes the PLL configuration of the MPC8540. Note that the platform clock is identical to the CCB clock.

## 15.1 Clock Ranges

Table 54 provides the clocking specifications for the processor core and Table 55 provides the clocking specifications for the memory bus.

**Table 54. Processor Core Clocking Specifications**

| Characteristic | Maximum Processor Core Frequency | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | 667 MHz | | 833 MHz | | 1 GHz | | | |
| | Min | Max | Min | Max | Min | Max | | |
| e500 core processor frequency | 400 | 667 | 400 | 833 | 400 | 1000 | MHz | 1, 2, 3 |

**Notes**:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, “Platform/System PLL Ratio,” and Section 15.3, “e500 Core PLL Ratio,” for ratio settings.
2. )The minimum e500 core frequency is based on the minimum platform frequency of 200 MHz.
3. )The 1.0 GHz core frequency is based on a 1.3 V VDD supply voltage.

**Table 55. Memory Bus Clocking Specifications**

| Characteristic | Maximum Processor Core Frequency | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | 667 MHz | | 833 MHz | | 1 GHz | | | |
| | Min | Max | Min | Max | Min | Max | | |
| Memory bus frequency | 100 | 166 | 100 | 166 | 100 | 166 | MHz | 1, 2, 3 |

**Notes:**

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, “Platform/System PLL Ratio,” and Section 15.3, “e500 Core PLL Ratio,” for ratio settings.
2. The memory bus speed is half of the DDR data rate, hence, half of the platform clock frequency.
3. )The 1.0 GHz core frequency is based on a 1.3 V VDD supply voltage.

**Table 59. Package Thermal Characteristics (continued)**

| Characteristic | Symbol | Value | Unit | Notes |
|---|---|---|---|---|
| Junction-to-case thermal | $R_{\theta JC}$ | 0.8 | •C/W | 4 |

**Notes**

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-6 with the board horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). Cold plate temperature is used for case temperature; measured value includes the thermal resistance of the interface layer.

## 16.2 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 45. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force.

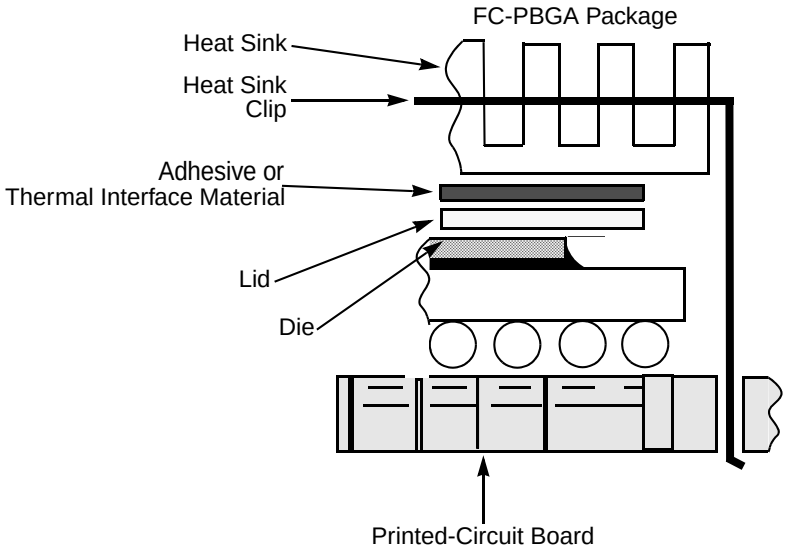



**Figure 45. Package Exploded Cross-Sectional View with Several Heat Sink Options**

The system board designer can choose between several types of heat sinks to place on the MPC8540. There are several commercially-available heat sinks from the following vendors:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

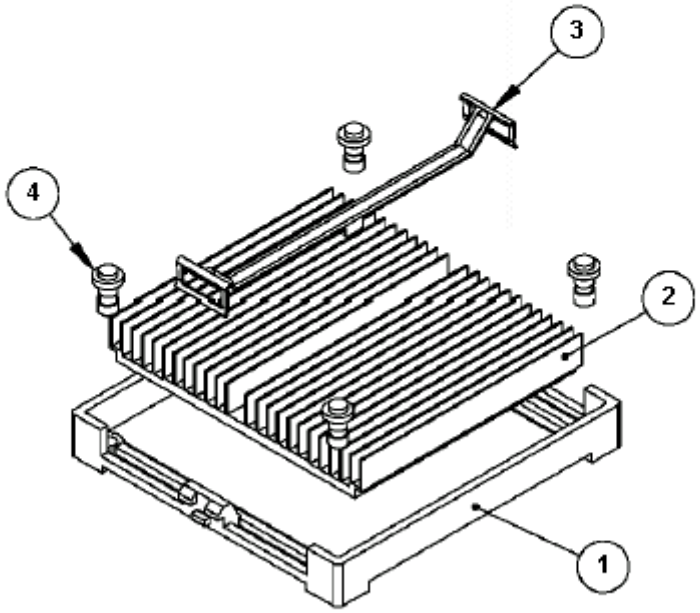
| | |
|---|---|
| Alpha Novatech<br>473 Sapena Ct. #15<br>Santa Clara, CA 95054<br>Internet: www.alphanovatech.com | 408-749-7601 |
| International Electronic Research Corporation (IERC)<br>413 North Moss St.<br>Burbank, CA 91502<br>Internet: www.ctscorp.com | 818-842-7277 |
| Millennium Electronics (MEI)<br>Loroco Sites<br>671 East Brokaw Road<br>San Jose, CA 95112<br>Internet: www.mei-millennium.com | 408-436-8770 |
| Tyco Electronics<br>Chip Coolers™<br>P.O. Box 3668<br>Harrisburg, PA 17105-3668<br>Internet: www.chipcoolers.com | 800-522-6752 |
| Wakefield Engineering<br>33 Bridge St.<br>Pelham, NH 03076<br>Internet: www.wakefield.com | 603-635-5102 |

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the MPC8540 to function in various environments.

### 16.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8540 thermal model is shown in Figure 46. Five cuboids are used to represent this device. To simplify the model, the solder balls and substrate are modeled as a single block 29x29x1.47 mm with the conductivity adjusted accordingly. For modeling, the planar dimensions of the die are rounded to the nearest mm, so the die is modeled as 10x12 mm at a thickness of 0.76 mm. The bump/underfill layer is modeled as a collapsed resistance between the die and substrate assuming a conductivity of 0.6 in-plane and 1.9 W/m•K in the thickness dimension of 0.76 mm. The lid attach adhesive is also modeled as a collapsed resistance with dimensions of 10x12x0.050 mm and the conductivity of 1 W/m•K. The nickel plated copper lid is modeled as 12x14x1 mm. Note that the die and lid are not centered on the substrate; there is a 1.5 mm offset documented in the case outline drawing in Figure 44.

| Item No | QTY | MEI PN | Description |
|---|---|---|---|
| 1 | 1 | MFRAME-2000 | HEATSINK FRAME |
| 2 | 1 | MSNK-1120 | EXTRUDED HEATSINK |
| 3 | 1 | MCLIP-1013 | CLIP |
| 4 | 4 | MPPINS-1000 | FRAME ATTACHMENT PINS |




Illustrative source provided by
Millennium Electronics (MEI)

**Figure 51. Exploded Views (2) of a Heat Sink Attachment using a Plastic Fence**

The die junction-to-ambient and the heat sink-to-ambient thermal resistances are common figure-of-merits used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature: airflow, board population (local heat flux of adjacent components), system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the boards, as well as, system-level designs.

**Table 61. Document Revision History (continued)**

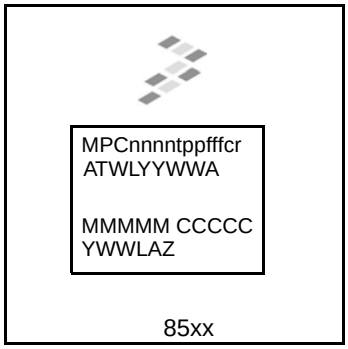
| Rev. No. | Substantive Change(s) |
|---|---|
| 2.0 | Section 1.1—Updated features list to coincide with latest version of the reference manual<br>Table 1 and Table 2—Addition of SYSCLK to $OV_{IN}$<br>Table 2—Addition of notes 1 and 2<br>Table 3—Addition of note 1<br>Table 5—New<br>Section 4—New<br>Table 13—Addition of $I_{VREF}$<br>Removed Figure 4 DDR SRAM Input TIming Diagram<br>Table 15—Modified maximum values for $t_{DISKEW}$<br>Table 16—Added MSYNC_OUT to tMCKSKEW2<br>Figure 5—New<br>Section 6.2.1—Removed Figure 4, “DDR SDRAM Input Timing Diagram”<br>Section 8.1—Removed references to 2.5 V from first paragraph<br>Figure 8—New<br>Table 21 and Table 22—Modified “conditions” for $I_{IH}$ and $I_{IL}$<br>Table 23—Addition of min and max for GTX_CLK125 reference clock duty cycle<br>Table 27 —Addition of min and max for GTX_CLK125 reference clock duty cycle<br>Table 29—Addition of min and max for GTX_CLK125 reference clock duty cycle<br>Table 30—VOH min and conditions; $I_{IH}$ and $I_{IL}$ conditions<br>Table 31—Min and max for $t_{MTXR}$ and $t_{MTXF}$<br>Table 32—Min and max for $t_{MRXR}$ and $t_{MRXF}$<br>Figure 23 and Figure 24—Changed LSYNC_IN to Internal clock at top of each figure<br>Figure 18—New<br>Figure 18—New<br>Table 36—Removed row for tLBKHOX3<br>Table 43—New (AC timing of PCI-X at 66 MHz)<br>Table 53—Addition of note 19<br>Figure 55—Addition of jumper and note at top of diagram<br>Table 55: Changed max bus freq for 667 core to 166<br>Section 16.2.1—Modified first paragraph<br>Figure 46—Modified<br>Figure 47—New<br>Table 59—Modified thermal resistance data<br>Section 16.2.4.2—Modified first and second paragraphs |

**Table 61. Document Revision History (continued)**

| Rev. No. | Substantive Change(s) |
|---|---|
| 1.2 | Section 1.1.1—Updated feature list.<br>Section 1.2.1.1—Updated notes for Table 1.<br>Section 1.2.1.2—Removed 5-V PCI interface overshoot and undershoot figure.<br>Section 1.2.1.3—Added this section to summarize impedance driver settings for various interfaces.<br>Section 1.4—Updated rows in Reset Initialization timing specifications table. Added a table with DLL and PLL timing specifications.<br>Section 1.5.2.2—Updated note 6 of DDR SDRAM Output AC Timing Specifications table.<br>Section 1.7—Changed the minimum input low current from -600 to -15 μA for the RGMII DC electrical characteristics.<br>Section 1.8.2—Changed LCS[3:4] to TSEC1_TXD[6:5] in. Updated notes regarding LCS[3:4].<br>Section 1.13.2—Updated the mechanical dimensions diagram for the package.<br>Section 1.13.3—Updated the notes for LBCTL, TRIG_OUT, and ASLEEP. Corrected pin assignments for IIC_SDA and IIC_SCL. Corrected reserved pin assignment of V11 to U11. V11 is actually $\overline{\text{PCI\_STOP}}$.<br>Section 1.14.1—Updated the table for frequency options with respect to platform/CCB frequencies.<br>Section 1.14.4—Edited Frequency options with respect to memory bus speeds. |
| 1.1 | Section 1.6.1—Added symbols and note for the GTX_CLK125 timing parameters.<br>Section 1.11.3—Updated pin list table: LGPL5/LSDAMUX to LGPL5, LA[27:29] and LA[30:31] to LA[27:31], FEC_TXD[0:3] to FEC_TXD[3:0], FEC_RXD[0:3] to FEC_RXD[3:0], TRST to $\overline{\text{TRST}}$, added GBE Clocking section and EC_GTX_CLK125 signal.<br>Updated thermal model information to match current offering. |
| 1 | Original Customer Version. |

## 19.2 Part Marking

Parts are marked as the example shown in Figure 56.




FC-PBGA

**Notes:**

MMMMM is the 5-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.
YWWLAZ is the assembly traceability code.

**Figure 56. Part Marking for FC-PBGA Device**