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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	833MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1), 10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8540px833lb

  - Interrupts can be routed to the e500 core's standard or critical interrupt inputs
  - Interrupt summary registers allow fast identification of interrupt source
- I^2C controller
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the I^2C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I^2C addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
  - Programming model compatible with the original 16450 UART and the PC16550D
- 10/100 fast Ethernet controller (FEC)
  - Operates at 10 to 100 megabits per second (Mbps) as a device debug and maintenance port
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 166 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
  - Three protocol engines available on a per chip select basis:
    - General purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-,16-, or 32-bit)
- Two three-speed (10/100/1Gb) Ethernet controllers (TSECs)
  - Dual IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab compliant controllers
  - Support for different Ethernet physical interfaces:
    - 10/100/1Gb Mbps IEEE 802.3 GMII
    - 10/100 Mbps IEEE 802.3 MII
    - 10 Mbps IEEE 802.3 MII
    - 1000 Mbps IEEE 802.3z TBI
    - 10/100/1Gb Mbps RGMII/RTBI
  - Full- and half-duplex support

4 Clock Timing

4.1 System Clock Timing

Table 7 provides the system clock (SYSCLK) AC timing specifications for the MPC8540.

Table 7. SYSCLK AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	—	—	166	MHz	1
SYSCLK cycle time	t_{SYSCLK}	6.0	—	—	ns	
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KHKL}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	+/- 150	ps	4, 5

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2, "Platform/System PLL Ratio," and Section 15.3, "e500 Core PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. For spread spectrum clocking, guidelines are +/-1% of the input frequency with a maximum of 60 kHz of modulation regardless of the input frequency.

4.2 TSEC Gigabit Reference Clock Timing

Table 7 provides the TSEC gigabit reference clock (EC_GTX_CLK125) AC timing specifications for the MPC8540.

Table 8. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	
EC_GTX_CLK125 rise and fall time LV_{DD}=2.5 LV_{DD}=3.3	t_{G125R}, t_{G125F}	—	—	 0.75 1	ns	2
EC_GTX_CLK125 duty cycle GMII, TBI RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	1,3

Notes:

1. Timing is guaranteed by design and characterization.
2. Rise and fall times for EC_GTX_CLK125 are measured from 0.5V and 2.0V for LV_{DD}=2.5V, and from 0.6 and 2.7V for LV_{DD}=3.3V.
3. EC_GTX_CLK125 is used to generate GTX clock for TSEC transmitter with 2% degradation EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as PHY device can tolerate the duty cycle generated by GTX_CLK of TSEC.

Table 16. DDR SDRAM Output AC Timing Specifications–DLL Mode (continued)

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDSHME}	1.5	4.0	ns	7, 8

Notes:

1.The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (OX or DX). For example, t_{DDKHOV} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (O) are valid (V) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.

2.All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.

3.Maximum possible clock skew between a clock MCK[n] and its relative inverse clock $\overline{\text{MCK}}$[n], or between a clock MCK[n] and a relative clock MCK[m] or MSYNC_OUT. Skew measured between complementary signals at $GV_{DD}/2$.

4.ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$ and MDQ/MECC/MDM/MDQS.

5.Note that t_{DDSHMH} follows the symbol conventions described in note 1. For example, t_{DDSHMH} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) until the MDQS signal is valid (MH). t_{DDSHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. These controls allow the relationship between the synchronous clock control timing and the source-synchronous DQS domain to be modified by the user. For best turnaround times, these may need to be set to delay t_{DDSHMH} an additional $0.25t_{MCK}$. This will also affect t_{DDSHMP} and t_{DDSHME} accordingly. See the *MPC8540 PowerQUICC III Integrated Host Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.

6.Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8540.

7.All outputs are referenced to the rising edge of MSYNC_IN (S) at the pins of the MPC8540. Note that t_{DDSHMP} follows the symbol conventions described in note 1. For example, t_{DDSHMP} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) for the duration of the MDQS signal precharge period (MP).

8.Guaranteed by design.

9.Guaranteed by characterization.

Figure 5 provides the AC test load for the DDR bus.

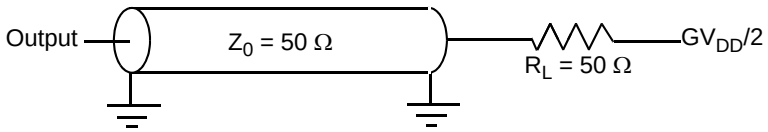

Figure 5. DDR AC Test Load

Table 17. DDR SDRAM Measurement Conditions

Symbol	DDR	Unit	Notes
V_{TH}	MV_{REF} ± 0.31 V	V	1
V_{OUT}	0.5 × GV_{DD}	V	2

Notes:

1.Data input threshold measurement point.

2.Data output measurement point.

8.2.2.2 MII Receive AC Timing Specifications

Table 26 provides the MII receive AC timing specifications.

Table 26. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX} [3]	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise and fall time	t_{MRXR}, t_{MRXF} [2,3]	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 11 shows the MII receive AC timing diagram.

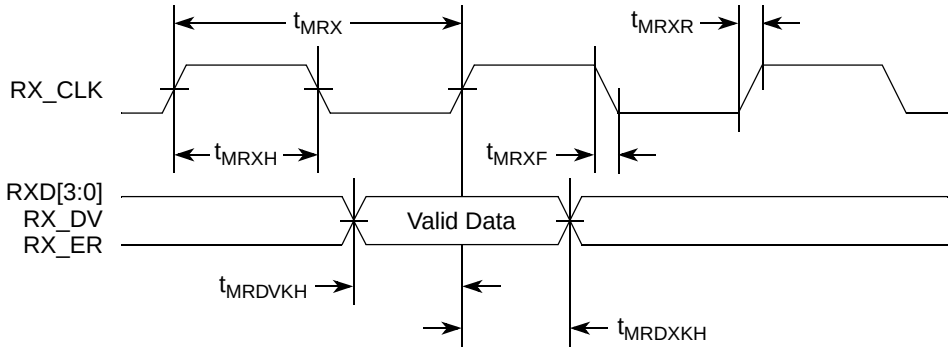

Figure 11. MII Receive AC Timing Diagram

8.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.3.1 TBI Transmit AC Timing Specifications

Table 27 provides the TBI transmit AC timing specifications.

Table 27. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t_{TTKHDX}	1.0	—	—	ns
GTX_CLK clock rise and fall time	t_{TTXR}, t_{TTXF} [2,3]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 12 shows the TBI transmit AC timing diagram.

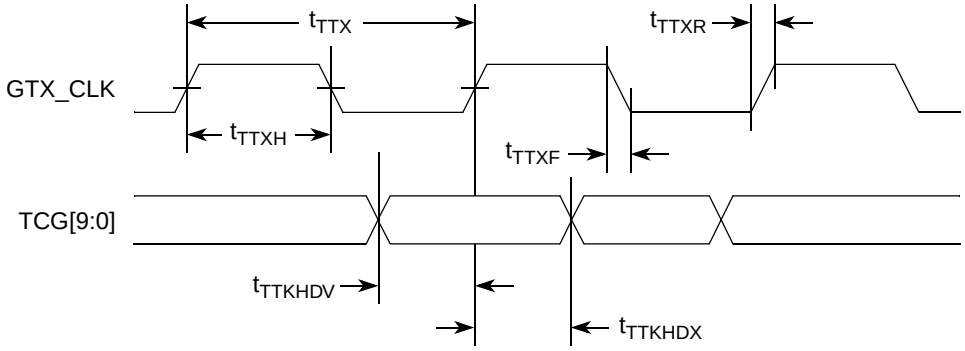

Figure 12. TBI Transmit AC Timing Diagram

Table 30. MII DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3 V	OV_{DD}	3.13	3.47	V
Output high voltage (OV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.40	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} = Min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	1.70	—	V
Input low voltage	V_{IL}	–0.3	0.90	V
Input high current (V_{IN}= OV_{DD} [1])	I_{IH}	—	40	μA
Input low current (V_{IN}= GND [1])	I_{IL}	–600	—	μA

Note:

1.Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

8.3.2 MII AC Electrical Specifications

This section describes the MII transmit and receive AC specifications.

8.3.2.1 MII Transmit AC Timing Specifications

Table 31 provides the MII transmit AC timing specifications.

Table 31. MII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise and fall time	t_{MTXR}, t_{MTXF} [2,3]	1.0	—	4.0	ns

Note:

1.The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) from the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII (M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2.Signal timings are measured at 0.7 V and 1.9 V voltage levels.

3.Guaranteed by design.

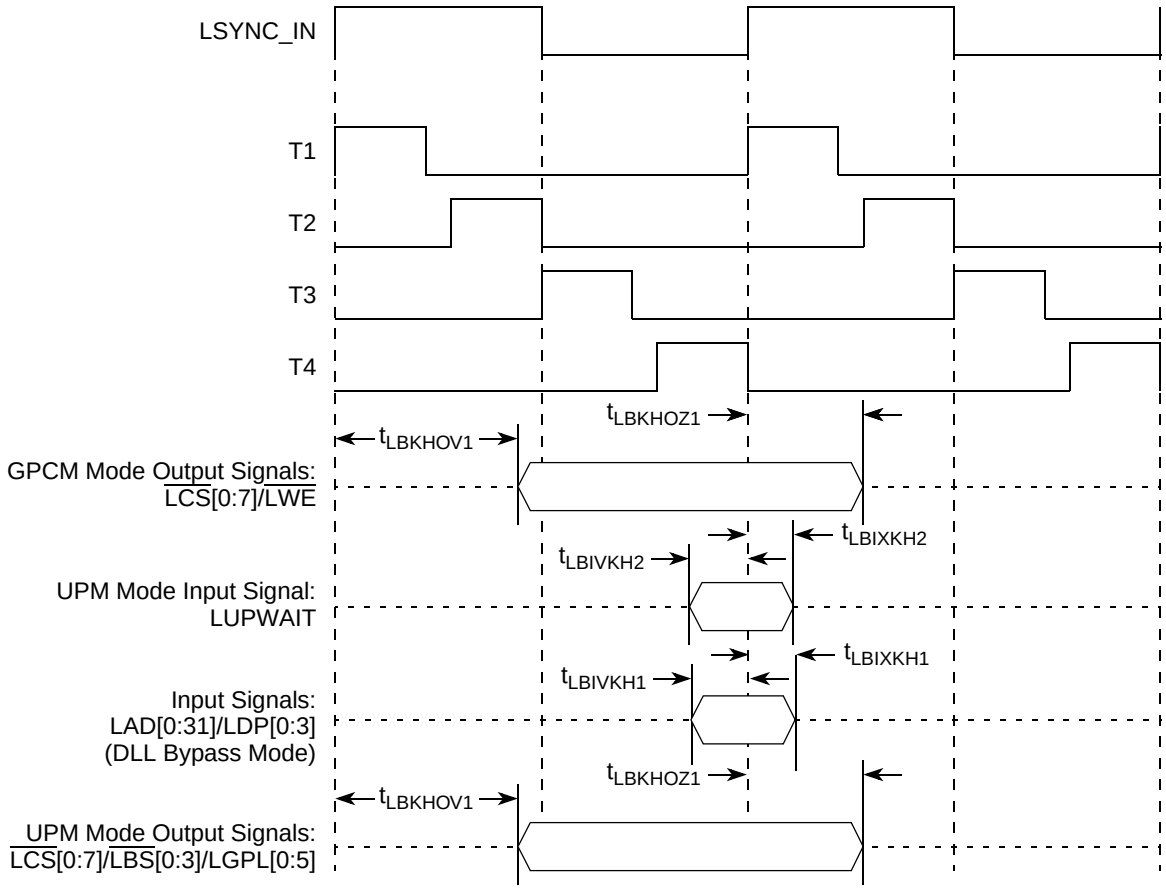

Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Enabled)

Figure 29 provides the test access port timing diagram.

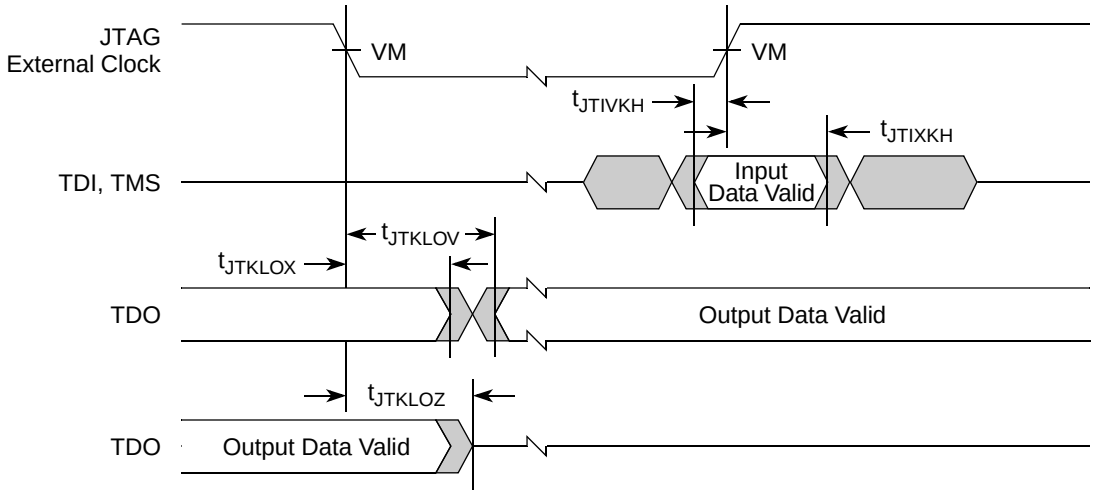

Figure 29. Test Access Port Timing Diagram

11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8540.

11.1 I²C DC Electrical Characteristics

Table 39 provides the DC electrical characteristics for the I²C interface of the MPC8540.

Table 39. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	OV_{DD}+ 0.3	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	μA	3
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:

1.Output voltage (open drain or open collector) condition = 3 mA sink current.

2.Refer to the *MPC8540 Integrated Processor Preliminary Reference Manual* for information on the digital filter used.

3.I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

Figure 31 shows the AC timing diagram for the I^2C bus.

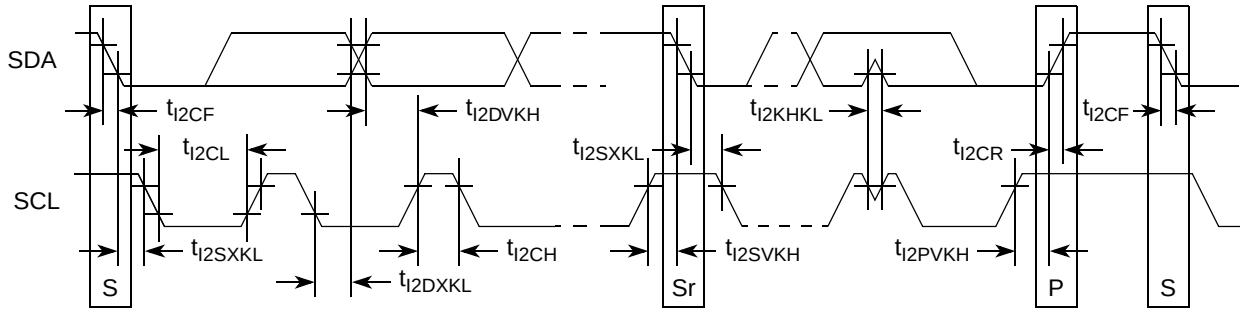

Figure 31. I^2C Bus AC Timing Diagram

12 PCI/PCI-X

This section describes the DC and AC electrical specifications for the PCI/PCI-X bus of the MPC8540.

12.1 PCI/PCI-X DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the PCI/PCI-X interface of the MPC8540.

Table 41. PCI/PCI-X DC Electrical Characteristics [1]

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [2] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Notes:

1.Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.

2.Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

The eye pattern for a data signal is generated by making a large number of recordings of the signal and then overlaying the recordings. The number of recordings used to generate the eye shall be large enough that further increasing the number of recordings used does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not. Each data signal in the interface shall be carrying random or pseudo-random data when the recordings are made. If pseudo-random data is used, the length of the pseudo-random sequence (repeat length) shall be long enough that increasing the length of the sequence does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not comply with the mask. The data carried by any given data signal in the interface may not be correlated with the data carried by any other data signal in the interface. The zero-crossings of the clock associated with a data signal shall be used as the timing reference for aligning the multiple recordings of the data signal when the recordings are overlaid.

While the method used to make the recordings and overlay them to form the eye pattern is not specified, the method used shall be demonstrably equivalent to the following method. The signal under test is repeatedly recorded with a digital oscilloscope in infinite persistence mode. Each recording is triggered by a zero-crossing of the clock associated with the data signal under test. Roughly half of the recordings are triggered by positive-going clock zero-crossings and roughly half are triggered by negative-going clock zero-crossings. Each recording is at least 1.9 UI in length (to ensure that at least one complete eye is formed) and begins 0.5 UI before the trigger point (0.5 UI before the associated clock zero-crossing). Depending on the length of the individual recordings used to generate the eye pattern, one or more complete eyes will be formed. Regardless of the number of eyes, the eye whose center is immediately to the right of the trigger point is the eye used for compliance testing.

An example of an eye pattern generated using the above method with recordings 3 UI in length is shown in Figure 39. In this example, there is no skew between the signal under test and the associated clock used to trigger the recordings. If skew was present, the eye pattern would be shifted to the left or right relative to the oscilloscope trigger point.

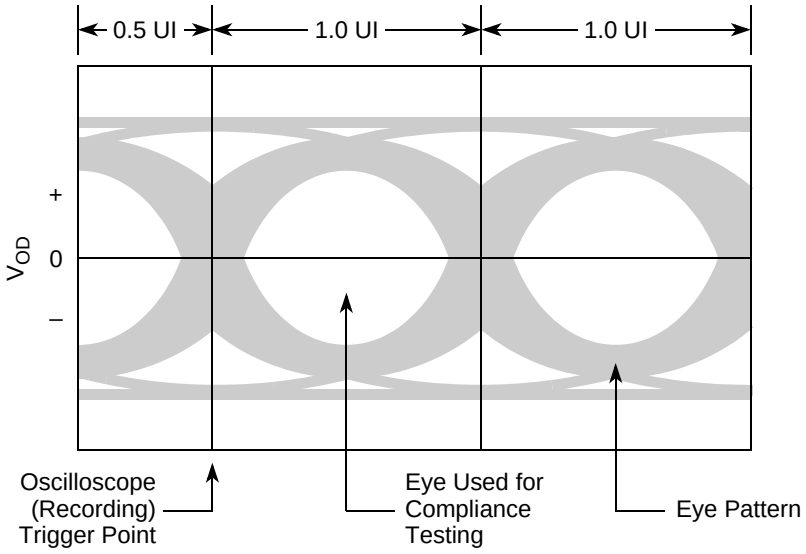

Figure 39. Example Driver Output Eye Pattern

Table 52. RapidIO Receiver AC Timing Specifications—1 Gbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1, 5
Data valid	DV	425	—	ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}	—	300	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–200	200	ps	4

Notes:
1.Measured at V_{ID} = 0 V.
2.Measured using the RapidIO receive mask shown in Figure 40.
3.See Figure 43.
4.See Figure 42 and Figure 43.
5.Guaranteed by design.

The compliance of receiver input signals RD[0:15] and RFRAME with their minimum data valid window (DV) specification shall be determined by generating an eye pattern for each of the data signals and comparing the eye pattern of each data signal with the RapidIO receive mask shown in Figure 40. The value of X2 used to construct the mask shall be $(1 – DV_{min})/2$. The ±100 mV minimum data valid and ±600 mV maximum input voltage values are from the DC specification. A signal is compliant with the data valid window specification if and only if the receive mask can be positioned on the signal's eye pattern such that the eye pattern falls entirely within the unshaded portion of the mask.

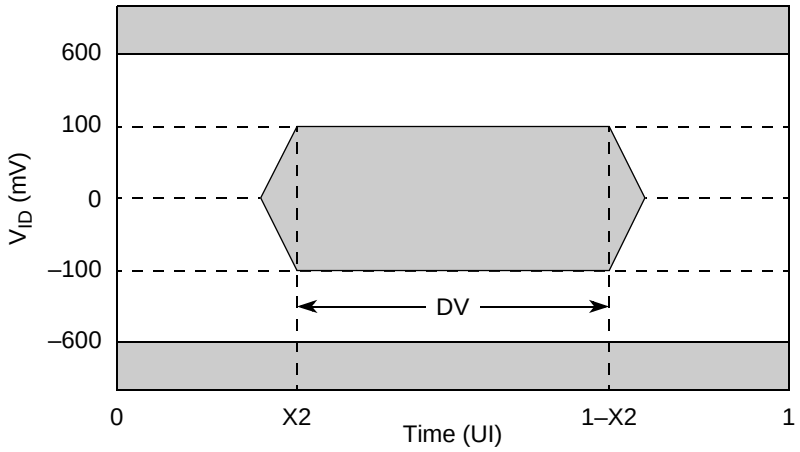

Figure 40. RapidIO Receive Mask

The eye pattern for a data signal is generated by making a large number of recordings of the signal and then overlaying the recordings. The number of recordings used to generate the eye shall be large enough that further increasing the number of recordings used does not cause the resulting eye pattern to change from one that complies with the RapidIO receive mask to one that does not. Each data signal in the interface shall be carrying random or pseudo-random data when the recordings are made. If pseudo-random data is used, the length of the pseudo-random sequence (repeat length) shall be long

Figure 42 shows the definitions of the data to clock static skew parameter $t_{SKEW,PAIR}$ and the data valid window parameter DV. The data and frame bits are those that are associated with the clock. The figure applies for all zero-crossings of the clock. All of the signals are differential signals. V_D represents V_{OD} for the transmitter and V_{ID} for the receiver. The center of the eye is defined as the midpoint of the region in which the magnitude of the signal voltage is greater than or equal to the minimum DV voltage.

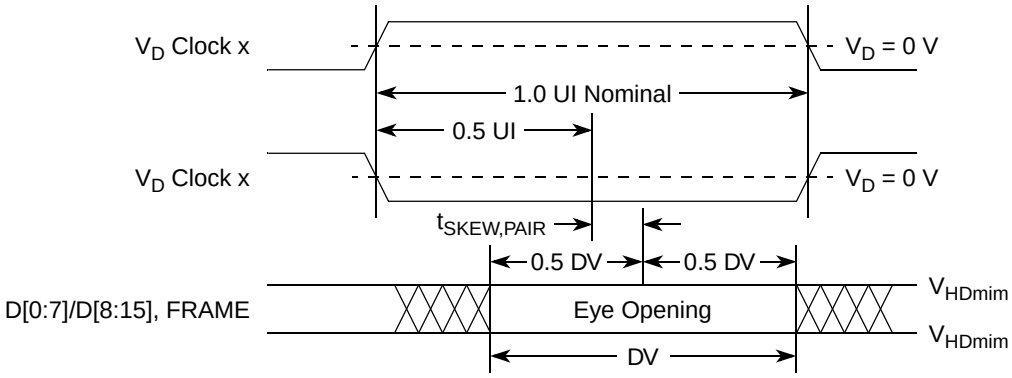

Figure 42. Data to Clock Skew

Figure 43 shows the definition of the data to data static skew parameter t_{DPAIR} and how the skew parameters are applied.

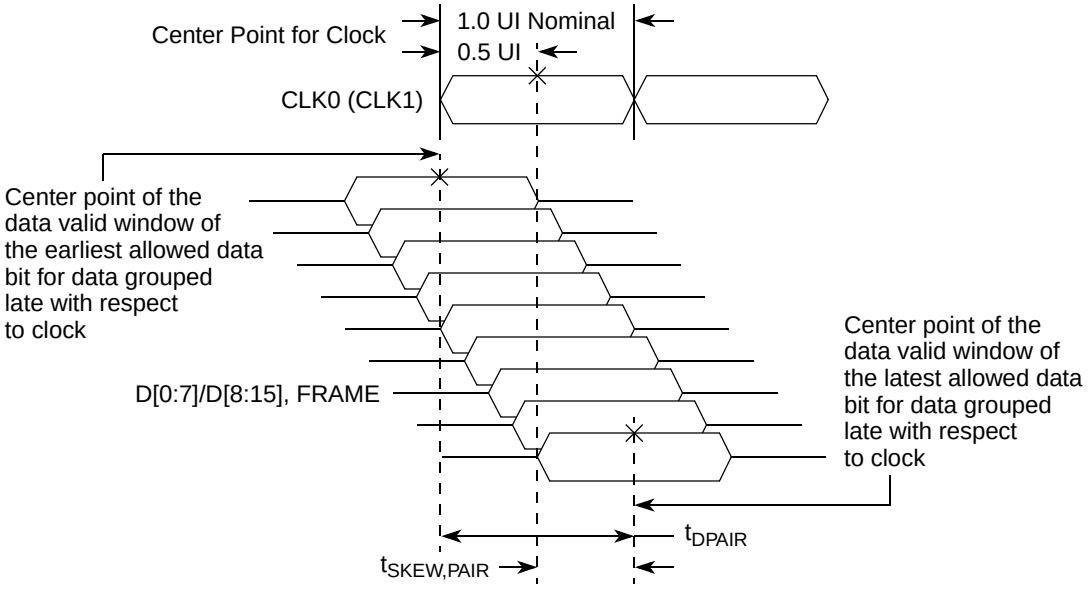

Figure 43. Static Skew Diagram

Table 53. MPC8540 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface				
MDQ[0:63]	M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12	I/O	GV_{DD}	
MECC[0:7]	N20, M20, L19, E19, C21, A21, G19, A19	I/O	GV_{DD}	
MDM[0:8]	L24, H28, F24, L21, E18, E16, G14, B13, M19	O	GV_{DD}	
MDQS[0:8]	L26, J25, D25, A22, H18, F16, F14, C13, C20	I/O	GV_{DD}	
MBA[0:1]	B18, B19	O	GV_{DD}	
MA[0:14]	N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13	O	GV_{DD}	
$\overline{\text{MWE}}$	D17	O	GV_{DD}	
$\overline{\text{MRAS}}$	F17	O	GV_{DD}	
$\overline{\text{MCAS}}$	J16	O	GV_{DD}	
$\overline{\text{MCS}}$[0:3]	H16, G16, J15, H15	O	GV_{DD}	
MCKE[0:1]	E26, E28	O	GV_{DD}	11
MCK[0:5]	J20, H25, A15, D20, F28, K14	O	GV_{DD}	
$\overline{\text{MCK}}$[0:5]	F20, G27, B15, E20, F27, L14	O	GV_{DD}	
MSYNC_IN	M28	I	GV_{DD}	
MSYNC_OUT	N28	O	GV_{DD}	
Local Bus Controller Interface				
LA[27]	U18	O	OV_{DD}	5, 9
LA[28:31]	T18, T19, T20, T21	O	OV_{DD}	7, 9
LAD[0:31]	AD26, AD27, AD28, AC26, AC27, AC28, AA22, AA23, AA26, Y21, Y22, Y26, W20, W22, W26, V19, T22, R24, R23, R22, R21, R18, P26, P25, P20, P19, P18, N22, N23, N24, N25, N26	I/O	OV_{DD}	
LALE	V21	O	OV_{DD}	8, 9
LBCTL	V20	O	OV_{DD}	9
LCKE	U23	O	OV_{DD}	
LCLK[0:2]	U27, U28, V18	O	OV_{DD}	
$\overline{\text{LCS}}$[0:4]	Y27, Y28, W27, W28, R27	O	OV_{DD}	18
$\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$	R28	I/O	OV_{DD}	1

Table 53. MPC8540 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
System Control				
$\overline{\text{HRESET}}$	AH16	I	OV_{DD}	
$\overline{\text{HRESET\_REQ}}$	AG20	O	OV_{DD}	
$\overline{\text{SRESET}}$	AF20	I	OV_{DD}	
$\overline{\text{CKSTP\_IN}}$	M11	I	OV_{DD}	
$\overline{\text{CKSTP\_OUT}}$	G1	O	OV_{DD}	2, 4
Debug				
TRIG_IN	N12	I	OV_{DD}	
TRIG_OUT/READY	G2	O	OV_{DD}	6, 9, 19
MSRCID[0:1]	J9, G3	O	OV_{DD}	5, 6, 9
MSRCID[2:4]	F3, F5, F2	O	OV_{DD}	6
MDVAL	F4	O	OV_{DD}	6
Clock				
SYSCLK	AH21	I	OV_{DD}	
RTC	AB23	I	OV_{DD}	
CLK_OUT	AF22	O	OV_{DD}	11
JTAG				
TCK	AF21	I	OV_{DD}	
TDI	AG21	I	OV_{DD}	12
TDO	AF19	O	OV_{DD}	11
TMS	AF23	I	OV_{DD}	12
$\overline{\text{TRST}}$	AG23	I	OV_{DD}	12
DFT				
$\overline{\text{LSSD\_MODE}}$	AG19	I	OV_{DD}	21
L1_TSTCLK	AB22	I	OV_{DD}	21
L2_TSTCLK	AG22	I	OV_{DD}	21
TEST_SEL	AH20	I	OV_{DD}	3
Thermal Management				
THERM0	AG2	I	—	14
THERM1	AH3	I	—	14

Conductivity	Value	Unit
Lid (12 × 14 × 1 mm)		
k_x	360	W/(m × K)
k_y	360	
k_z	360	
Lid Adhesive—Collapsed resistance (10 × 12 × 0.050 mm)		
k_x	1	
k_y	1	
k_z	1	
Die (10 × 12 × 0.76 mm)		
Bump/Underfill—Collapsed resistance (10 × 12 × 0.070 mm)		
k_x	0.6	
k_y	0.6	
k_z	1.9	
Substrate and Solder Balls (29 × 29 × 1.47 mm)		
k_x	10.2	
k_y	10.2	
k_z	1.6	

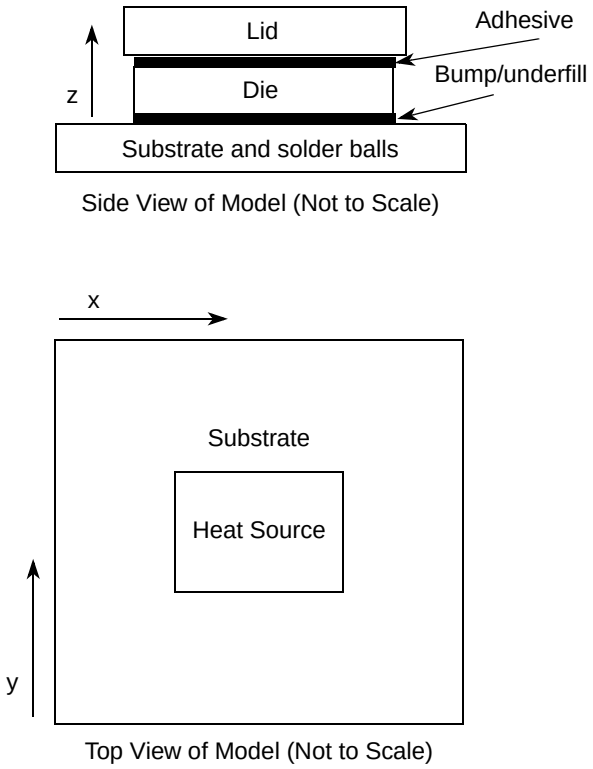

Figure 46. MPC8540 Thermal Model

16.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in Table 59, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

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16.2.4 Heat Sink Selection Examples

The following section provides a heat sink selection example using one of the commercially available heat sinks.

16.2.4.1 Case 1

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_I + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

where

T_J is the die-junction temperature

T_I is the inlet cabinet ambient temperature

T_R is the air temperature rise within the computer cabinet

θ_{JC} is the junction-to-case thermal resistance

θ_{INT} is the adhesive or interface material thermal resistance

θ_{SA} is the heat sink base-to-ambient thermal resistance

P_D is the power dissipated by the device

During operation the die-junction temperatures (T_J) should be maintained within the range specified in Table 2. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_A) may range from 30° to 40°C. The air temperature rise within a cabinet (T_R) may be in the range of 5° to 10°C. The thermal resistance of some thermal interface material (θ_{INT}) may be about 1°C/W. Assuming a T_I of 30 C, a T_R of 5 C, a FC-PBGA package θ_{JC} = 0.8, and a power consumption (P_D) of 7.0 W, the following expression for T_J is obtained:

$$\text{Die-junction temperature: } T_J = 30°C + 5°C + (0.8°C/W + 1.0°C/W + \theta_{SA}) \times 7.0\ W$$

The heat sink-to-ambient thermal resistance (θ_{SA}) versus airflow velocity for a Thermalloy heat sink #2328B is shown in Figure 49.

Assuming an air velocity of 2 m/s, we have an effective θ_{SA+} of about 3.3 C/W, thus

$$T_J = 30\ C + 5\ C + (0.8\ C/W + 1.0\ C/W + 3.3\ C/W) \times 7.0\ W,$$

resulting in a die-junction temperature of approximately 71 C which is well within the maximum operating temperature of the component.

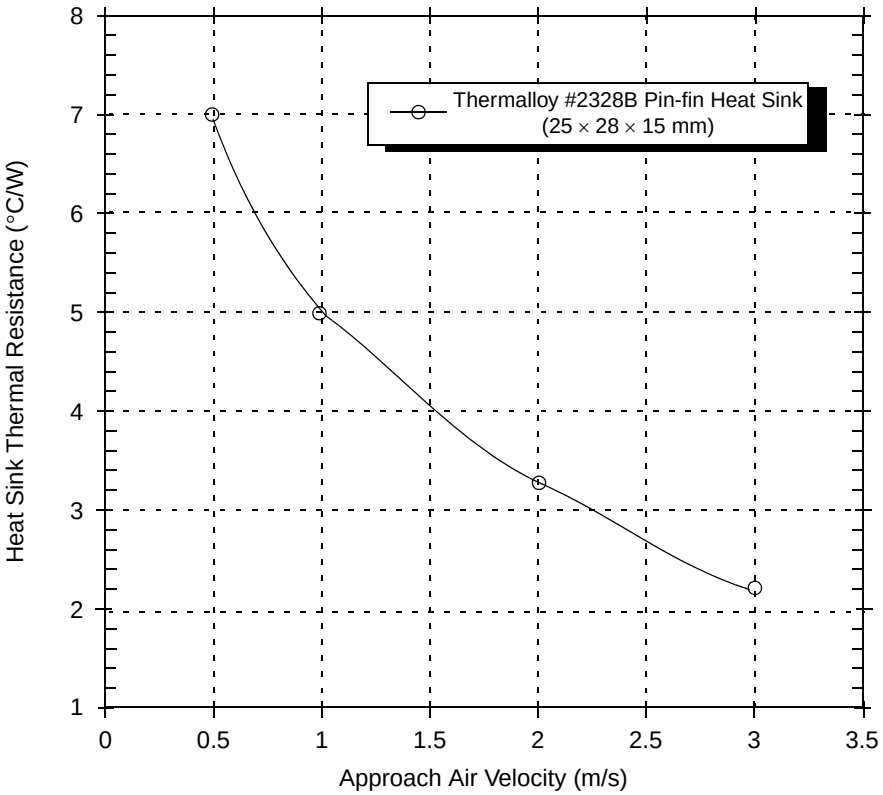

Figure 49. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

16.2.4.2 Case 2

Every system application has different conditions that the thermal management solution must solve. As an alternate example, assume that the air reaching the component is 85 C with an approach velocity of 1 m/sec. For a maximum junction temperature of 105 C at 7 W, the total thermal resistance of junction to case thermal resistance plus thermal interface material plus heat sink thermal resistance must be less than 2.8 C/W. The value of the junction to case thermal resistance in Table 59 includes the thermal interface resistance of a thin layer of thermal grease as documented in footnote 4 of the table. Assuming that the heat sink is flat enough to allow a thin layer of grease or phase change material, then the heat sink must be less than 2 C/W.

Millennium Electronics (MEI) has tooled a heat sink MTHERM-1051 for this requirement assuming a compactPCI environment at 1 m/sec and a heat sink height of 12 mm. The MEI solution is illustrated in Figure 50 and Figure 51. This design has several significant advantages:

- The heat sink is clipped to a plastic frame attached to the application board with screws or plastic inserts at the corners away from the primary signal routing areas.
- The heat sink clip is designed to apply the force holding the heat sink in place directly above the die at a maximum force of less than 10 lbs.
- For applications with significant vibration requirements, silicone damping material can be applied between the heat sink and plastic frame.

17.6 Configuration Pin Muxing

The MPC8540 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While HRESET is asserted however, these pins are treated as inputs. The value presented on these pins while HRESET is asserted, is latched when HRESET deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during HRESET (and for platform/system clocks after HRESET deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

17.7 Pull-Up Resistor Requirements

The MPC8540 requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including EPIC interrupt pins. I^2C open drain type pins should be pulled up with ~1 kΩ resistors.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 55. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

TSEC1_TXD[3:0] must not be pulled low during reset. Some PHY chips have internal pulldowns that could cause this to happen. If such PHY chips are used, then a pullup must be placed on these signals strong enough to restore these signals to a logical 1 during reset.

Three test pins also require pull-up resistors (100 Ω - 1 kΩ). These pins are L1_TSTCLK, L2_TSTCLK, and LSSD_MODE. These signals are for factory use only and must be pulled up to OVDD for normal machine operation.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

Table 61. Document Revision History (continued)

Rev. No.	Substantive Change(s)
3.2	Updated Table 1 and Table 2 with 1.0 GHz device parameter requirements. Added Section 2.1.2, “Power Sequencing”. Updated Table 4 with Maximum power data. Updated Table 4 and Table 5 with 1 GHz speed grade information. Updated Table 6 with corrected typical I/O power numbers. Updated Table 7 Note 2 lower voltage measurement point. Replaced Table 7 Note 5 with spread spectrum clocking guidelines. Added to Table 8 rise and fall time information. Added Section 4.4, “Real Time Clock Timing”. Added precharge information to Section 6.2.2, “DDR SDRAM Output AC Timing Specifications”. Updated Table 20 minimum and maximum baud rates. Removed V_{IL} and V_{IH} references from Table 23, Table 24, Table 25, and Table 26. Added reference level note to Table 23, Table 24, Table 25, Table 26, Table 27, Table 28, and Table 29. Updated TXD references to TCG in Section 8.2.3.1, “TBI Transmit AC Timing Specifications”. Updated PMA_RX_CLK references to RX_CLK in Section 8.2.3.2, “TBI Receive AC Timing Specifications”. Updated t_{TTKHDX} value in Table 27. Updated RXD references to RCG in Section 8.2.3.2, “TBI Receive AC Timing Specifications”. Updated Table 29 Note 2. Removed V_{IL} and V_{IH} references from Table 31, and Table 32. Added reference level note to Table 31, and Table 32. Corrected Figure 15 and Figure 16. Corrected Table 34 f_{MDC} and t_{MDC} to reflect the correct minimum operating frequency. Updated Table 34 t_{MDKHDV} and t_{MDKHDX} values for clarification. Added t_{LBKHKT} and updated Note 2 in Table 37. Corrected $\overline{\text{LGTA}}$ timing references in Figure 19. Updated Figure 20, Figure 22, and Figure 24. Updated Figure 44. Clarified Table 53 Note 5. Updated Table 54 and Table 55 with 1 GHz information. Added heat sink removal discussion to Section 16.2.3, “Thermal Interface Materials”. Corrected and added 1 GHz part number to Table 62.
3.1	Updated Table 4 and Table 5. Added Table 6. Added MCK duty cycle to Table 16. Updated f_{MDC}, t_{MDC}, t_{MDKHDV}, and t_{MDKHDX} parameters in Table 34. Added LALE to $t_{LBKHOV3}$ parameter in Table 36 and Table 37, and updated Figure 19 and Figure 20. Corrected active level designations of some of the pins in Table 53. Updated Table 62.

Table 61. Document Revision History (continued)

Rev. No.	Substantive Change(s)
2.0	Section 1.1—Updated features list to coincide with latest version of the reference manual Table 1 and Table 2—Addition of SYSCLK to OV_{IN} Table 2—Addition of notes 1 and 2 Table 3—Addition of note 1 Table 5—New Section 4—New Table 13—Addition of I_{VREF} Removed Figure 4 DDR SRAM Input TIming Diagram Table 15—Modified maximum values for t_{DISKEW} Table 16—Added MSYNC_OUT to tMCKSKEW2 Figure 5—New Section 6.2.1—Removed Figure 4, “DDR SDRAM Input Timing Diagram” Section 8.1—Removed references to 2.5 V from first paragraph Figure 8—New Table 21 and Table 22—Modified “conditions” for I_{IH} and I_{IL} Table 23—Addition of min and max for GTX_CLK125 reference clock duty cycle Table 27 —Addition of min and max for GTX_CLK125 reference clock duty cycle Table 29—Addition of min and max for GTX_CLK125 reference clock duty cycle Table 30—VOH min and conditions; I_{IH} and I_{IL} conditions Table 31—Min and max for t_{MTXR} and t_{MTXF} Table 32—Min and max for t_{MRXR} and t_{MRXF} Figure 23 and Figure 24—Changed LSYNC_IN to Internal clock at top of each figure Figure 18—New Figure 18—New Table 36—Removed row for tLBKHOX3 Table 43—New (AC timing of PCI-X at 66 MHz) Table 53—Addition of note 19 Figure 55—Addition of jumper and note at top of diagram Table 55: Changed max bus freq for 667 core to 166 Section 16.2.1—Modified first paragraph Figure 46—Modified Figure 47—New Table 59—Modified thermal resistance data Section 16.2.4.2—Modified first and second paragraphs