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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	833MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1), 10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8540vt833lb

  - Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
  - Sleep mode support for self refresh SDRAM
  - Supports auto refreshing
  - On-the-fly power management using CKE signal
  - Registered DIMM support
  - Fast memory access via JTAG port
  - 2.5-V SSTL2 compatible I/O
- RapidIO interface unit
  - 8-bit RapidIO I/O and messaging protocols
  - Source-synchronous double data rate (DDR) interfaces
  - Supports small type systems (small domain, 8-bit device ID)
  - Supports four priority levels (ordering within a level)
  - Reordering across priority levels
  - Maximum data payload of 256 bytes per packet
  - Packet pacing support at the physical layer
  - CRC protection for packets
  - Supports atomic operations increment, decrement, set, and clear
  - LVDS signaling
- RapidIO–compliant message unit
  - One inbound data message structure (inbox)
  - One outbound data message structure (outbox)
  - Supports chaining and direct modes in the outbox
  - Support of up to 16 packets per message
  - Support of up to 256 bytes per packet and up to 4 Kbytes of data per message
  - Supports one inbound doorbell message structure
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts with 32-bit messages
  - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
  - Four global high resolution timers/counters that can generate interrupts
  - Supports 22 other internal interrupt sources
  - Supports fully nested interrupt delivery
  - Interrupts can be routed to external pin for external processing

  - Interrupts can be routed to the e500 core's standard or critical interrupt inputs
  - Interrupt summary registers allow fast identification of interrupt source
- I^2C controller
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the I^2C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I^2C addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
  - Programming model compatible with the original 16450 UART and the PC16550D
- 10/100 fast Ethernet controller (FEC)
  - Operates at 10 to 100 megabits per second (Mbps) as a device debug and maintenance port
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 166 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
  - Three protocol engines available on a per chip select basis:
    - General purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-,16-, or 32-bit)
- Two three-speed (10/100/1Gb) Ethernet controllers (TSECs)
  - Dual IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab compliant controllers
  - Support for different Ethernet physical interfaces:
    - 10/100/1Gb Mbps IEEE 802.3 GMII
    - 10/100 Mbps IEEE 802.3 MII
    - 10 Mbps IEEE 802.3 MII
    - 1000 Mbps IEEE 802.3z TBI
    - 10/100/1Gb Mbps RGMII/RTBI
  - Full- and half-duplex support

2.1.2 Power Sequencing

The MPC8540 requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD}, AV_{DD}
2. GV_{DD}, LV_{DD}, OV_{DD} (I/O supplies)

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90 percent of their value before the voltage rails on the current step reach 10 percent of theirs.

NOTE

If the items on line 2 must precede items on line 1, please ensure that the delay will not exceed 500 ms and the power sequence is not done greater than once per day in production environment.

NOTE

From a system standpoint, if the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os on the MPC8540 may drive a logic one or zero during power-up.

2.1.3 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8540. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

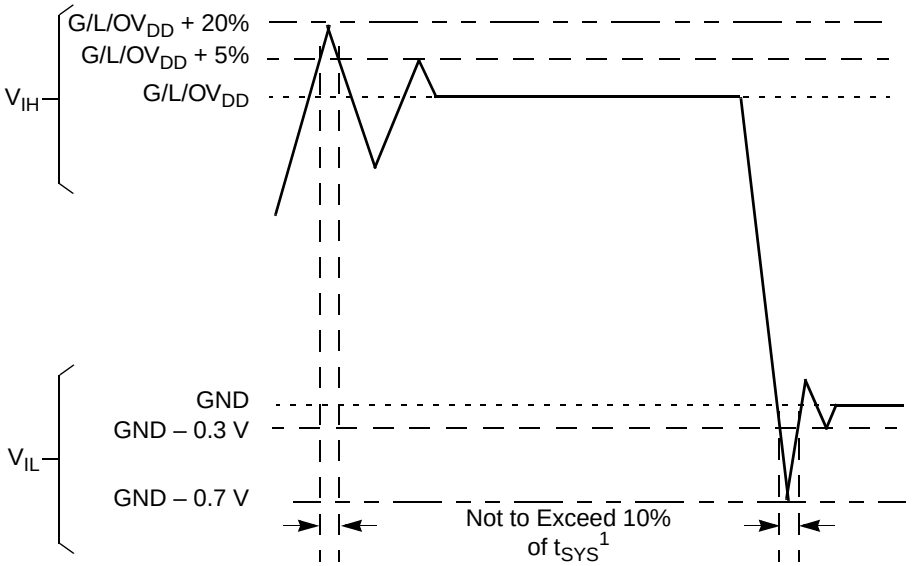
Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit
Core supply voltage For devices rated at 667 and 833 MHz For devices rated at 1 GHz	V_{DD}	 1.2 V ± 60 mV 1.3 V ± 50 mV	V
PLL supply voltage For devices rated at 667 and 833 MHz For devices rated at 1 GHz	AV_{DD}	 1.2 V ± 60 mV 1.3 V ± 50 mV	V
DDR DRAM I/O voltage	GV_{DD}	2.5 V ± 125 mV	V
Three-speed Ethernet I/O voltage	LV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V
PCI/PCI-X, local bus, RapidIO, 10/100 Ethernet, MII management, DUART, system control and power management, I^2C, and JTAG I/O voltage	OV_{DD}	3.3 V ± 165 mV	V

Table 2. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit
Input voltage	DDR DRAM signals	MV_{IN}	GND to GV_{DD}	V
	DDR DRAM reference	MV_{REF}	GND to $GV_{DD/2}$	V
	Three-speed Ethernet signals	LV_{IN}	GND to LV_{DD}	V
	PCI/PCI-X, local bus, RapidIO, 10/100 Ethernet, MII management, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V
Die-junction temperature		T_j	0 to 105	•C

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8540.



Note:
t_{SYS} refers to the clock period associated with the SYSCLK signal.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

The MPC8540 core voltage must always be provided at nominal 1.2 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

Table 11. RESET Initialization Timing Specifications (continued)

Parameter/Condition	Min	Max	Unit	Notes
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Notes:
1.SYSCLK is identical to the PCI_CLK signal and is the primary clock input for the MPC8540. See the MPC8540 Integrated Processor Preliminary Reference Manual for more details.

Table 12 provides the PLL and DLL lock times.

Table 12. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	
DLL lock times	7680	122,880	CCB Clocks	1, 2

Notes:
1.DLL lock times are a function of the ratio between the output clock and the platform (or CCB) clock. A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The CCB clock is determined by the SYSCLK × platform PLL ratio.

6 DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8540.

6.1 DDR SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8540.

Table 13. DDR SDRAM DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	4
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.18$	V	4
Output leakage current	I_{OZ}	–10	10	μA	5
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–15.2	—	mA	
Output low current (V_{OUT} = 0.35 V)	I_{OL}	15.2	—	mA	

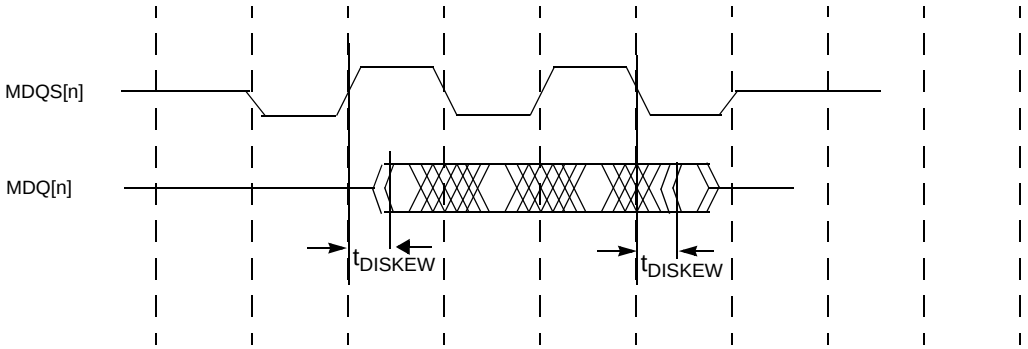


Figure 4. DDR SDRAM Interface Input Timing

6.2.2 DDR SDRAM Output AC Timing Specifications

For chip selects $\overline{\text{MCS1}}$ and $\overline{\text{MCS2}}$, there will always be at least 200 DDR memory clocks coming out of self-refresh after an $\overline{\text{HRESET}}$ before a precharge occurs. This will not necessarily be the case for chip selects $\overline{\text{MCS0}}$ and $\overline{\text{MCS3}}$.

6.2.2.1 DLL Enabled Mode

Table 16 and Table 17 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface with the DDR DLL enabled.

Table 16. DDR SDRAM Output AC Timing Specifications–DLL Mode

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing)	t_{MCK}	6	10	ns	2
On chip Clock Skew	$t_{MCKSKEW}$	—	150	ps	3, 8
MCK[n] duty cycle	t_{MCKH}/t_{MCK}	45	55	%	8
ADDR/CMD output valid	t_{DDKHOV}	—	3	ns	4, 9
ADDR/CMD output invalid	t_{DDKHOX}	1	—	ns	4, 9
Write CMD to first MDQS capture edge	t_{DDSHMH}	t_{MCK} + 1.5	t_{MCK} + 4.0	ns	5
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 900 1100 1200	—	ps	6, 9
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 900 1100 1200	—	ps	6, 9
MDQS preamble start	t_{DDSHMP}	0.75 × t_{MCK} + 1.5	0.75 × t_{MCK} + 4.0	ns	7, 8

8.2.4 RGMII and RTBI AC Timing Specifications

Table 29 presents the RGMII and RTBI AC timing specifications.

Table 29. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT} [5]	–500	0	500	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns
Clock period[3]	t_{RGT} [6]	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4]	t_{RGTH}/t_{RGT} [6]	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3]	t_{RGTH}/t_{RGT} [6]	40	50	60	%
Rise and fall time	t_{RGTR}, t_{RGTF} [6,7]	—	—	0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. The RGMII specification requires that PC board designer add 1.5 ns or greater in trace delay to the RX_CLK in order to meet this specification. However, as stated above, this device will function with only 1.0 ns of delay.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by characterization.
6. Guaranteed by design.
7. Signal timings are measured at 0.5 V and 2.0 V voltage levels.

Figure 15 shows the MII transmit AC timing diagram.

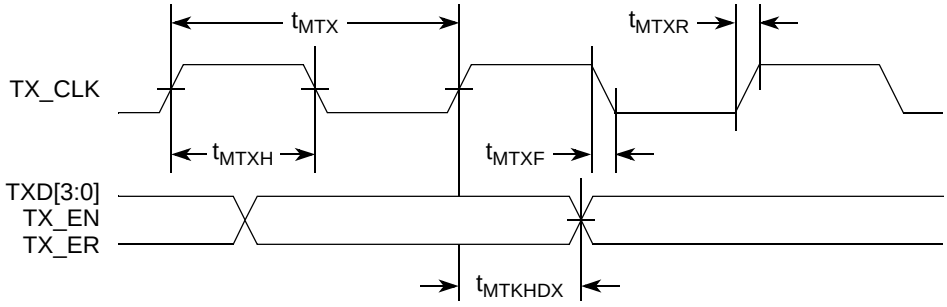


Figure 15. MII Transmit AC Timing Diagram

8.3.2.2 MII Receive AC Timing Specifications

Table 32 provides the MII receive AC timing specifications.

Table 32. MII Receive AC Timing Specifications

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[7:0], TX_DV, TX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[7:0], TX_DV, TX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise and fall time	t_{MRXR}, t_{MRXF} [2,3]	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKH} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the high (H) state or hold time. Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

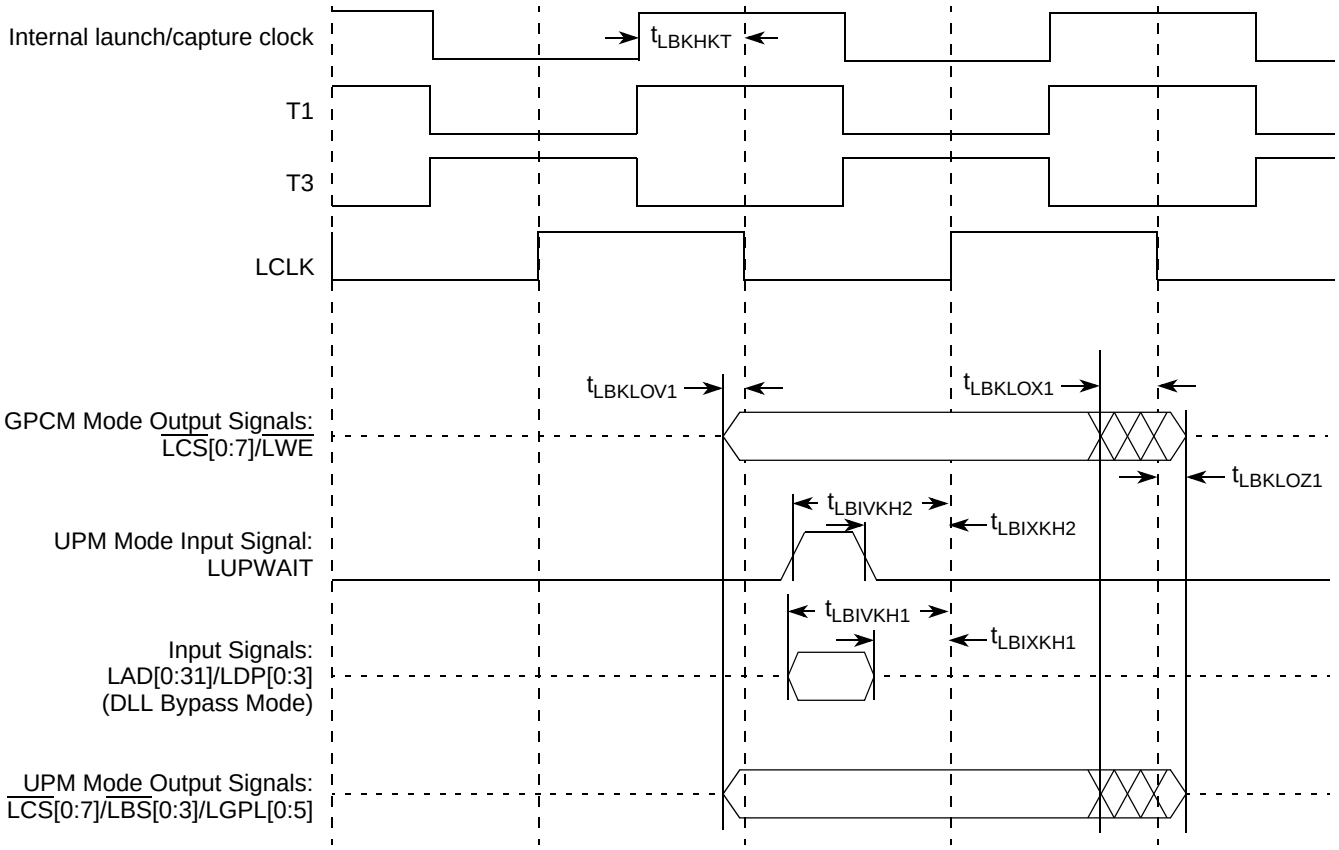


Figure 22. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

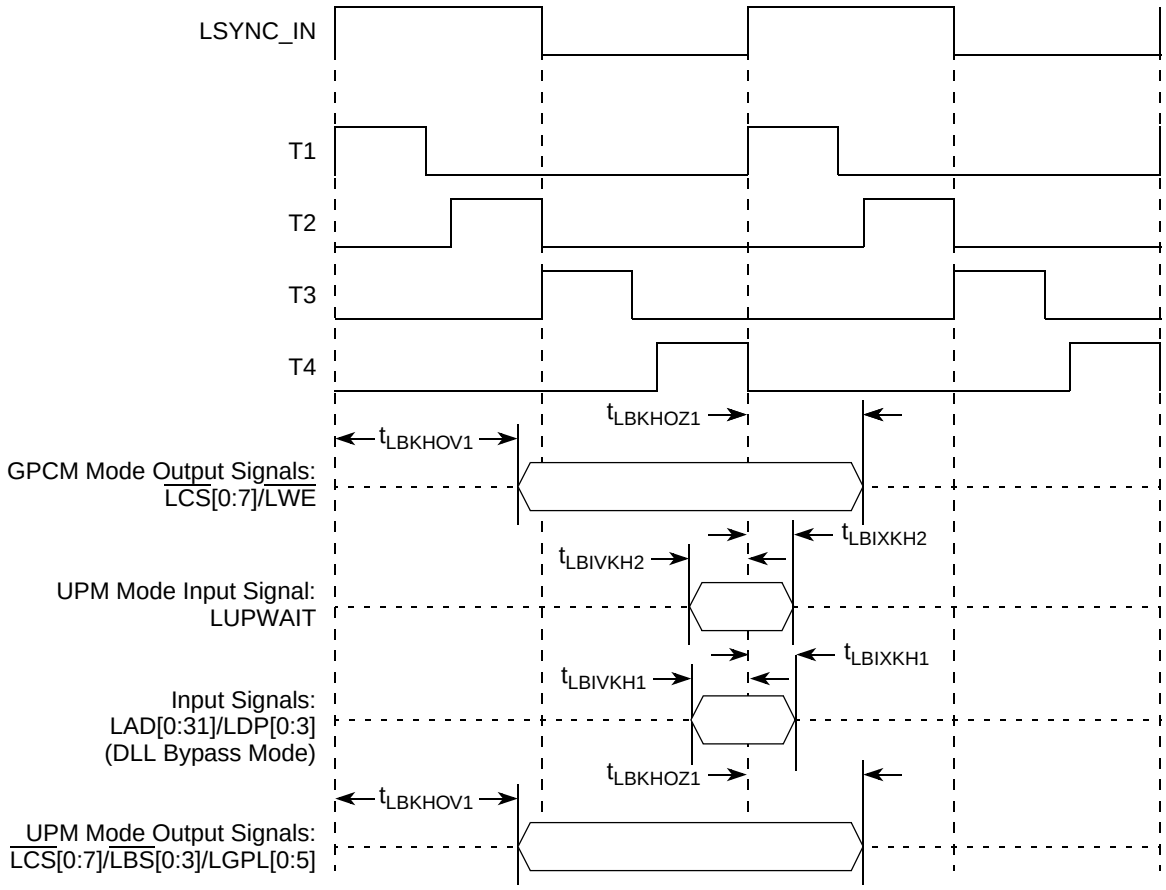


Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Enabled)

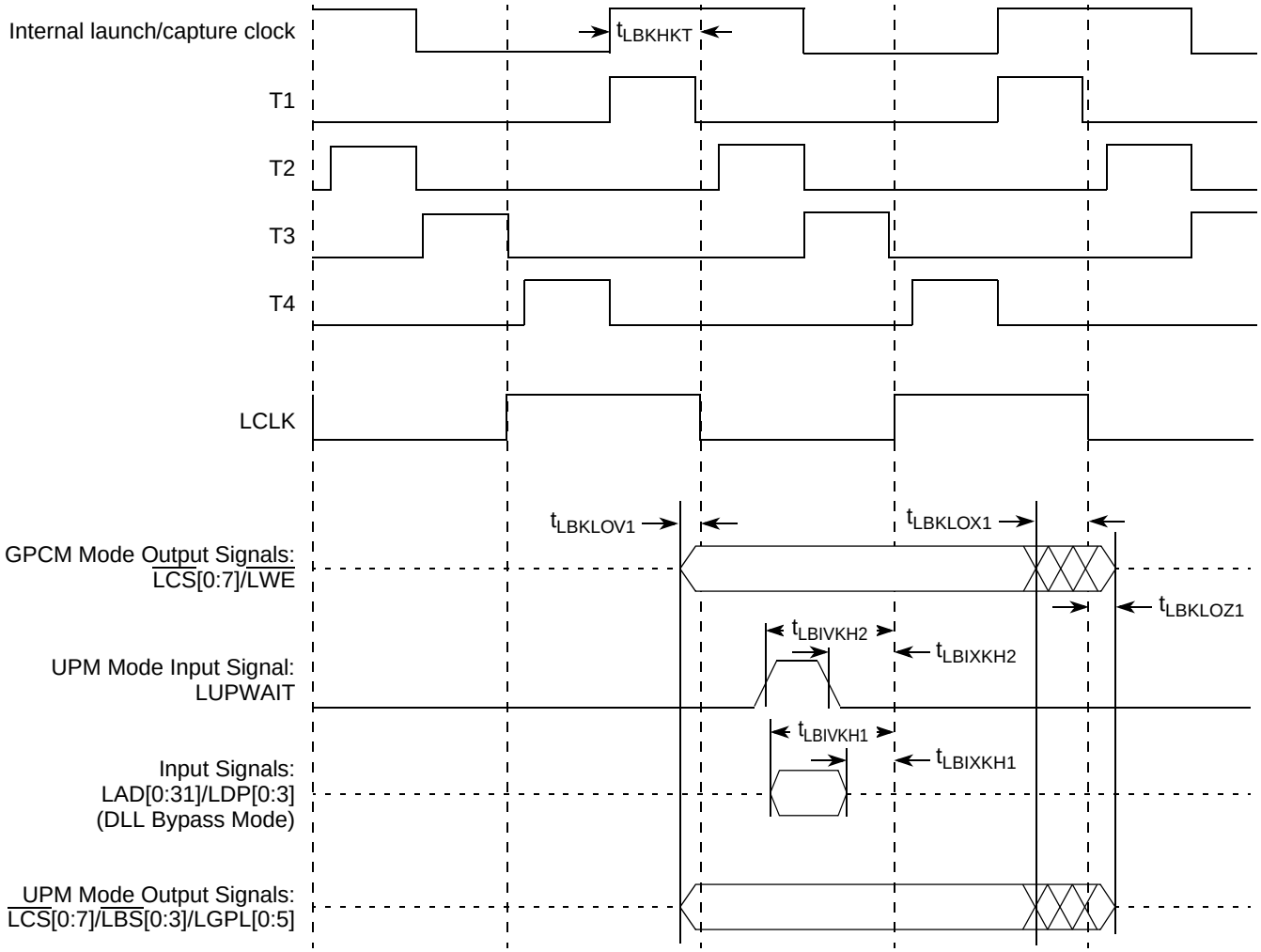


Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Bypass Mode)

- The peak differential signal of the transmitter output or receiver input, is A – B volts.
- The peak-to-peak differential signal of the transmitter output or receiver input, is 2 × (A – B) volts.

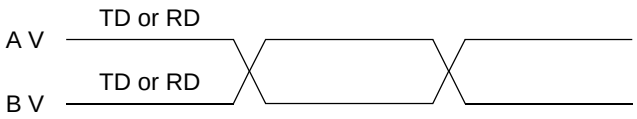


Figure 36. Differential Peak-to-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using numerical values, consider the case where a LVDS transmitter has a common mode voltage of 1.2 V and each signal has a swing that goes between 1.4 and 1.0 V. Using these values, the peak-to-peak voltage swing of the signals TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ is 400 mV. The differential signal ranges between 400 and –400 mV. The peak differential signal is 400 mV, and the peak-to-peak differential signal is 800 mV.

A timing edge is the zero-crossing of a differential signal. Each skew timing parameter on a parallel bus is synchronously measured on two signals relative to each other in the same cycle, such as data to data, data to clock, or clock to clock. A skew timing parameter may be relative to the edge of a signal or to the middle of two sequential edges.

Static skew represents the timing difference between signals that does not vary over time regardless of system activity or data pattern. Path length differences are a primary source of static skew.

Dynamic skew represents the amount of timing difference between signals that is dependent on the activity of other signals and varies over time. Crosstalk between signals is a source of dynamic skew.

Eye diagrams and compliance masks are a useful way to visualize and specify driver and receiver performance. This technique is used in several serial bus specifications. An example compliance mask is shown in Figure 37. The key difference in the application of this technique for a parallel bus is that the data is source synchronous to its bus clock while serial data is referenced to its embedded clock. Eye diagrams reveal the quality (cleanness, openness, goodness) of a driver output or receiver input. An advantage of using an eye diagram and a compliance mask is that it allows specifying the quality of a signal without requiring separate specifications for effects such as rise time, duty cycle distortion, data dependent dynamic skew, random dynamic skew, etc. This allows the individual semiconductor manufacturer maximum flexibility to trade off various performance criteria while keeping the system performance constant.

In using the eye pattern and compliance mask approach, the quality of the signal is specified by the compliance mask. The mask specifies the maximum permissible magnitude of the signal and the minimum permissible eye opening. The eye diagram for the signal under test is generated according to the specification. Compliance is determined by whether the compliance mask can be positioned over the eye diagram such that the eye pattern falls entirely within the unshaded portion of the mask.

Serial specifications have clock encoded with the data, but the LP-LVDS physical layer defined by RapidIO is a source synchronous parallel port so additional specifications to include effects that are not found in serial links are required. Specifications for the effect of bit to bit timing differences caused by static skew have been added and the eye diagrams specified are measured relative to the associated clock in order to include clock to data effects. With the transmit output (or receiver input) eye diagram, the user can determine if the transmitter output (or receiver input) is compliant with an oscilloscope with the appropriate software.

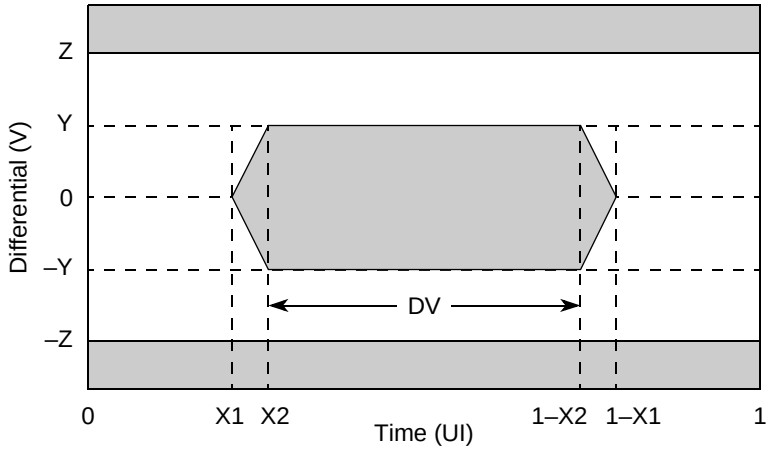


Figure 37. Example Compliance Mask

Y = minimum data valid amplitude

Z = maximum amplitude

1 UI = 1 unit interval = 1/baud rate

X1 = end of zero crossing region

X2 = beginning of data valid window

DV = data valid window = 1 – 2 × X2

The waveform of the signal under test must fall within the unshaded area of the mask to be compliant. Different masks are used for the driver output and the receiver input allowing each to be separately specified.

13.3.1 RapidIO Driver AC Timing Specifications

Driver AC timing specifications are provided in Table 47, Table 48, and Table 49. A driver shall comply with the specifications for each data rate/frequency for which operation of the driver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The output of a driver shall be connected to a 100 Ω, ±1%, differential (bridged) resistive load.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7]).

Table 47. RapidIO Driver AC Timing Specifications—500 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential output high voltage	V_{OHD}	200	540	mV	1
Differential output low voltage	V_{OLD}	–540	–200	mV	1

Table 47. RapidIO Driver AC Timing Specifications—500 Mbps Data Rate (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle	DC	48	52	%	2, 6
V_{OD} rise time, 20%–80% of peak-to-peak differential signal swing	t_{FALL}	200	—	ps	3, 6
V_{OD} fall time, 20%–80% of peak-to-peak differential signal swing	t_{RISE}	200	—	ps	6
Data valid	DV	1260	—	ps	
Skew of any two data outputs	t_{DPAIR}	—	180	ps	4, 6
Skew of single data outputs to associated clock	$t_{SKEW,PAIR}$	–180	180	ps	5, 6

Notes:

1.See Figure 38.

2.Requires ±100 ppm long term frequency stability.

3.Measured at V_{OD} = 0 V.

4.Measured using the RapidIO transmit mask shown in Figure 38.

5.See Figure 43.

6.Guaranteed by design.

Table 48. RapidIO Driver AC Timing Specifications—750 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential output high voltage	V_{OHD}	200	540	mV	1
Differential output low voltage	V_{OLD}	–540	–200	mV	1
Duty cycle	DC	48	52	%	2, 6
V_{OD} rise time, 20%–80% of peak-to-peak differential signal swing	t_{FALL}	133	—	ps	3, 6
V_{OD} fall time, 20%–80% of peak-to-peak differential signal swing	t_{RISE}	133	—	ps	6
Data valid	DV	800	—	ps	6
Skew of any two data outputs	t_{DPAIR}	—	133	ps	4, 6
Skew of single data outputs to associated clock	$t_{SKEW,PAIR}$	–133	133	ps	5, 6

Notes:

1.See Figure 38.

2.Requires ±100 ppm long term frequency stability.

3.Measured at V_{OD} = 0 V.

4.Measured using the RapidIO transmit mask shown in Figure 38.

5.See Figure 43.

6.Guaranteed by design.

enough that increasing the length of the sequence does not cause the resulting eye pattern to change from one that complies with the RapidIO receive mask to one that does not comply with the mask. The data carried by any given data signal in the interface may not be correlated with the data carried by any other data signal in the interface. The zero-crossings of the clock associated with a data signal shall be used as the timing reference for aligning the multiple recordings of the data signal when the recordings are overlaid.

While the method used to make the recordings and overlay them to form the eye pattern is not specified, the method used shall be demonstrably equivalent to the following method. The signal under test is repeatedly recorded with a digital oscilloscope in infinite persistence mode. Each recording is triggered by a zero-crossing of the clock associated with the data signal under test. Roughly half of the recordings are triggered by positive-going clock zero-crossings and roughly half are triggered by negative-going clock zero-crossings. Each recording is at least 1.9 UI in length (to ensure that at least one complete eye is formed) and begins 0.5 UI before the trigger point (0.5 UI before the associated clock zero-crossing). Depending on the length of the individual recordings used to generate the eye pattern, one or more complete eyes will be formed. Regardless of the number of eyes, the eye whose center is immediately to the right of the trigger point is the eye used for compliance testing.

An example of an eye pattern generated using the above method with recordings 3 UI in length is shown in Figure 41. In this example, there is no skew between the signal under test and the associated clock used to trigger the recordings. If skew was present, the eye pattern would be shifted to the left or right relative to the oscilloscope trigger point.

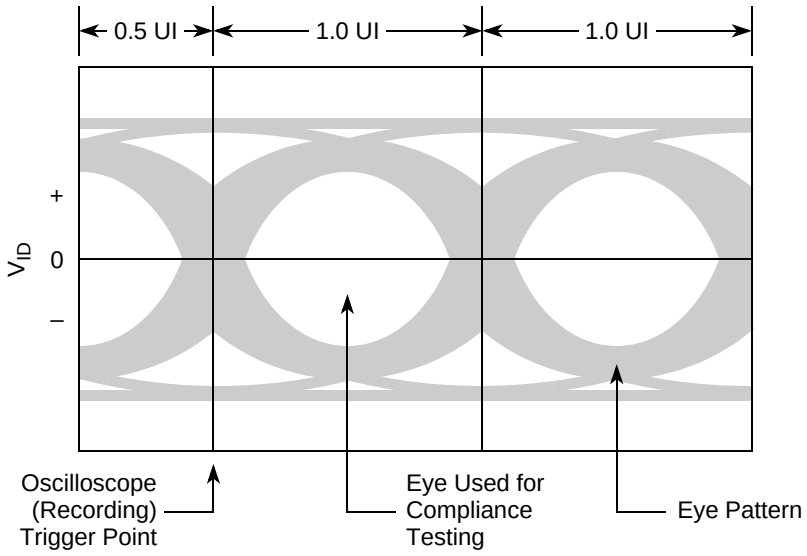


Figure 41. Example Receiver Input Eye Pattern

14.2 Mechanical Dimensions of the MPC8540 FC-PBGA

Figure 44 the mechanical dimensions and bottom surface nomenclature of the MPC8540, 783 FC-PBGA package.

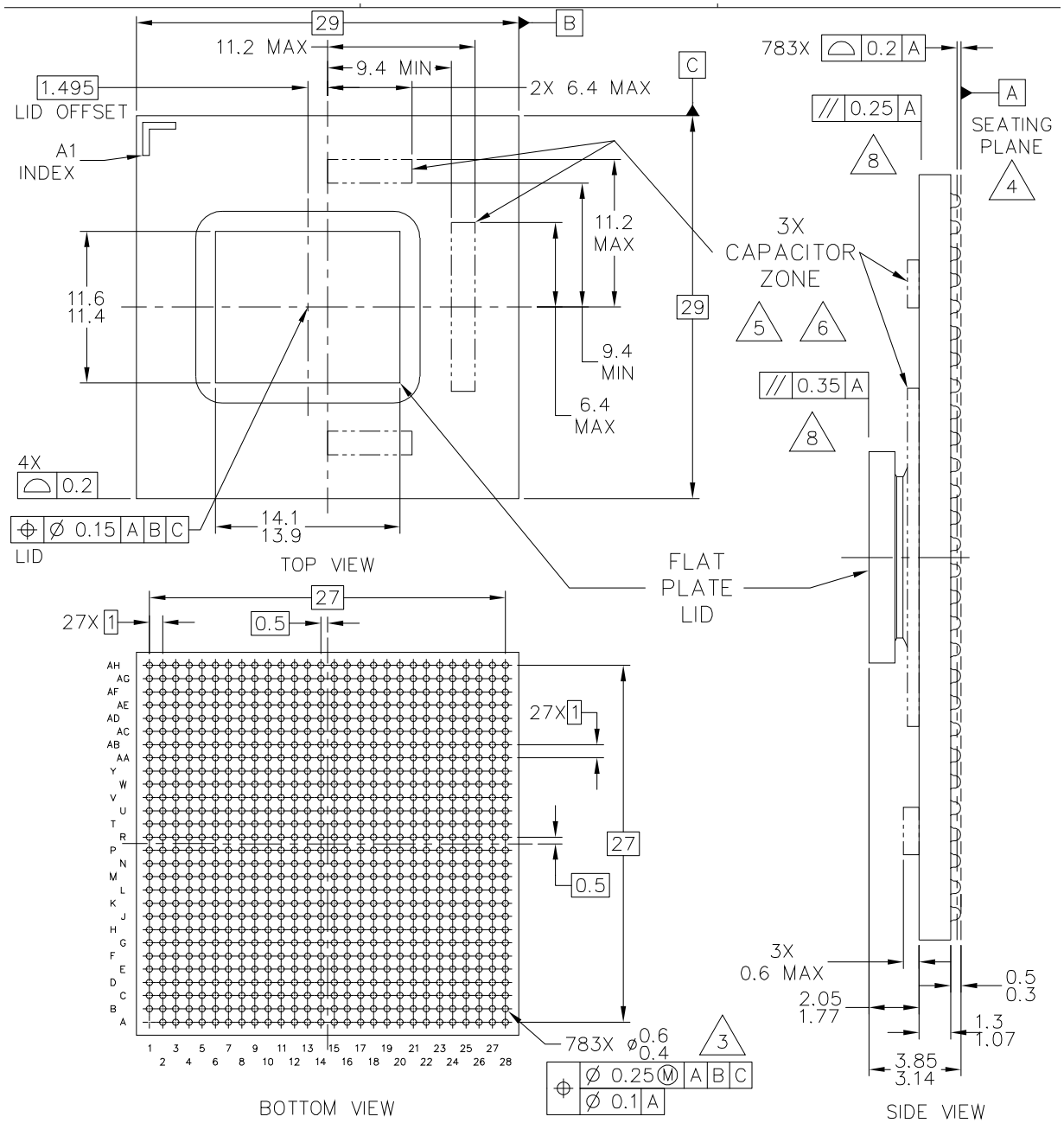
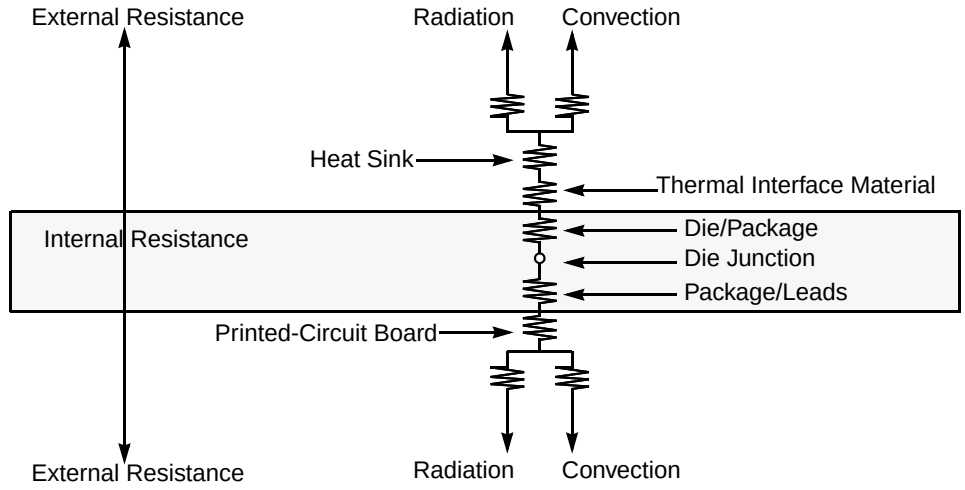


Figure 44. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8540 FC-PBGA

NOTES

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.

Figure 47 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 47. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

16.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 48 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 45). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink, the heat sink should be slowly removed. Heating the heat sink to 40-50•C with an air gun can soften the interface material and make the removal easier. The use of an adhesive for heat sink attach is not recommended.

17 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8540.

17.1 System Clocking

The MPC8540includes two PLLs.

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 15.2, “Platform/System PLL Ratio.”
2. The e500 Core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 15.3, “e500 Core PLL Ratio.”

17.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}1$ and $AV_{DD}2$, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide three independent filter circuits as illustrated in Figure 52, one to each of the three AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias.

Figure 52 shows the PLL power supply filter circuit.

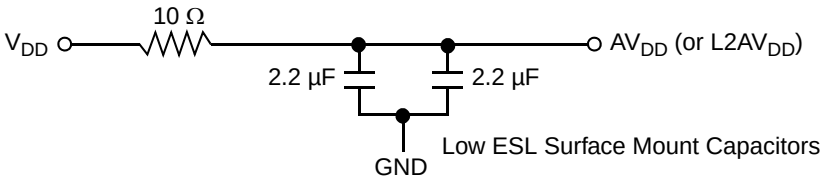


Figure 52. PLL Power Supply Filter Circuit

17.6 Configuration Pin Muxing

The MPC8540 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While HRESET is asserted however, these pins are treated as inputs. The value presented on these pins while HRESET is asserted, is latched when HRESET deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during HRESET (and for platform/system clocks after HRESET deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

17.7 Pull-Up Resistor Requirements

The MPC8540 requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including EPIC interrupt pins. I^2C open drain type pins should be pulled up with ~1 kΩ resistors.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 55. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

TSEC1_TXD[3:0] must not be pulled low during reset. Some PHY chips have internal pulldowns that could cause this to happen. If such PHY chips are used, then a pullup must be placed on these signals strong enough to restore these signals to a logical 1 during reset.

Three test pins also require pull-up resistors (100 Ω - 1 kΩ). These pins are L1_TSTCLK, L2_TSTCLK, and LSSD_MODE. These signals are for factory use only and must be pulled up to OVDD for normal machine operation.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

19 Device Nomenclature

Ordering information for the parts fully covered by this specification document is provided in Section 19.1, "Nomenclature of Parts Fully Addressed by this Document."

19.1 Nomenclature of Parts Fully Addressed by this Document

Table 62 provides the Freescale part numbering nomenclature for the MPC8540. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 62. Part Numbering Nomenclature

MPC	nnnn	*t*	pp	ff(f)	c	r
Product Code	**Part Identifier**	**Temperature Range[1]**	**Package [2]**	**Processor Frequency [3, 4]**	**Platform Frequency**	**Revision Level**
MPC	8540	Blank = 0 to 105°C C = –40 to 105°C	PX = FC-PBGA VT = FC-PBGA (Pb-free)	833 = 833 MHz 667 = 667 MHz	L = 333 MHz J = 266 MHz	B = Rev. 2.0 (SVR = 0x80300020) C = Rev. 2.1 (SVR = 0x80300021)
MPC	8540	Blank = 0 to 105°C C = –40 to 105°C	PX = FC-PBGA VT = FC-PBGA (Pb-free)	AQ = 1.0 GHz	F = 333 MHz	B = Rev. 2.0 (SVR = 0x80300020) C = Rev. 2.1 (SVR = 0x80300021)

Notes:

1. For Temperature Range=C, Processor Frequency is limited to 667 MHz.
2. See Section 14, "Package and Pin Listings," for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. The core must be clocked at a minimum frequency of 400MHz. A device must not be used beyond the core frequency or platform frequency indicated on the device.
4. Designers should use the maximum power value corresponding to the core and platform frequency grades indicated on the device. A lower maximum power value should not be assumed for design purposes even when running at a lower frequency.