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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1), 10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8540cpx667jb

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings [1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage For devices rated at 667 and 833 MHz For devices rated at 1 GHz		V_{DD}	 –0.3 to 1.32 –0.3 to 1.43	V	
PLL supply voltage For devices rated at 667 and 833 MHz For devices rated at 1 GHz		AV_{DD}	 –0.3 to 1.32 –0.3 to 1.43	V	
DDR DRAM I/O voltage		GV_{DD}	–0.3 to 3.63	V	
Three-speed Ethernet I/O voltage		LV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	
PCI/PCI-X, local bus, RapidIO, 10/100 Ethernet, MII management, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	3
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	4, 5
	Local bus, RapidIO, 10/100 Ethernet, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	5
	PCI/PCI-X	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	–55 to 150	•C	

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

Table 6 provides estimated I/O power numbers for each block: DDR, PCI, Local Bus, RapidIO, TSEC, and FEC.

Table 6. Estimated Typical I/O Power Consumption

Interface	Parameter	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Units	Notes
DDR I/O	CCB = 200 MHz	0.46				W	1
	CCB = 266 MHz	0.59					
	CCB = 300 MHz	0.66					
	CCB = 333 MHz	0.73					
PCI/PCI-X I/O	32-bit, 33 MHz		0.04			W	2
	32-bit 66 MHz		0.07				
	64-bit, 66 MHz		0.14				
	64-bit, 133 MHz		0.25				
Local Bus I/O	32-bit, 33 MHz		0.07			W	3
	32-bit, 66 MHz		0.13				
	32-bit, 133 MHz		0.24				
	32-bit, 167 MHz		0.30				
RapidIO I/O	500 MHz data rate		0.96			W	4
TSEC I/O	MII			10		mW	5, 6
	GMII, TBI (2.5 V)				40		
	GMII, TBI (3.3 V)			70			
	RGMII, RTBI				40		
FEC I/O	MII		10			mW	7

Notes:

1. GV_{DD}=2.5, ECC enabled, 66% bus utilization, 33% write cycles, 10pF load on data, 10pF load on address/command, 10pF load on clock
2. OV_{DD}=3.3, 30pF load per pin, 54% bus utilization, 33% write cycles
3. OV_{DD}=3.3, 25pF load per pin, 5pF load on clock, 40% bus utilization, 33% write cycles
4. V_{DD}=1.2, OV_{DD}=3.3
5. LVDD=2.5/3.3, 15pF load per pin, 25% bus utilization
6. Power dissipation for one TSEC only
7. OV_{DD}=3.3, 20pF load per pin, 25% bus utilization

8.4.2 MII Management AC Electrical Specifications

Table 34 provides the MII management AC timing specifications.

Table 34. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	0.893	—	10.4	MHz	2, 4
MDC period	t_{MDC}	96	—	1120	ns	
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	
MDC to MDIO valid	t_{MDKHDV}			$2*[1/(f_{ccb\_clk}/8)]$	ns	3
MDC to MDIO delay	t_{MDKHDX}	10	—	$2*[1/(f_{ccb\_clk}/8)]$	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	
MDC rise time	t_{MDCR}	—	—	10	ns	4
MDC fall time	t_{MDHF}	—	—	10	ns	4

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the CCB clock speed (that is, for a CCB clock of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a CCB clock of 333 MHz, the maximum frequency is 10.4 MHz and the minimum frequency is 1.5 MHz).
3. This parameter is dependent on the CCB clock speed (that is, for a CCB clock of 267 MHz, the delay is 60 ns and for a CCB clock of 333 MHz, the delay is 48 ns).
4. Guaranteed by design.

Figure 17 shows the MII management AC timing diagram.

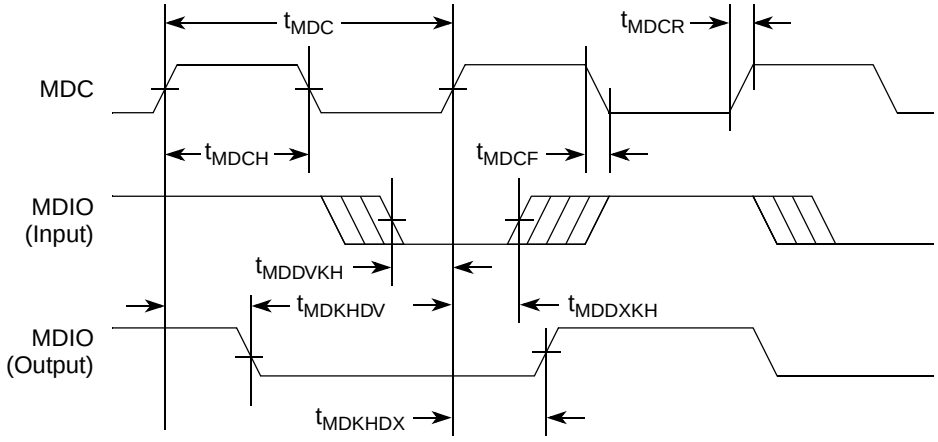


Figure 17. MII Management Interface Timing Diagram

Table 37 describes the general timing parameters of the local bus interface of the MPC8540 with the DLL bypassed.

Table 37. Local Bus General Timing Parameters—DLL Bypassed

Parameter	POR Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time		t_{LBK}	6.0	—	ns	2
Internal launch/capture clock to LCLK delay		t_{LBKHKT}	2.3	3.9	ns	8
LCLK[n] skew to LCLK[m] or LSYNC_OUT		$t_{LBKSKEW}$	—	150	ps	3, 9
Input setup to local bus clock (except LUPWAIT)		$t_{LBIVKH1}$	5.7	—	ns	4, 5
LUPWAIT input setup to local bus clock		$t_{LBIVKH2}$	5.6	—	ns	4, 5
Input hold from local bus clock (except LUPWAIT)		$t_{LBIXKH1}$	-1.8	—	ns	4, 5
LUPWAIT input hold from local bus clock		$t_{LBIXKH2}$	-1.3	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)		t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKLOV1}$	—	-0.3	ns	4
	TSEC2_TXD[6:5] = 11 (default)			1.2		
Local bus clock to data valid for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKLOV2}$	—	-0.1	ns	4
	TSEC2_TXD[6:5] = 11 (default)			1.4		
Local bus clock to address valid for LAD	TSEC2_TXD[6:5] = 00	$t_{LBKLOV3}$	—	0	ns	4
	TSEC2_TXD[6:5] = 11 (default)			1.5		
Local bus clock to LALE assertion		$t_{LBKHOV4}$	—	0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKLOX1}$	-3.2	—	ns	4
	TSEC2_TXD[6:5] = 11 (default)		-2.3			
Output hold from local bus clock for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKLOX2}$	-3.2	—	ns	4
	TSEC2_TXD[6:5] = 11 (default)		-2.3			
Local bus clock to output high Impedance (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKLOZ1}$	—	0.2	ns	7
	TSEC2_TXD[6:5] = 11 (default)			1.5		

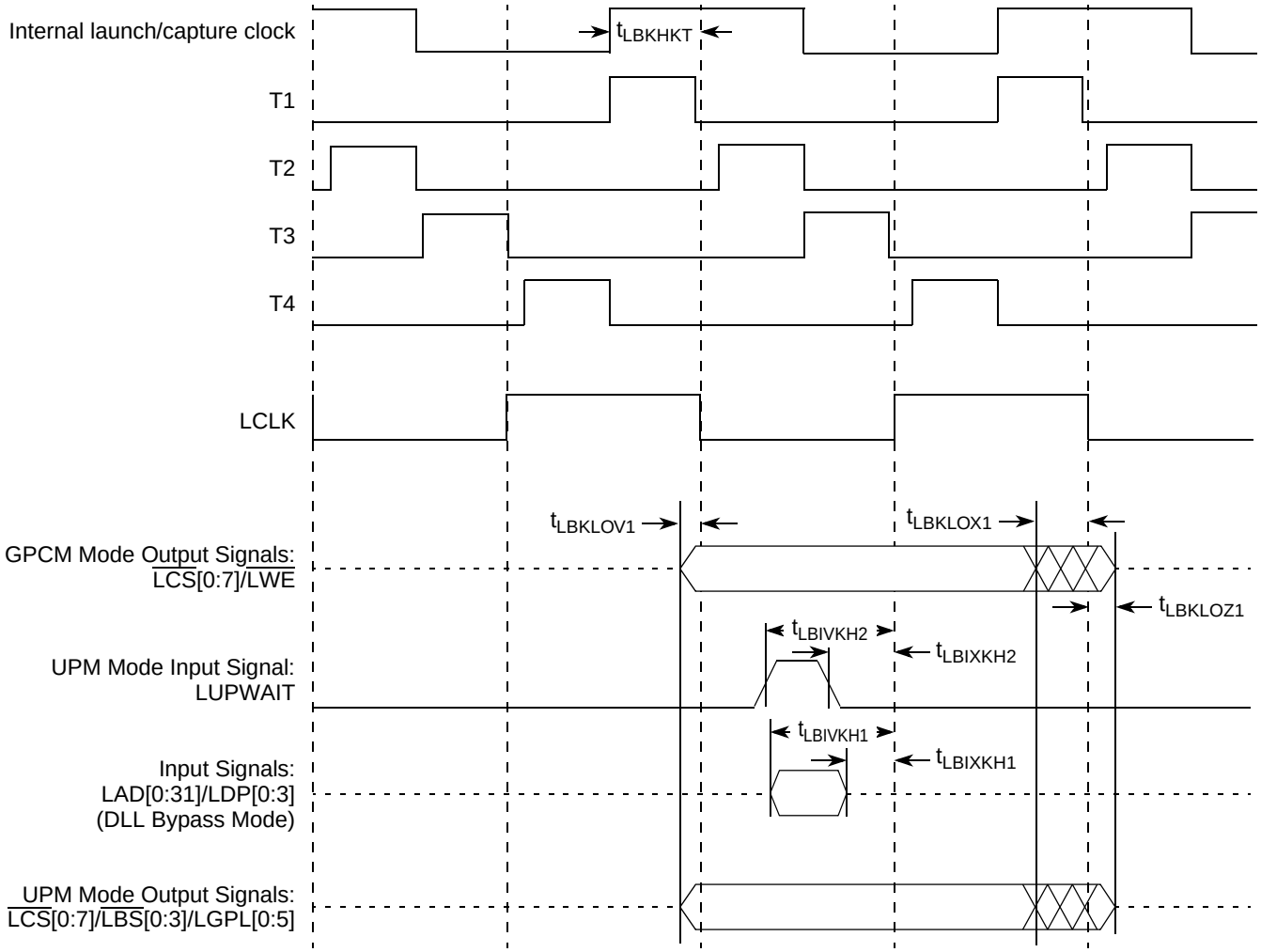


Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Bypass Mode)

The eye pattern for a data signal is generated by making a large number of recordings of the signal and then overlaying the recordings. The number of recordings used to generate the eye shall be large enough that further increasing the number of recordings used does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not. Each data signal in the interface shall be carrying random or pseudo-random data when the recordings are made. If pseudo-random data is used, the length of the pseudo-random sequence (repeat length) shall be long enough that increasing the length of the sequence does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not comply with the mask. The data carried by any given data signal in the interface may not be correlated with the data carried by any other data signal in the interface. The zero-crossings of the clock associated with a data signal shall be used as the timing reference for aligning the multiple recordings of the data signal when the recordings are overlaid.

While the method used to make the recordings and overlay them to form the eye pattern is not specified, the method used shall be demonstrably equivalent to the following method. The signal under test is repeatedly recorded with a digital oscilloscope in infinite persistence mode. Each recording is triggered by a zero-crossing of the clock associated with the data signal under test. Roughly half of the recordings are triggered by positive-going clock zero-crossings and roughly half are triggered by negative-going clock zero-crossings. Each recording is at least 1.9 UI in length (to ensure that at least one complete eye is formed) and begins 0.5 UI before the trigger point (0.5 UI before the associated clock zero-crossing). Depending on the length of the individual recordings used to generate the eye pattern, one or more complete eyes will be formed. Regardless of the number of eyes, the eye whose center is immediately to the right of the trigger point is the eye used for compliance testing.

An example of an eye pattern generated using the above method with recordings 3 UI in length is shown in Figure 39. In this example, there is no skew between the signal under test and the associated clock used to trigger the recordings. If skew was present, the eye pattern would be shifted to the left or right relative to the oscilloscope trigger point.

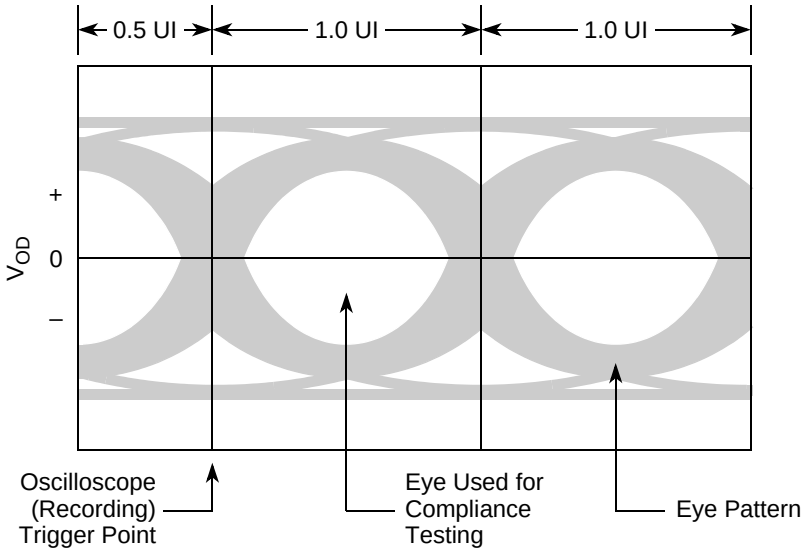


Figure 39. Example Driver Output Eye Pattern

Figure 42 shows the definitions of the data to clock static skew parameter $t_{SKEW,PAIR}$ and the data valid window parameter DV. The data and frame bits are those that are associated with the clock. The figure applies for all zero-crossings of the clock. All of the signals are differential signals. V_D represents V_{OD} for the transmitter and V_{ID} for the receiver. The center of the eye is defined as the midpoint of the region in which the magnitude of the signal voltage is greater than or equal to the minimum DV voltage.

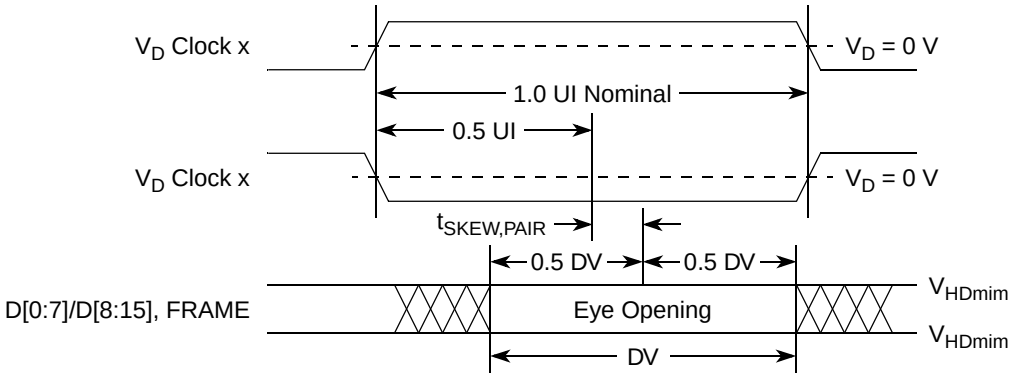


Figure 42. Data to Clock Skew

Figure 43 shows the definition of the data to data static skew parameter t_{DPAIR} and how the skew parameters are applied.

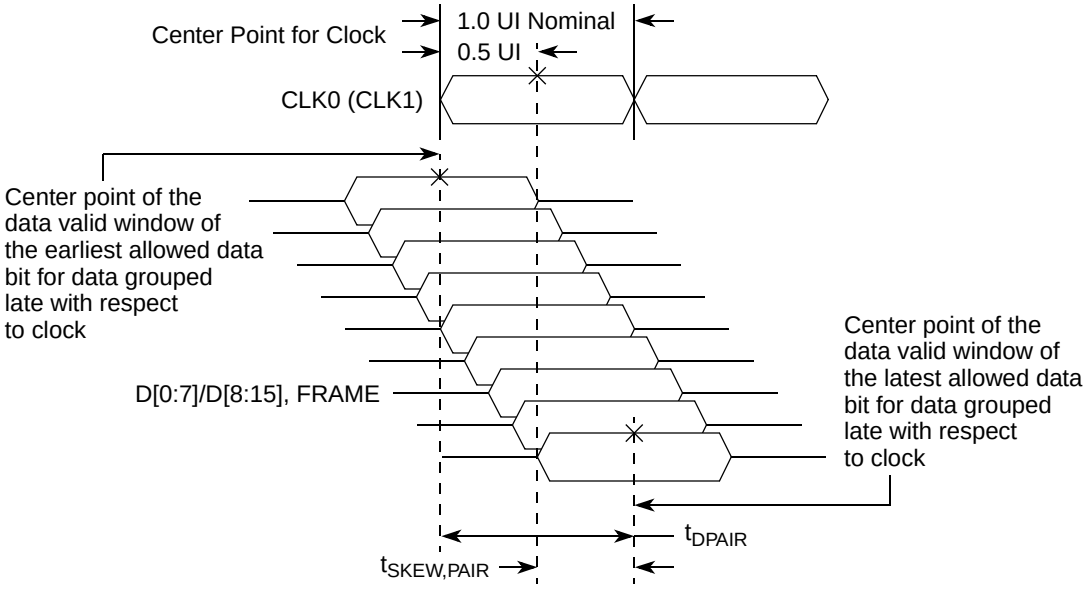


Figure 43. Static Skew Diagram

14 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions.

14.1 Package Parameters for the MPC8540 FC-PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip plastic ball grid array (FC-PBGA).

Die size	12.2 mm × 9.5 mm
Package outline	29 mm × 29 mm
Interconnects	783
Pitch	1 mm
Minimum module height	3.07 mm
Maximum module height	3.75 mm
Solder Balls	62 Sn/36 Pb/2 Ag
Ball diameter (typical)	0.5 mm

Table 53. MPC8540 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
System Control				
$\overline{\text{HRESET}}$	AH16	I	OV_{DD}	
$\overline{\text{HRESET\_REQ}}$	AG20	O	OV_{DD}	
$\overline{\text{SRESET}}$	AF20	I	OV_{DD}	
$\overline{\text{CKSTP\_IN}}$	M11	I	OV_{DD}	
$\overline{\text{CKSTP\_OUT}}$	G1	O	OV_{DD}	2, 4
Debug				
TRIG_IN	N12	I	OV_{DD}	
TRIG_OUT/READY	G2	O	OV_{DD}	6, 9, 19
MSRCID[0:1]	J9, G3	O	OV_{DD}	5, 6, 9
MSRCID[2:4]	F3, F5, F2	O	OV_{DD}	6
MDVAL	F4	O	OV_{DD}	6
Clock				
SYSCLK	AH21	I	OV_{DD}	
RTC	AB23	I	OV_{DD}	
CLK_OUT	AF22	O	OV_{DD}	11
JTAG				
TCK	AF21	I	OV_{DD}	
TDI	AG21	I	OV_{DD}	12
TDO	AF19	O	OV_{DD}	11
TMS	AF23	I	OV_{DD}	12
$\overline{\text{TRST}}$	AG23	I	OV_{DD}	12
DFT				
$\overline{\text{LSSD\_MODE}}$	AG19	I	OV_{DD}	21
L1_TSTCLK	AB22	I	OV_{DD}	21
L2_TSTCLK	AG22	I	OV_{DD}	21
TEST_SEL	AH20	I	OV_{DD}	3
Thermal Management				
THERM0	AG2	I	—	14
THERM1	AH3	I	—	14

Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-millennium.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the MPC8540 to function in various environments.

16.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8540 thermal model is shown in Figure 46. Five cuboids are used to represent this device. To simplify the model, the solder balls and substrate are modeled as a single block 29x29x1.47 mm with the conductivity adjusted accordingly. For modeling, the planar dimensions of the die are rounded to the nearest mm, so the die is modeled as 10x12 mm at a thickness of 0.76 mm. The bump/underfill layer is modeled as a collapsed resistance between the die and substrate assuming a conductivity of 0.6 in-plane and 1.9 W/m•K in the thickness dimension of 0.76 mm. The lid attach adhesive is also modeled as a collapsed resistance with dimensions of 10x12x0.050 mm and the conductivity of 1 W/m•K. The nickel plated copper lid is modeled as 12x14x1 mm. Note that the die and lid are not centered on the substrate; there is a 1.5 mm offset documented in the case outline drawing in Figure 44.

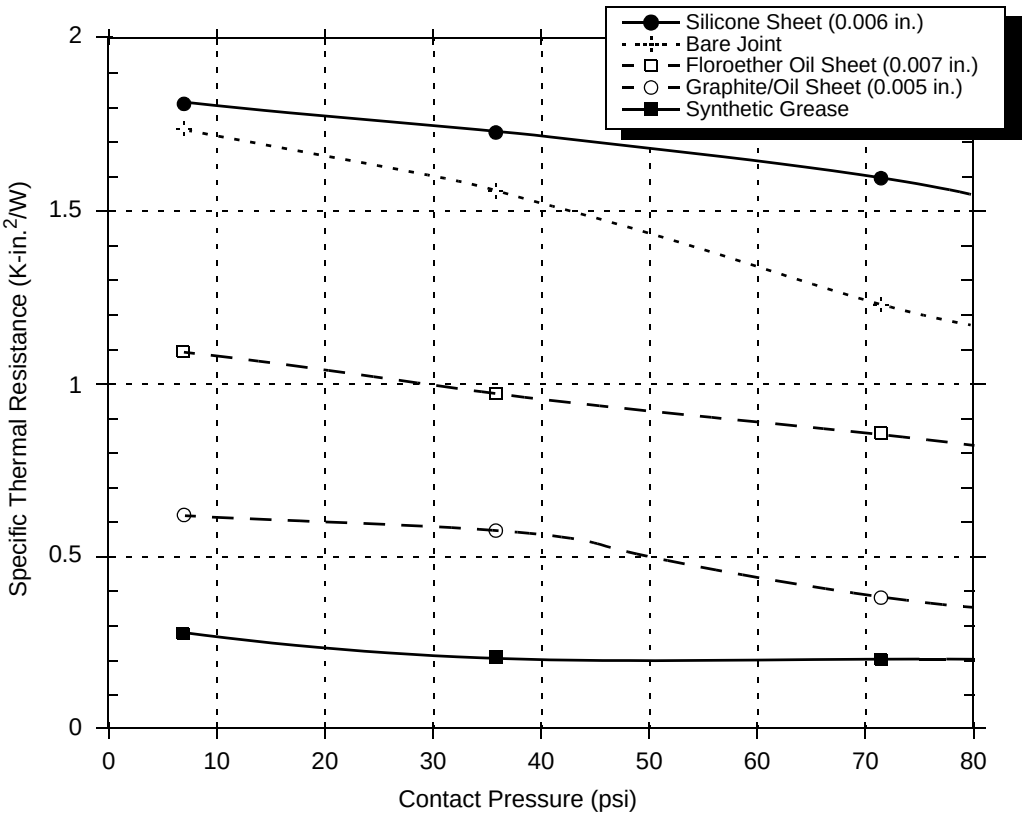


Figure 48. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

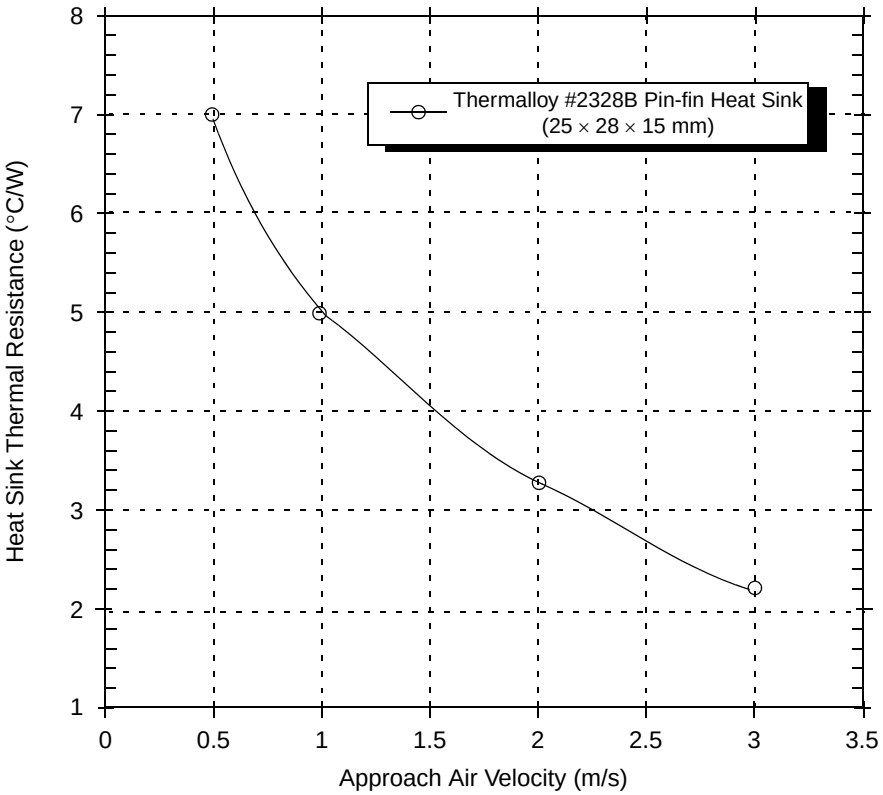


Figure 49. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

16.2.4.2 Case 2

Every system application has different conditions that the thermal management solution must solve. As an alternate example, assume that the air reaching the component is 85 C with an approach velocity of 1 m/sec. For a maximum junction temperature of 105 C at 7 W, the total thermal resistance of junction to case thermal resistance plus thermal interface material plus heat sink thermal resistance must be less than 2.8 C/W. The value of the junction to case thermal resistance in Table 59 includes the thermal interface resistance of a thin layer of thermal grease as documented in footnote 4 of the table. Assuming that the heat sink is flat enough to allow a thin layer of grease or phase change material, then the heat sink must be less than 2 C/W.

Millennium Electronics (MEI) has tooled a heat sink MTHERM-1051 for this requirement assuming a compactPCI environment at 1 m/sec and a heat sink height of 12 mm. The MEI solution is illustrated in Figure 50 and Figure 51. This design has several significant advantages:

- The heat sink is clipped to a plastic frame attached to the application board with screws or plastic inserts at the corners away from the primary signal routing areas.
- The heat sink clip is designed to apply the force holding the heat sink in place directly above the die at a maximum force of less than 10 lbs.
- For applications with significant vibration requirements, silicone damping material can be applied between the heat sink and plastic frame.

17 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8540.

17.1 System Clocking

The MPC8540includes two PLLs.

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 15.2, “Platform/System PLL Ratio.”
2. The e500 Core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 15.3, “e500 Core PLL Ratio.”

17.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}1$ and $AV_{DD}2$, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide three independent filter circuits as illustrated in Figure 52, one to each of the three AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias.

Figure 52 shows the PLL power supply filter circuit.

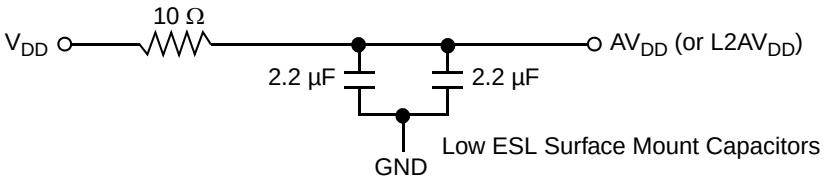


Figure 52. PLL Power Supply Filter Circuit

17.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8540 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8540 system, and the MPC8540 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pins of the MPC8540. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

17.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}, GV_{DD}, or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and GND pins of the MPC8540.

17.5 Output Buffer DC Impedance

The MPC8540 drivers are characterized over process, voltage, and temperature. There are two driver types: a push-pull single-ended driver (open drain for I^2C) for all buses except RapidIO, and a current-steering differential driver for the RapidIO port.

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 53). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

17.6 Configuration Pin Muxing

The MPC8540 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While HRESET is asserted however, these pins are treated as inputs. The value presented on these pins while HRESET is asserted, is latched when HRESET deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during HRESET (and for platform/system clocks after HRESET deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

17.7 Pull-Up Resistor Requirements

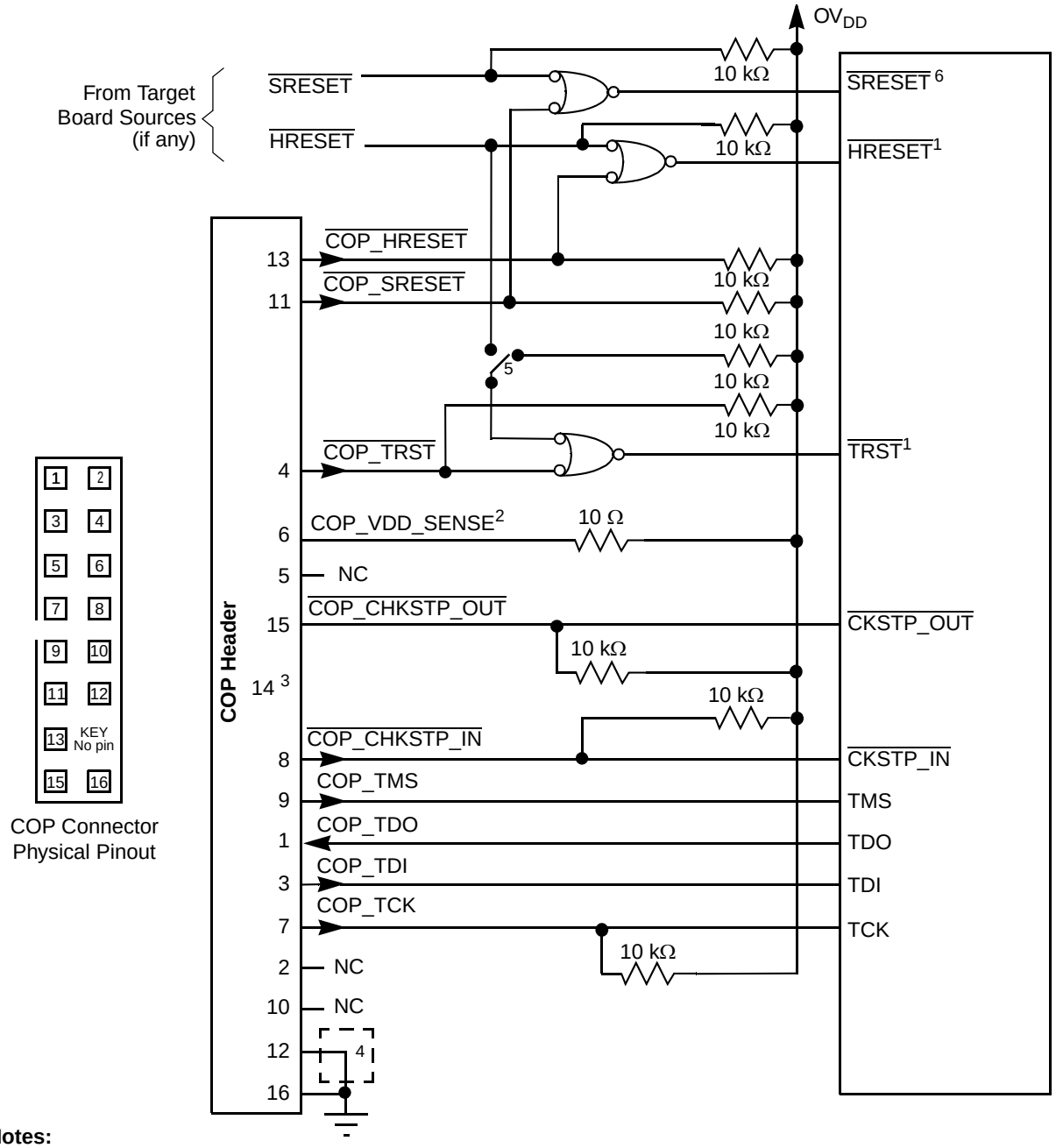
The MPC8540 requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including EPIC interrupt pins. I^2C open drain type pins should be pulled up with ~1 kΩ resistors.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 55. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

TSEC1_TXD[3:0] must not be pulled low during reset. Some PHY chips have internal pulldowns that could cause this to happen. If such PHY chips are used, then a pullup must be placed on these signals strong enough to restore these signals to a logical 1 during reset.

Three test pins also require pull-up resistors (100 Ω - 1 kΩ). These pins are L1_TSTCLK, L2_TSTCLK, and LSSD_MODE. These signals are for factory use only and must be pulled up to OVDD for normal machine operation.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 55. JTAG Interface Connection

18 Document Revision History

Table 61 provides a revision history for this hardware specification.

Table 61. Document Revision History

Rev. No.	Substantive Change(s)
4.1	Inserted Figure 3 and paragraph above it. Added PCI/PCI-X row to Input Voltage characteristic and added footnote 6 to Table 1.
4	Updated Note in Section 2.1.2, “Power Sequencing.” Updated back page information.
3.5	Updated Section 2.1.2, “Power Sequencing.” Replaced Section 17.8, “JTAG Configuration Signals.”
3.4	Corrected MV_{REF} Max Value in Table 1. Corrected MV_{REF} Max Value in Table 2. Added new revision level information to Table 62
3.3	Updated MV_{REF} Max Value in Table 1. Removed Figure 3. In Table 4, replaced TBD with power numbers and added footnote. Updated specs and footnotes in Table 8. Corrected max number for MV_{REF} in Table 13. Changed parameter “Clock cycle duration” to “Clock period” in Table 29. Added note 4 to $t_{LBKHOV1}$ and removed LALE reference from $t_{LBKHOV3}$ in Table 36 and Table 37. Updated LALE signal in Figure 19 and Figure 20. Modified Figure 23. Modified Figure 55.

Table 61. Document Revision History (continued)

Rev. No.	Substantive Change(s)
3.0	Table 1—Corrected MII management voltage reference Section 2.1.3—New Table 2—Corrected MII management voltage reference Table 4—Added V_{DD} power table Table 5—Added AV_{DD} power table Table 7—New Table 8—New Table 9—New Table 13—Added overshoot/undershoot note. Figure 4—New Table 16—Restated $t_{MCKSKEW1}$ as $t_{MCKSKEW}$, removed $t_{MCKSKEW2}$; added speed-specific minimum values for 333, 266, and 200 MHz; updated t_{DDSHME} values. Updated chapter to reflect that GMII, MII and TBI can be run with 2.5V signalling. Table 34—Added MDIO output valid timing Table 36—Updated $t_{LBIVKH1}$, $t_{LBIXKH1}$, and t_{LBOTOT}. Table 37—New Table 20, Table 22, Table 24—Updated clock reference Table 44—Updated t_{PCIVKH} Section 14.1— Changed minimum height from 2.22 to 3.07 and maximum from 2.76 to 3.75 Table 53.—Updated MII management voltage reference and added note 20. Section 16.2.4.1—Changed θ_{JC} from 0.3 to 0.8; changed die-junction temperature from 67 to 71 Section 17.7—Added paragraph that begins “TSEC1_TXD[3:0]...”

Table 61. Document Revision History (continued)

Rev. No.	Substantive Change(s)
1.2	Section 1.1.1—Updated feature list. Section 1.2.1.1—Updated notes for Table 1. Section 1.2.1.2—Removed 5-V PCI interface overshoot and undershoot figure. Section 1.2.1.3—Added this section to summarize impedance driver settings for various interfaces. Section 1.4—Updated rows in Reset Initialization timing specifications table. Added a table with DLL and PLL timing specifications. Section 1.5.2.2—Updated note 6 of DDR SDRAM Output AC Timing Specifications table. Section 1.7—Changed the minimum input low current from -600 to -15 μA for the RGMII DC electrical characteristics. Section 1.8.2—Changed LCS[3:4] to TSEC1_TXD[6:5] in. Updated notes regarding LCS[3:4]. Section 1.13.2—Updated the mechanical dimensions diagram for the package. Section 1.13.3—Updated the notes for LBCTL, TRIG_OUT, and ASLEEP. Corrected pin assignments for IIC_SDA and IIC_SCL. Corrected reserved pin assignment of V11 to U11. V11 is actually $\overline{\text{PCI\_STOP}}$. Section 1.14.1—Updated the table for frequency options with respect to platform/CCB frequencies. Section 1.14.4—Edited Frequency options with respect to memory bus speeds.
1.1	Section 1.6.1—Added symbols and note for the GTX_CLK125 timing parameters. Section 1.11.3—Updated pin list table: LGPL5/LSDAMUX to LGPL5, LA[27:29] and LA[30:31] to LA[27:31], FEC_TXD[0:3] to FEC_TXD[3:0], FEC_RXD[0:3] to FEC_RXD[3:0], TRST to $\overline{\text{TRST}}$, added GBE Clocking section and EC_GTX_CLK125 signal. Updated thermal model information to match current offering.
1	Original Customer Version.

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