NXP USA Inc. - MPC8540PX533JB Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1), 10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8540px533jb

  - Interrupts can be routed to the e500 core's standard or critical interrupt inputs
  - Interrupt summary registers allow fast identification of interrupt source
- I^{2}C controller
  - Two-wire interface
  - Multiple master support
  - Master or slave I^{2}C mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the I^{2}C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I^{2}C addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
  - Programming model compatible with the original 16450 UART and the PC16550D
- 10/100 fast Ethernet controller (FEC)
  - Operates at 10 to 100 megabits per second (Mbps) as a device debug and maintenance port
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 166 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
  - Three protocol engines available on a per chip select basis:
    - General purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-,16-, or 32-bit)
- Two three-speed (10/100/1Gb) Ethernet controllers (TSECs)
  - Dual IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab compliant controllers
  - Support for different Ethernet physical interfaces:
    - 10/100/1Gb Mbps IEEE 802.3 GMII
    - 10/100 Mbps IEEE 802.3 MII
    - 10 Mbps IEEE 802.3 MII
    - 1000 Mbps IEEE 802.3z TBI
    - 10/100/1Gb Mbps RGMII/RTBI
  - Full- and half-duplex support

- Power management
  - Fully static 1.2-V CMOS design with 3.3- and 2.5-V I/O
  - Supports power saving modes: doze, nap, and sleep
  - Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle.
- System performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the 8 counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- System access port
  - Uses JTAG interface and a TAP controller to access entire system memory map
  - Supports 32-bit accesses to configuration registers
  - Supports cache-line burst accesses to main memory
  - Supports large block (4-Kbyte) uploads and downloads
  - Supports continuous bit streaming of entire block for fast upload and download
- IEEE 1149.1-compliant, JTAG boundary scan
- 783 FC-PBGA package

2 Electrical Characteristics

This section provides the electrical specifications and thermal characteristics for the MPC8540. The MPC8540 is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8540 for the 3.3-V signals, respectively.

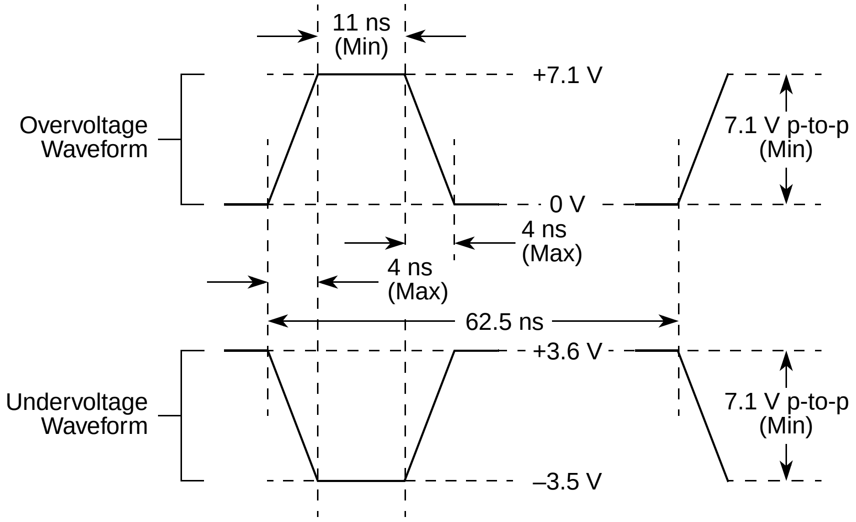

Figure 3. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

2.1.4 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25	OV_{DD} = 3.3 V	1
	42 (default)		
PCI signals	25		2
	42 (default)		
DDR signal	20	GV_{DD} = 2.5 V	
TSEC/10/100 signals	42	LV_{DD} = 2.5/3.3 V	
DUART, system control, I2C, JTAG	42	OV_{DD} = 3.3 V	
RapidIO N/A (LVDS signaling)	N/A		

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the $\overline{\text{PCI\_GNT1}}$ signal at reset.

Table 13. DDR SDRAM DC Electrical Characteristics (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
MV_{REF} input leakage current	I_{VREF}	—	100	μA	

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. V_{IH} can tolerate an overshoot of 1.2V over GV_{DD} for a pulse width of ≤3 ns, and the pulse width cannot be greater than t_{MCK}. V_{IL} can tolerate an undershoot of 1.2V below GND for a pulse width of ≤3 ns, and the pulse width cannot be greater than t_{MCK}.
5. Output leakage is measured with all outputs disabled, $0\ V \leq V_{OUT} \leq GV_{DD}$.

Table 14 provides the DDR capacitance.

Table 14. DDR SDRAM Capacitance

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, MSYNC_IN	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 2.5\ V \pm 0.125\ V$, f = 1 MHz, $T_A = 25°C$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak to peak) = 0.2 V.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 15 provides the input AC timing specifications for the DDR SDRAM interface.

Table 15. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.31$	V	
AC input high voltage	V_{IH}	$MV_{REF} + 0.31$	$GV_{DD} + 0.3$	V	
MDQS—MDQ/MECC input skew per byte	t_{DISKEW}			ps	1, 2
For DDR = 333 MHz		-750	750		
For DDR ≤ 266 MHz		-1125	1125		

Note:

1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if $0 \leq n \leq 7$) or ECC (MECC[{0...7}] if n=8).
2. For timing budget analysis, the MPC8540 consumes ±550 ps of the total budget.

Table 30. MII DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3 V	OV_{DD}	3.13	3.47	V
Output high voltage (OV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.40	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} = Min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	1.70	—	V
Input low voltage	V_{IL}	–0.3	0.90	V
Input high current (V_{IN}= OV_{DD} [1])	I_{IH}	—	40	μA
Input low current (V_{IN}= GND [1])	I_{IL}	–600	—	μA

Note:

1.Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

8.3.2 MII AC Electrical Specifications

This section describes the MII transmit and receive AC specifications.

8.3.2.1 MII Transmit AC Timing Specifications

Table 31 provides the MII transmit AC timing specifications.

Table 31. MII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise and fall time	t_{MTXR}, t_{MTXF} [2,3]	1.0	—	4.0	ns

Note:

1.The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) from the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII (M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2.Signal timings are measured at 0.7 V and 1.9 V voltage levels.

3.Guaranteed by design.

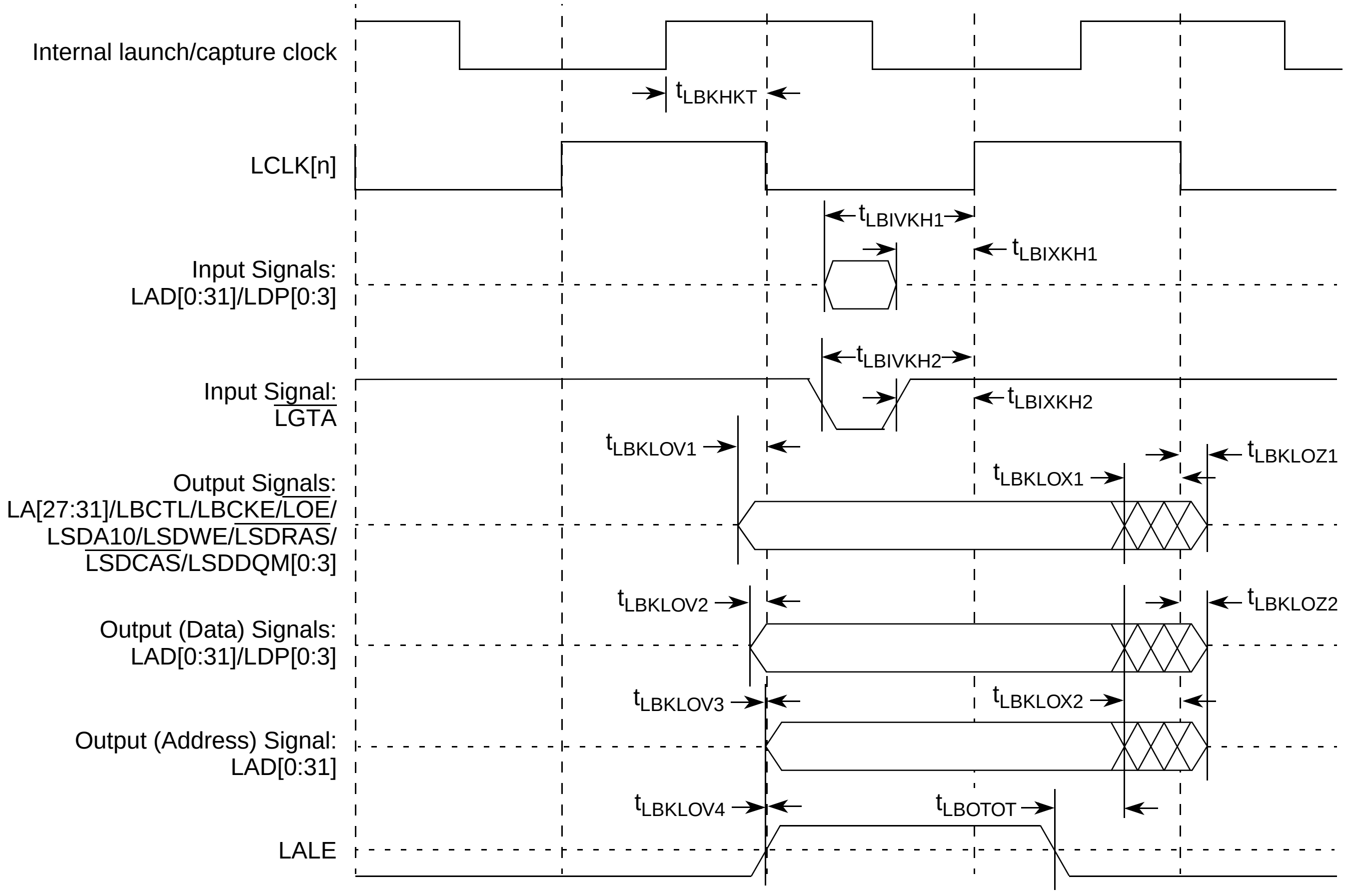

Figure 20. Local Bus Signals (DLL Bypass Mode)

Figure 31 shows the AC timing diagram for the I^2C bus.

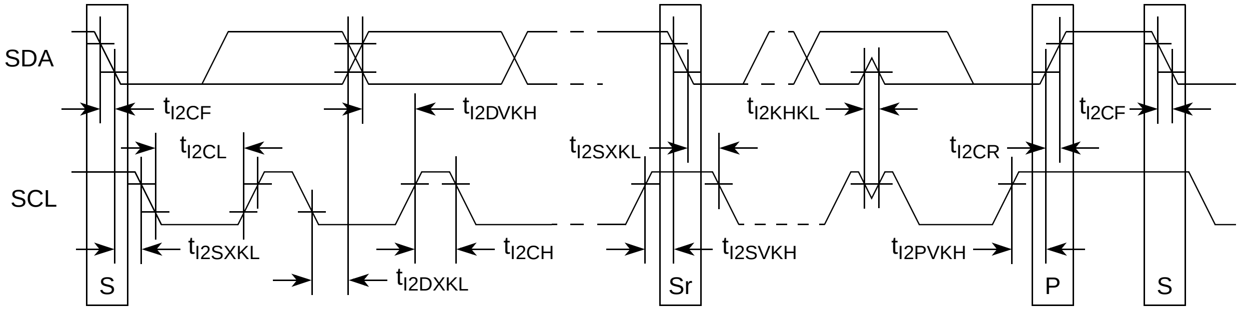

Figure 31. I^2C Bus AC Timing Diagram

12 PCI/PCI-X

This section describes the DC and AC electrical specifications for the PCI/PCI-X bus of the MPC8540.

12.1 PCI/PCI-X DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the PCI/PCI-X interface of the MPC8540.

Table 41. PCI/PCI-X DC Electrical Characteristics [1]

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [2] = 0 V or $V_{IN} = V_{DD}$)	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Notes:

1.Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.

2.Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

Figure 18 provides the AC test load for PCI and PCI-X.

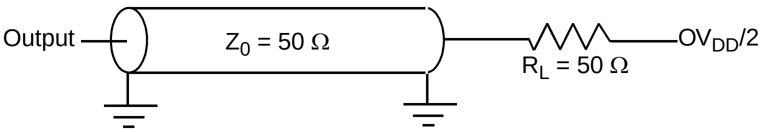

Figure 32. PCI/PCI-X AC Test Load

Figure 33 shows the PCI/PCI-X input AC timing conditions.

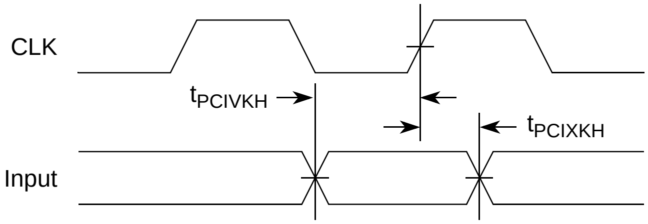

Figure 33. PCI-PCI-X Input AC Timing Measurement Conditions

Figure 34 shows the PCI/PCI-X output AC timing conditions.

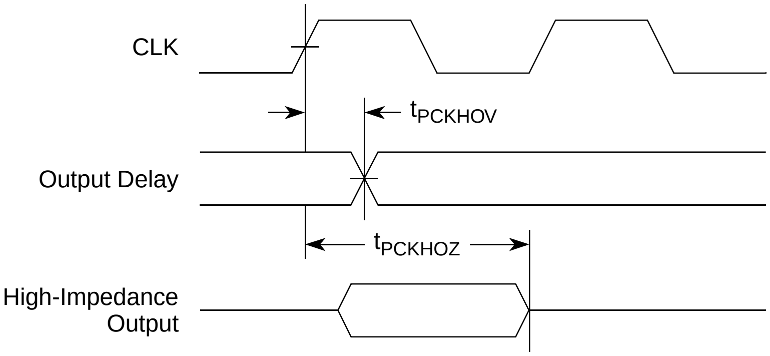

Figure 34. PCI-PCI-X Output AC Timing Measurement Condition

Table 43 provides the PCI-X AC timing specifications at 66 MHz.

Table 43. PCI-X AC Timing Specifications at 66 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	—	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t_{PCKHOX}	0.7	—	ns	1, 10
SYSCLK to output high impedance	t_{PCKHOZ}	—	7	ns	1, 4, 8, 11
Input setup time to SYSCLK	t_{PCIVKH}	1.7	—	ns	3, 5
Input hold time from SYSCLK	t_{PCIXKH}	0.5	—	ns	10
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time	t_{PCRVRH}	10	—	clocks	11
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	11
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	9, 11

Table 44. PCI-X AC Timing Specifications at 133 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time	t_{PCRHIX}	0	50	ns	6, 12

Notes:

1.See the timing measurement conditions in the *PCI-X 1.0a Specification*.

2.Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.

3.Setup time for point-to-point signals applies to $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ only. All other signals are bused.

4.For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

5.Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.

6.Maximum value is also limited by delay to the first transaction (time for $\overline{\text{HRESET}}$ high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of $\overline{\text{HRESET}}$ must be negated no later than two clocks before the first $\overline{\text{FRAME}}$ and must be floated no later than one clock before $\overline{\text{FRAME}}$ is asserted.

7.A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.

8.Device must meet this specification independent of how many outputs switch simultaneously.

9.The timing parameter t_{PCIVKH} is a minimum of 1.4 ns rather than the minimum of 1.2 ns in the *PCI-X 1.0a Specification.*

10.The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*

11.Guaranteed by characterization.

12.Guaranteed by design.

13 RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8540.

13.1 RapidIO DC Electrical Characteristics

RapidIO driver and receiver DC electrical characteristics are provided in Table 45 and Table 46, respectively.

Table 45. RapidIO 8/16 LP-LVDS Driver DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Characteristic	Symbol	Min	Max	Unit	Notes
Differential output high voltage	V_{OHD}	247	454	mV	1, 2
Differential output low voltage	V_{OLD}	–454	–247	mV	1, 2
Differential offset voltage	ΔV_{OSD}	—	50	mV	1,3
Output high common mode voltage	V_{OHCM}	1.125	1.375	V	1, 4
Output low common mode voltage	V_{OLCM}	1.125	1.375	V	1, 5

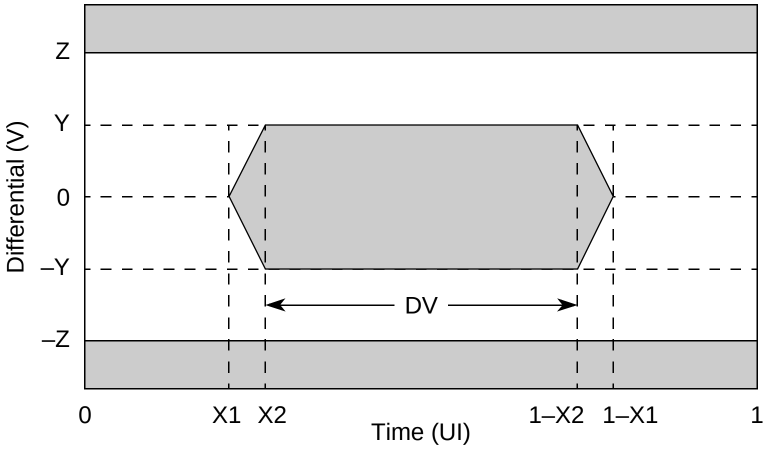

Figure 37. Example Compliance Mask

Y = minimum data valid amplitude
Z = maximum amplitude
1 UI = 1 unit interval = 1/baud rate
X1 = end of zero crossing region
X2 = beginning of data valid window
DV = data valid window = 1 – 2 × X2

The waveform of the signal under test must fall within the unshaded area of the mask to be compliant. Different masks are used for the driver output and the receiver input allowing each to be separately specified.

13.3.1 RapidIO Driver AC Timing Specifications

Driver AC timing specifications are provided in Table 47, Table 48, and Table 49. A driver shall comply with the specifications for each data rate/frequency for which operation of the driver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The output of a driver shall be connected to a 100 Ω, ±1%, differential (bridged) resistive load.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7]).

Table 47. RapidIO Driver AC Timing Specifications—500 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential output high voltage	V_{OHD}	200	540	mV	1
Differential output low voltage	V_{OLD}	–540	–200	mV	1

The eye pattern for a data signal is generated by making a large number of recordings of the signal and then overlaying the recordings. The number of recordings used to generate the eye shall be large enough that further increasing the number of recordings used does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not. Each data signal in the interface shall be carrying random or pseudo-random data when the recordings are made. If pseudo-random data is used, the length of the pseudo-random sequence (repeat length) shall be long enough that increasing the length of the sequence does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not comply with the mask. The data carried by any given data signal in the interface may not be correlated with the data carried by any other data signal in the interface. The zero-crossings of the clock associated with a data signal shall be used as the timing reference for aligning the multiple recordings of the data signal when the recordings are overlaid.

While the method used to make the recordings and overlay them to form the eye pattern is not specified, the method used shall be demonstrably equivalent to the following method. The signal under test is repeatedly recorded with a digital oscilloscope in infinite persistence mode. Each recording is triggered by a zero-crossing of the clock associated with the data signal under test. Roughly half of the recordings are triggered by positive-going clock zero-crossings and roughly half are triggered by negative-going clock zero-crossings. Each recording is at least 1.9 UI in length (to ensure that at least one complete eye is formed) and begins 0.5 UI before the trigger point (0.5 UI before the associated clock zero-crossing). Depending on the length of the individual recordings used to generate the eye pattern, one or more complete eyes will be formed. Regardless of the number of eyes, the eye whose center is immediately to the right of the trigger point is the eye used for compliance testing.

An example of an eye pattern generated using the above method with recordings 3 UI in length is shown in Figure 39. In this example, there is no skew between the signal under test and the associated clock used to trigger the recordings. If skew was present, the eye pattern would be shifted to the left or right relative to the oscilloscope trigger point.

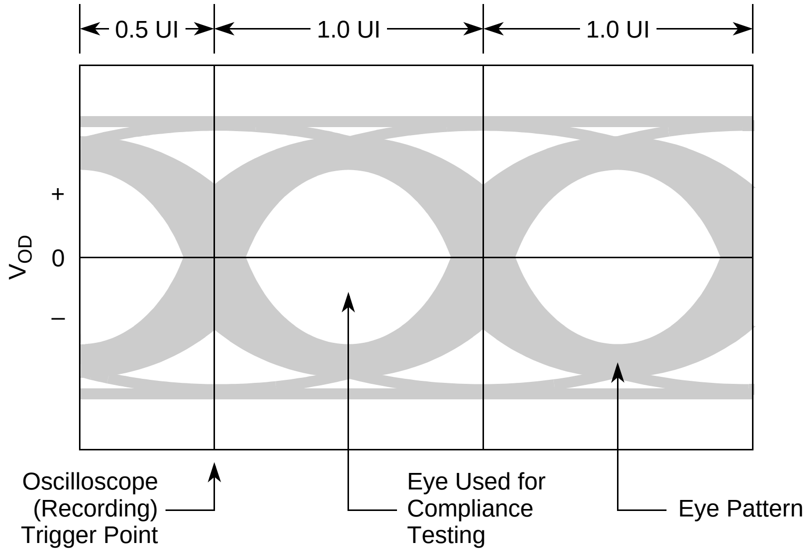

Figure 39. Example Driver Output Eye Pattern

13.3.2 RapidIO Receiver AC Timing Specifications

The RapidIO receiver AC timing specifications are provided in Table 50. A receiver shall comply with the specifications for each data rate/frequency for which operation of the receiver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The specifications apply over the receiver common mode and differential input voltage ranges.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7])

Table 50. RapidIO Receiver AC Timing Specifications—500 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1, 5
Data valid	DV	1080		ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}	—	380	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–300	300	ps	4

Notes:

1.Measured at $V_{ID} = 0$ V.

2.Measured using the RapidIO receive mask shown in Figure 40.

3.See Figure 43.

4.See Figure 42 and Figure 43.

5.Guaranteed by design.

Table 51. RapidIO Receiver AC Timing Specifications—750 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1, 5
Data valid	DV	600	—	ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}	—	400	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–267	267	ps	4

Notes:

1.Measured at $V_{ID} = 0$ V.

2.Measured using the RapidIO receive mask shown in Figure 40.

3.See Figure 43.

4.See Figure 42 and Figure 43.

5.Guaranteed by design.

Table 53. MPC8540 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LCS6/DMA_DACK2	P27	O	OV_{DD}	1
LCS7/DMA_DDONE2	P28	O	OV_{DD}	1
LDP[0:3]	AA27, AA28, T26, P21	I/O	OV_{DD}	
LGPL0/LSDA10	U19	O	OV_{DD}	5, 9
LGPL1/LSDWE	U22	O	OV_{DD}	5, 9
LGPL2/LOE/LSDRAS	V28	O	OV_{DD}	8, 9
LGPL3/LSDCAS	V27	O	OV_{DD}	5, 9
LGPL4/LGTA/LUPWAIT/ LPBSE	V23	I/O	OV_{DD}	22
LGPL5	V22	O	OV_{DD}	5, 9
LSYNC_IN	T27	I	OV_{DD}	
LSYNC_OUT	T28	O	OV_{DD}	
LWE[0:1]/LSDDQM[0:1]/LBS [0:1]	AB28, AB27	O	OV_{DD}	1, 5, 9
LWE[2:3]/LSDDQM[2:3]/LBS [2:3]	T23, P24	O	OV_{DD}	1, 5, 9
DMA				
DMA_DREQ[0:1]	H5, G4	I	OV_{DD}	
DMA_DACK[0:1]	H6, G5	O	OV_{DD}	
DMA_DDONE[0:1]	H7, G6	O	OV_{DD}	
DUART				
UART_SIN[0:1]	AE2, AD5	I	OV_{DD}	
UART_SOUT[0:1]	AE3, AD2	O	OV_{DD}	
UART_CTS[0:1]	U9, U7	I	OV_{DD}	
UART_RTS[0:1]	AD6, AD1	O	OV_{DD}	
Programmable Interrupt Controller				
MCP	AG17	I	OV_{DD}	
UDE	AG16	I	OV_{DD}	
IRQ[0:7]	AA18, Y18, AB18, AG24, AA21, Y19, AA19, AG25	I	OV_{DD}	
IRQ8	AB20	I	OV_{DD}	9
IRQ9/DMA_DREQ3	Y20	I	OV_{DD}	1
IRQ10/DMA_DACK3	AF26	I/O	OV_{DD}	1
IRQ11/DMA_DDONE3	AH24	I/O	OV_{DD}	1

15.4 Frequency Options

Table 58 shows the expected frequency values for the platform frequency when using a CCB to SYSCLK ratio in comparison to the memory bus speed.

Table 58. Frequency Options with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)								
	16.67	**25**	**33.33**	**41.63**	**66.67**	**83**	**100**	**111**	**133.33**
	Platform/CCB Frequency (MHz)								
2							200	222	267
3					200	250	300	333	
4					267	333			
5				208	333				
6			200	250					
8		200	267	333					
9		225	300						
10		250	333						
12	200	300							
16	267								

16 Thermal

This section describes the thermal specifications of the MPC8540.

16.1 Thermal Characteristics

Table 59 provides the package thermal characteristics for the MPC8540.

Table 59. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection on four layer board (2s2p)	$R_{\theta JMA}$	16	°C/W	1, 2
Junction-to-ambient (@100 ft/min or 0.5 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	14	°C/W	1, 2
Junction-to-ambient (@200 ft/min or 1 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	12	•C/W	1, 2
Junction-to-board thermal	$R_{\theta JB}$	7.5	•C/W	3

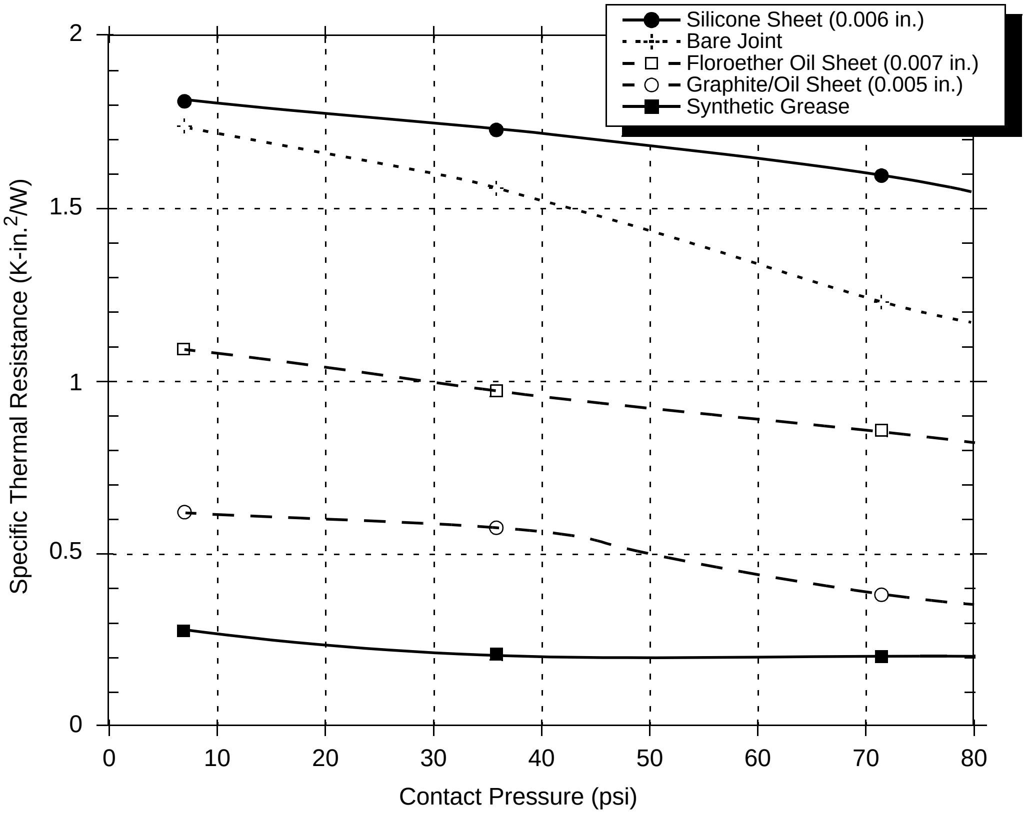

Figure 48. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

17 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8540.

17.1 System Clocking

The MPC8540includes two PLLs.

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 15.2, “Platform/System PLL Ratio.”
2. The e500 Core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 15.3, “e500 Core PLL Ratio.”

17.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD}1 and AV_{DD}2, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide three independent filter circuits as illustrated in Figure 52, one to each of the three AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias.

Figure 52 shows the PLL power supply filter circuit.

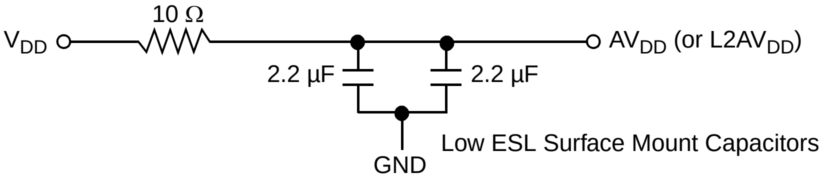

Figure 52. PLL Power Supply Filter Circuit

17.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8540 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8540 system, and the MPC8540 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pins of the MPC8540. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

17.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}, GV_{DD}, or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and GND pins of the MPC8540.

17.5 Output Buffer DC Impedance

The MPC8540 drivers are characterized over process, voltage, and temperature. There are two driver types: a push-pull single-ended driver (open drain for I^2C) for all buses except RapidIO, and a current-steering differential driver for the RapidIO port.

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 53). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

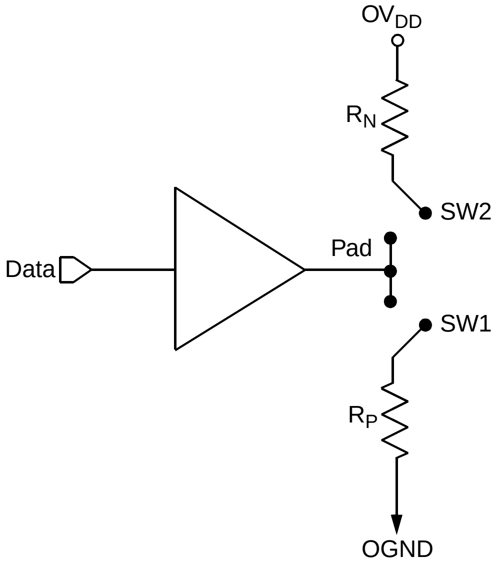

Figure 53. Driver Impedance Measurement

The output impedance of the RapidIO port drivers targets 200-Ω differential resistance. The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 60 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 60. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI/PCI-X	DDR DRAM	RapidIO	Symbol	Unit
R_N	43 Target	25 Target	20 Target	NA	Z_0	W
R_P	43 Target	25 Target	20 Target	NA	Z_0	W
Differential	NA	NA	NA	200 Target	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

17.8 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1 specification, but is provided on all processors that implement the Power Architecture. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 54 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 54, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 54 is common to all known emulators.

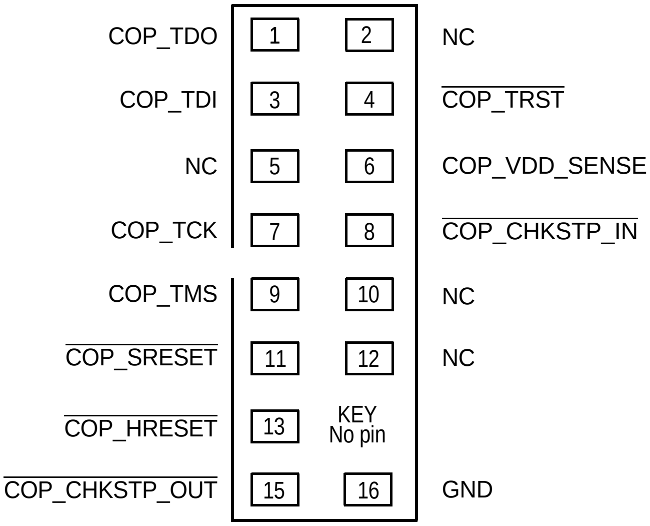

Figure 54. COP Connector Physical Pinout

17.8.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 55. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 kΩ resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.