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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

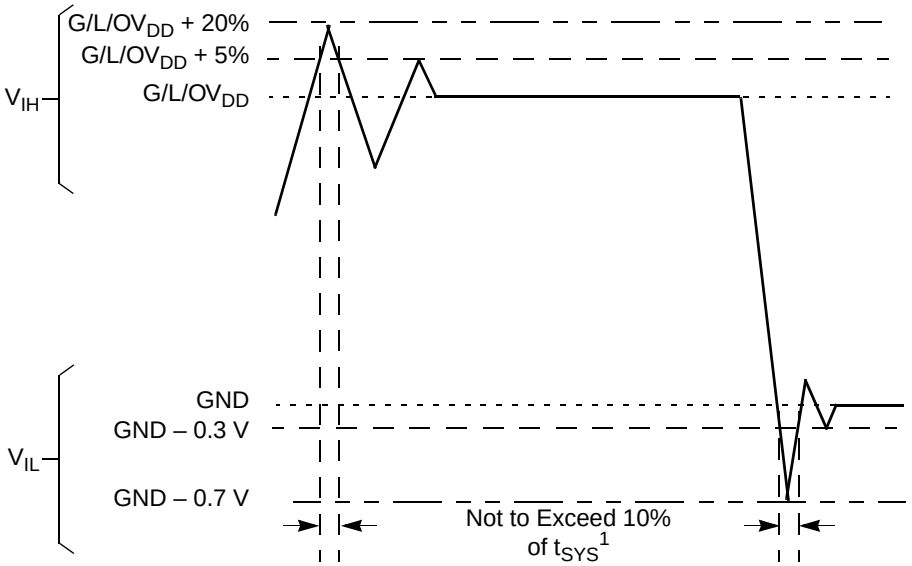
Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	833MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1), 10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8540px833lb

Table 2. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit
Input voltage	DDR DRAM signals	MV_{IN}	GND to GV_{DD}	V
	DDR DRAM reference	MV_{REF}	GND to $GV_{DD/2}$	V
	Three-speed Ethernet signals	LV_{IN}	GND to LV_{DD}	V
	PCI/PCI-X, local bus, RapidIO, 10/100 Ethernet, MII management, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V
Die-junction temperature		T_j	0 to 105	•C

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8540.



Note:
t_{SYS} refers to the clock period associated with the SYSCLK signal.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

The MPC8540 core voltage must always be provided at nominal 1.2 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

Figure 6 shows the DDR SDRAM output timing diagram.

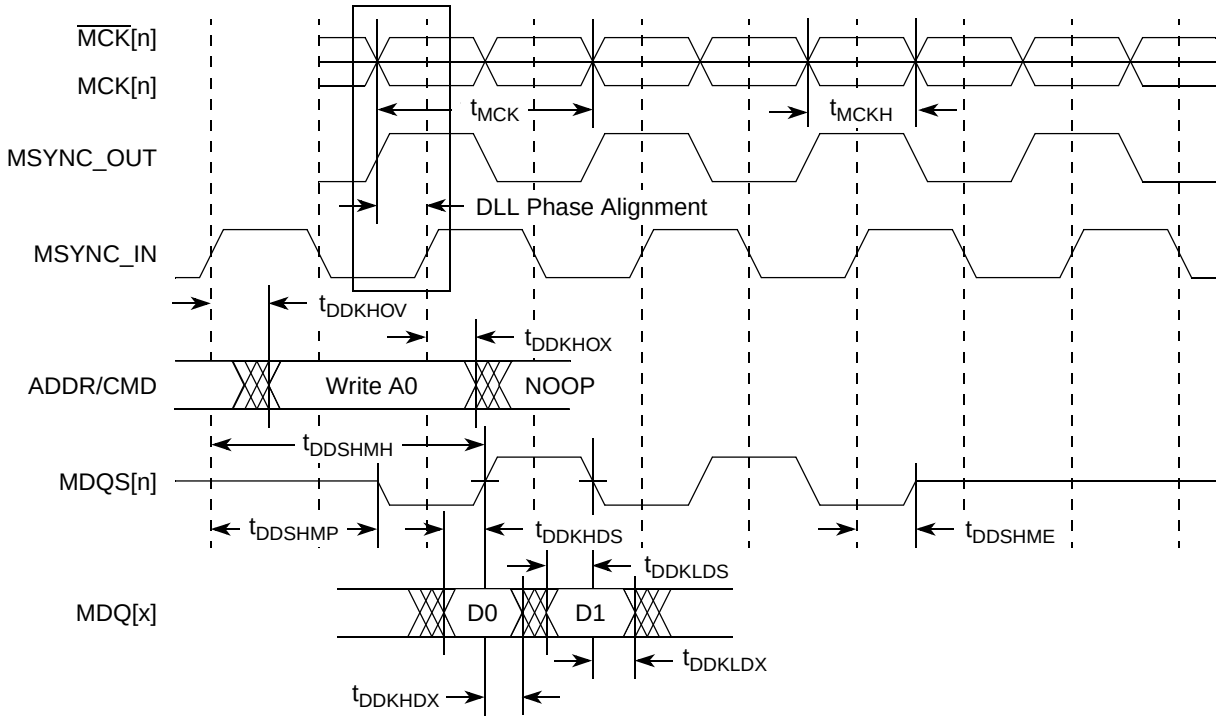


Figure 6. DDR SDRAM Output Timing Diagram

6.2.2.2 Load Effects on Address/Command Bus

Table 18 provides approximate delay information that can be expected for the address and command signals of the DDR controller for various loadings. These numbers are the result of simulations for one topology. The delay numbers will strongly depend on the topology used. These delay numbers show the total delay for the address and command to arrive at the DRAM devices. The actual delay could be different than the delays seen in simulation, depending on the system topology. If a heavily loaded system is used, the DLL loop may need to be adjusted to meet setup requirements at the DRAM.

Table 18. Expected Delays for Address/Command

Load	Delay	Unit
4 devices (12 pF)	3.0	ns
9 devices (27 pF)	3.6	ns
36 devices (108 pF) + 40 pF compensation capacitor	5.0	ns
36 devices (108 pF) + 80 pF compensation capacitor	5.2	ns

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8540.

7.1 DUART DC Electrical Characteristics

Table 19 provides the DC electrical characteristics for the DUART interface of the MPC8540.

Table 19. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:

1.Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 20 provides the AC timing parameters for the DUART interface of the MPC8540.

Table 20. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{CCB_CLK} / 1048576	baud	3
Maximum baud rate	f_{CCB_CLK} / 16	baud	1, 3
Oversample rate	16	—	2, 3

Notes:

1.Actual attainable baud rate will be limited by the latency of interrupt processing.

2.The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

3.Guaranteed by design.

8.2.2.2 MII Receive AC Timing Specifications

Table 26 provides the MII receive AC timing specifications.

Table 26. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX} [3]	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise and fall time	t_{MRXR}, t_{MRXF} [2,3]	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 11 shows the MII receive AC timing diagram.

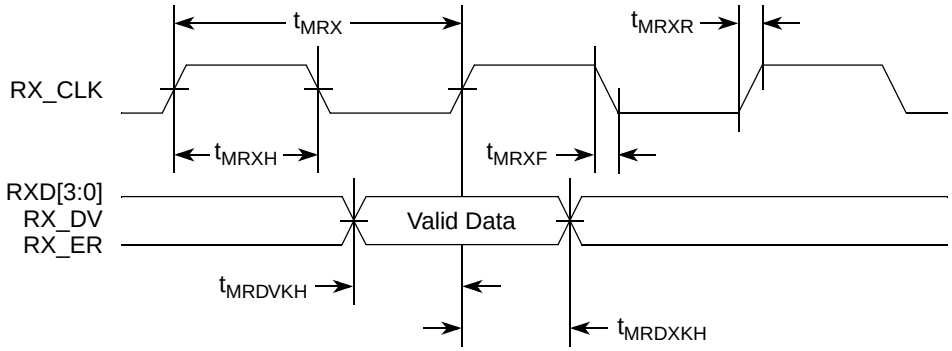


Figure 11. MII Receive AC Timing Diagram

8.2.4 RGMII and RTBI AC Timing Specifications

Table 29 presents the RGMII and RTBI AC timing specifications.

Table 29. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT} [5]	–500	0	500	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns
Clock period[3]	t_{RGT} [6]	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4]	t_{RGTH}/t_{RGT} [6]	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3]	t_{RGTH}/t_{RGT} [6]	40	50	60	%
Rise and fall time	t_{RGTR}, t_{RGTF} [6,7]	—	—	0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. The RGMII specification requires that PC board designer add 1.5 ns or greater in trace delay to the RX_CLK in order to meet this specification. However, as stated above, this device will function with only 1.0 ns of delay.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by characterization.
6. Guaranteed by design.
7. Signal timings are measured at 0.5 V and 2.0 V voltage levels.

Figure 19 through Figure 24 show the local bus signals.

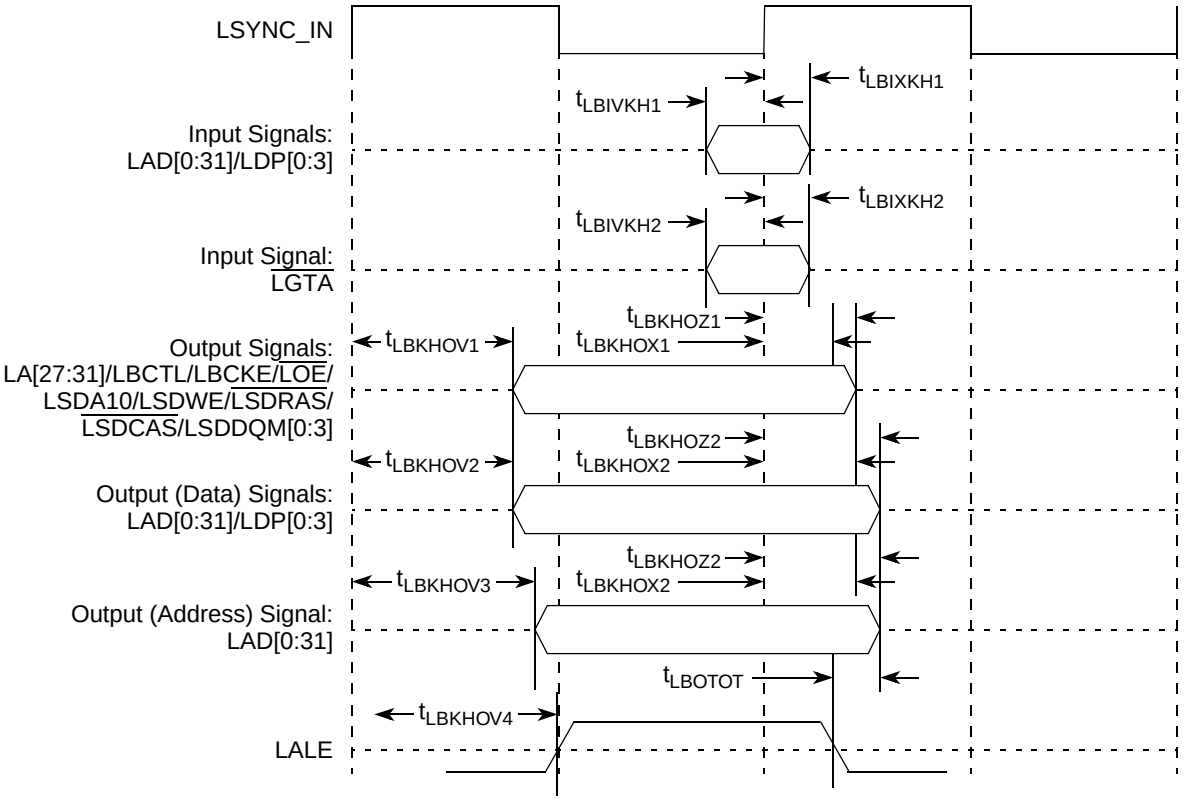


Figure 19. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

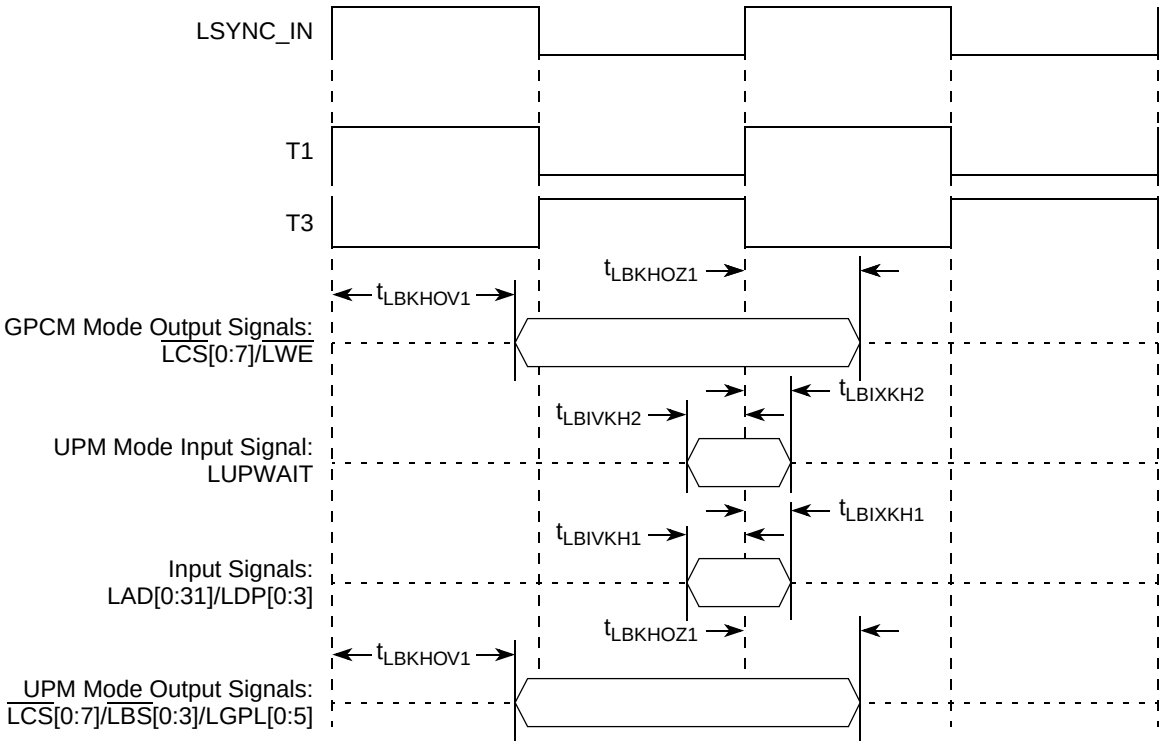


Figure 21. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

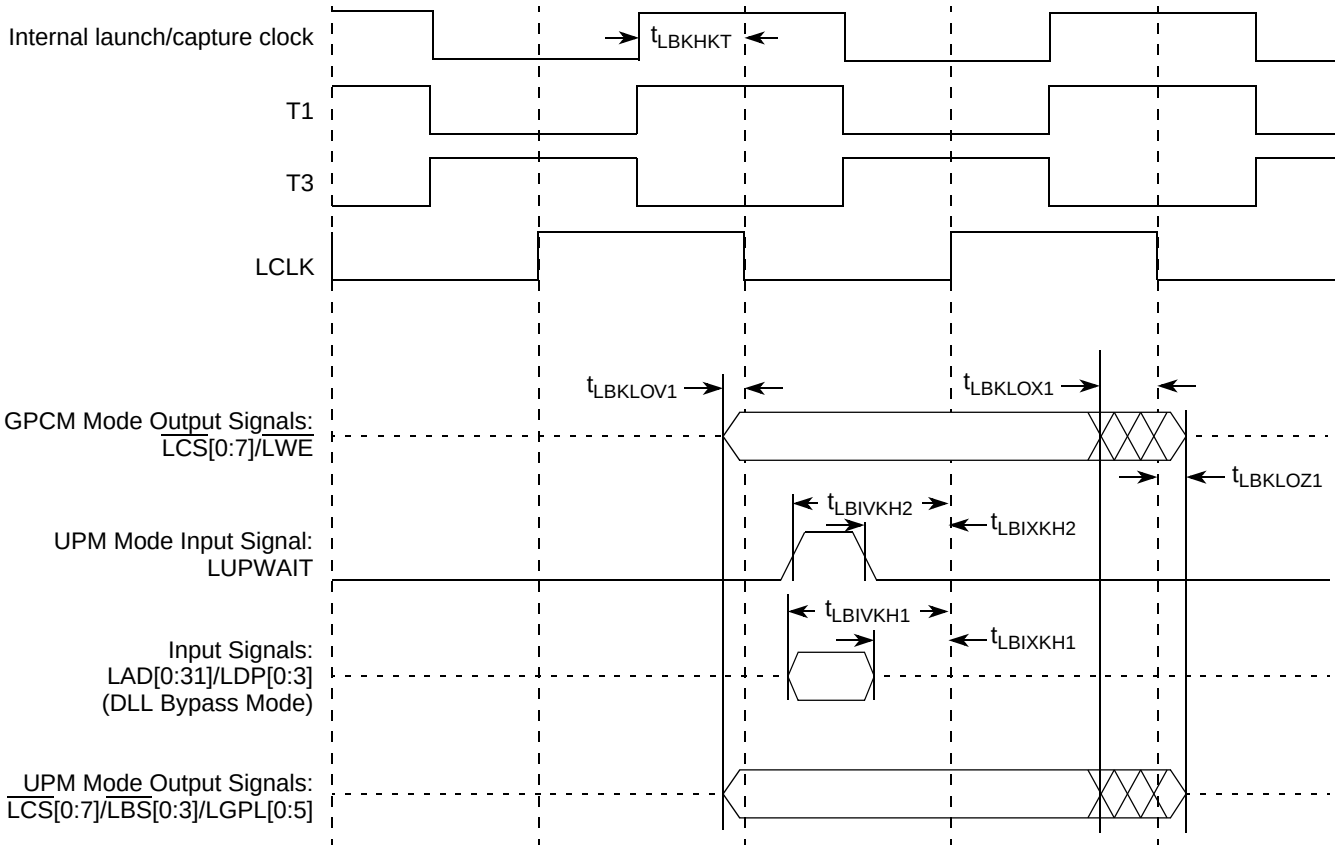


Figure 22. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

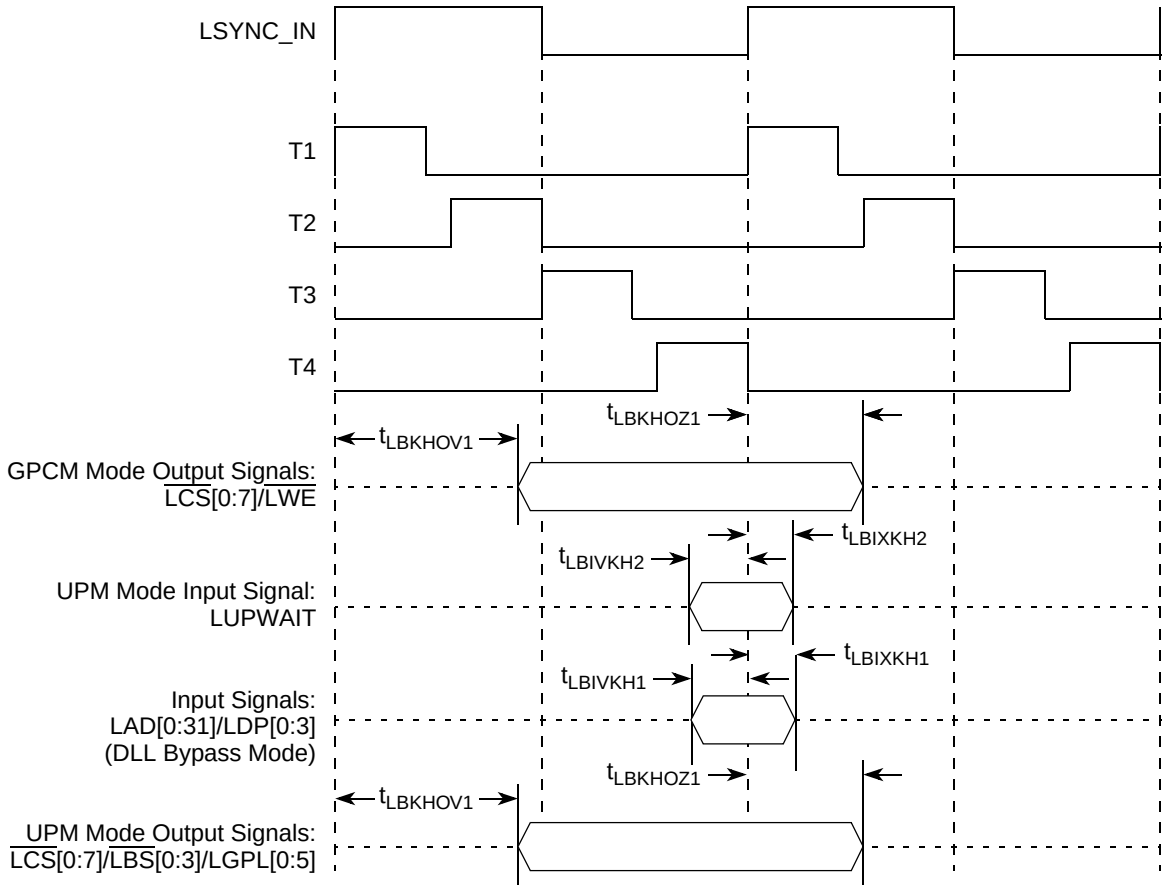


Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Enabled)

Figure 31 shows the AC timing diagram for the I^2C bus.

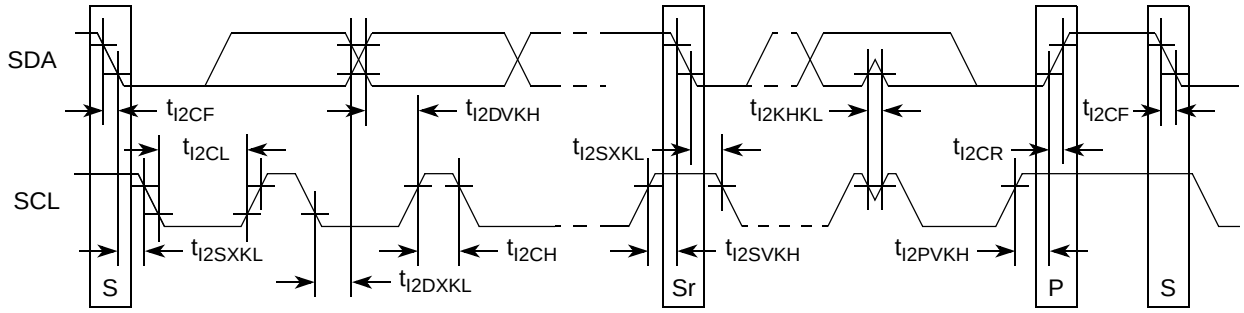


Figure 31. I^2C Bus AC Timing Diagram

12 PCI/PCI-X

This section describes the DC and AC electrical specifications for the PCI/PCI-X bus of the MPC8540.

12.1 PCI/PCI-X DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the PCI/PCI-X interface of the MPC8540.

Table 41. PCI/PCI-X DC Electrical Characteristics [1]

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [2] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Notes:

1.Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.

2.Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

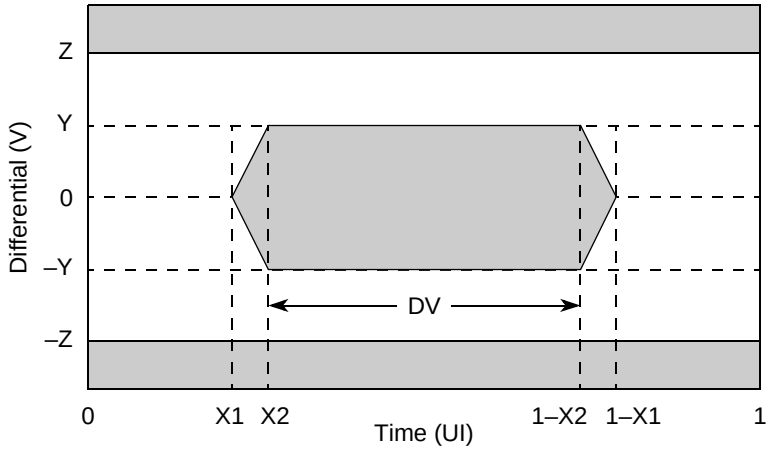


Figure 37. Example Compliance Mask

Y = minimum data valid amplitude

Z = maximum amplitude

1 UI = 1 unit interval = 1/baud rate

X1 = end of zero crossing region

X2 = beginning of data valid window

DV = data valid window = 1 – 2 × X2

The waveform of the signal under test must fall within the unshaded area of the mask to be compliant. Different masks are used for the driver output and the receiver input allowing each to be separately specified.

13.3.1 RapidIO Driver AC Timing Specifications

Driver AC timing specifications are provided in Table 47, Table 48, and Table 49. A driver shall comply with the specifications for each data rate/frequency for which operation of the driver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The output of a driver shall be connected to a 100 Ω, ±1%, differential (bridged) resistive load.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7]).

Table 47. RapidIO Driver AC Timing Specifications—500 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential output high voltage	V_{OHD}	200	540	mV	1
Differential output low voltage	V_{OLD}	–540	–200	mV	1

14.2 Mechanical Dimensions of the MPC8540 FC-PBGA

Figure 44 the mechanical dimensions and bottom surface nomenclature of the MPC8540, 783 FC-PBGA package.

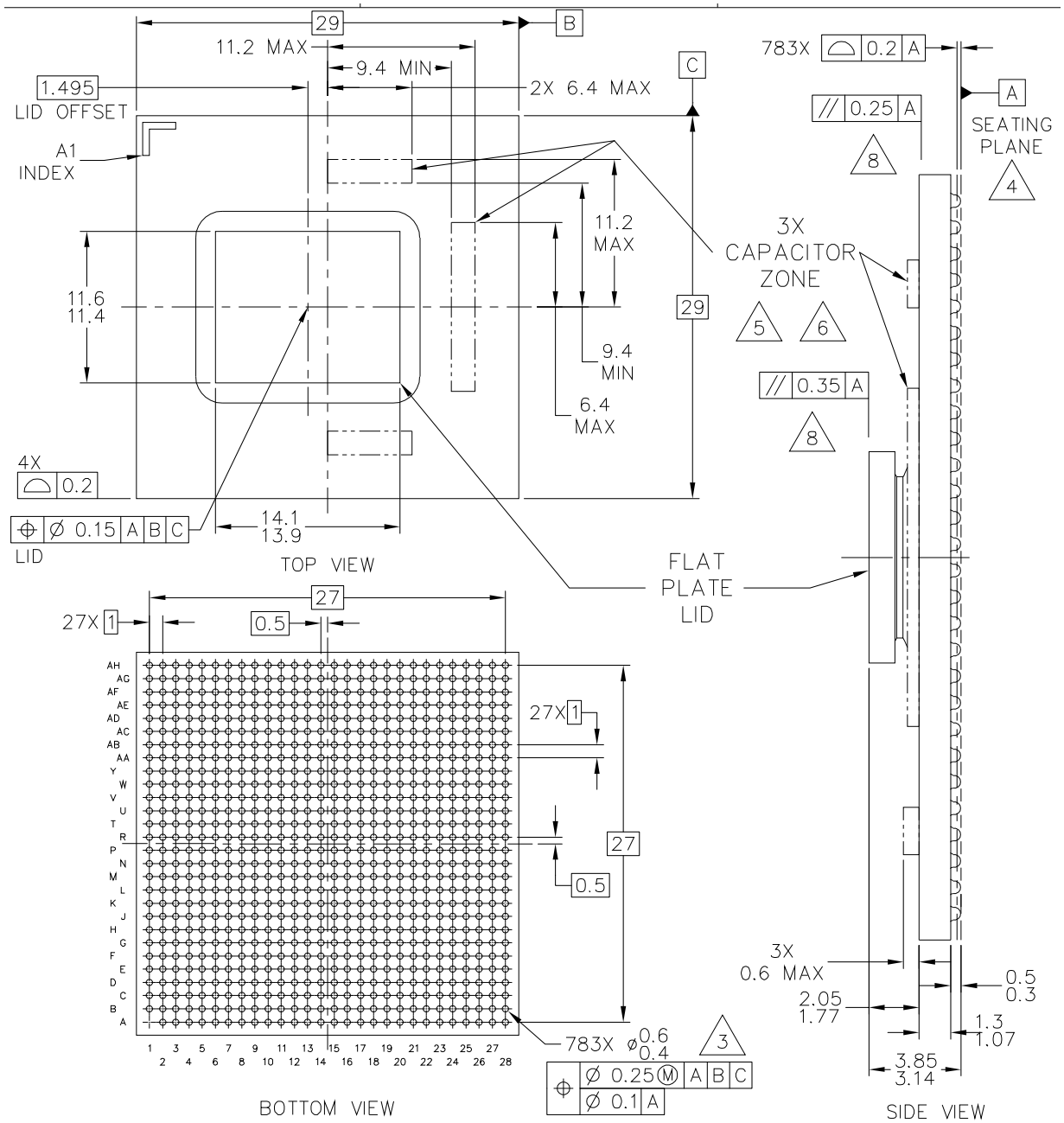


Figure 44. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8540 FC-PBGA

NOTES

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.

3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
7. The socket lid must always be oriented to A1.

14.3 Pinout Listings

Table 53 provides the pin-out listing for the MPC8540, 783 FC-PBGA package.

Table 53. MPC8540 Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI/PCI-X				
PCI_AD[63:0]	AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14, V15, W15, Y15, AA15, AB15, AC15, AD15, AG15, AH15, V16, W16, AB16, AC16, AD16, AE16, AF16, V17, W17, Y17, AA17, AB17, AE17, AF17, AF18, AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9, AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11, AG11, AH11, V12, W12, Y12, AB12, AD12, AE12, AG12, AH12, V13, Y13, AB13, AC13	I/O	OV_{DD}	17
PCI_C_$\overline{BE}$[7:0]	AG13, AH13, V14, W14, AH8, AB10, AD11, AC12	I/O	OV_{DD}	17
PCI_PAR	AA11	I/O	OV_{DD}	
PCI_PAR64	Y14	I/O	OV_{DD}	
$\overline{\text{PCI\_FRAME}}$	AC10	I/O	OV_{DD}	2
$\overline{\text{PCI\_TRDY}}$	AG10	I/O	OV_{DD}	2
$\overline{\text{PCI\_IRDY}}$	AD10	I/O	OV_{DD}	2
$\overline{\text{PCI\_STOP}}$	V11	I/O	OV_{DD}	2
$\overline{\text{PCI\_DEVSEL}}$	AH10	I/O	OV_{DD}	2
PCI_IDSEL	AA9	I	OV_{DD}	
$\overline{\text{PCI\_REQ64}}$	AE13	I/O	OV_{DD}	5, 10
$\overline{\text{PCI\_ACK64}}$	AD13	I/O	OV_{DD}	2
$\overline{\text{PCI\_PERR}}$	W11	I/O	OV_{DD}	2
$\overline{\text{PCI\_SERR}}$	Y11	I/O	OV_{DD}	2, 4
$\overline{\text{PCI\_REQ0}}$	AF5	I/O	OV_{DD}	
$\overline{\text{PCI\_REQ}}$[1:4]	AF3, AE4, AG4, AE5	I	OV_{DD}	
$\overline{\text{PCI\_GNT}}$[0]	AE6	I/O	OV_{DD}	
$\overline{\text{PCI\_GNT}}$[1:4]	AG5, AH5, AF6, AG6	O	OV_{DD}	5, 9

Table 59. Package Thermal Characteristics (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-case thermal	$R_{\theta JC}$	0.8	•C/W	4

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-6 with the board horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). Cold plate temperature is used for case temperature; measured value includes the thermal resistance of the interface layer.

16.2 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 45. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force.

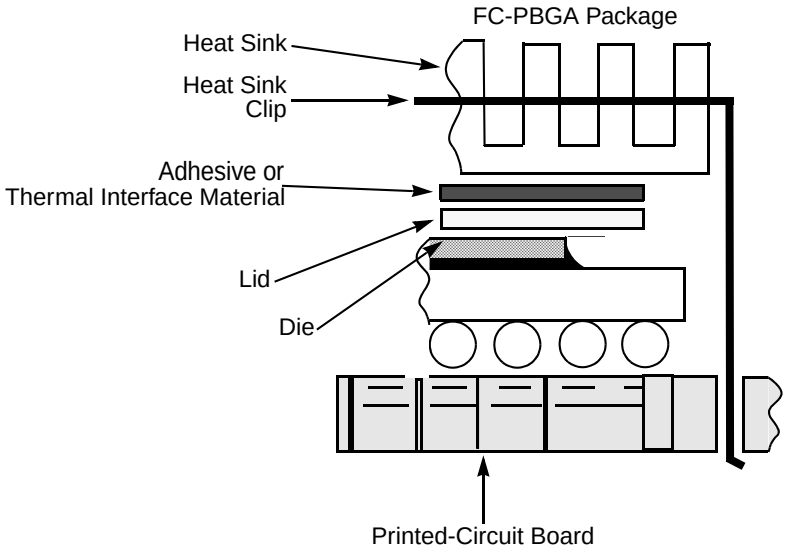


Figure 45. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the MPC8540. There are several commercially-available heat sinks from the following vendors:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Conductivity	Value	Unit
Lid (12 × 14 × 1 mm)		
k_x	360	W/(m × K)
k_y	360	
k_z	360	
Lid Adhesive—Collapsed resistance (10 × 12 × 0.050 mm)		
k_x	1	
k_y	1	
k_z	1	
Die (10 × 12 × 0.76 mm)		
Bump/Underfill—Collapsed resistance (10 × 12 × 0.070 mm)		
k_x	0.6	
k_y	0.6	
k_z	1.9	
Substrate and Solder Balls (29 × 29 × 1.47 mm)		
k_x	10.2	
k_y	10.2	
k_z	1.6	

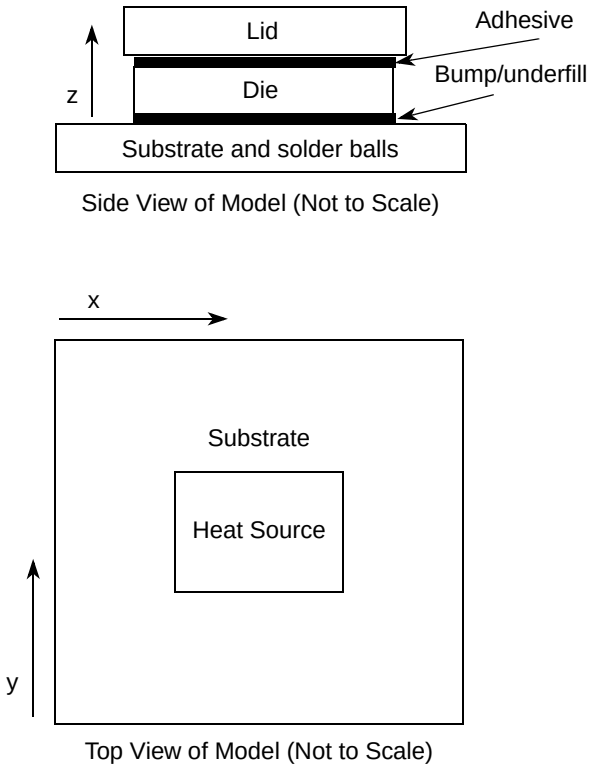


Figure 46. MPC8540 Thermal Model

16.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in Table 59, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

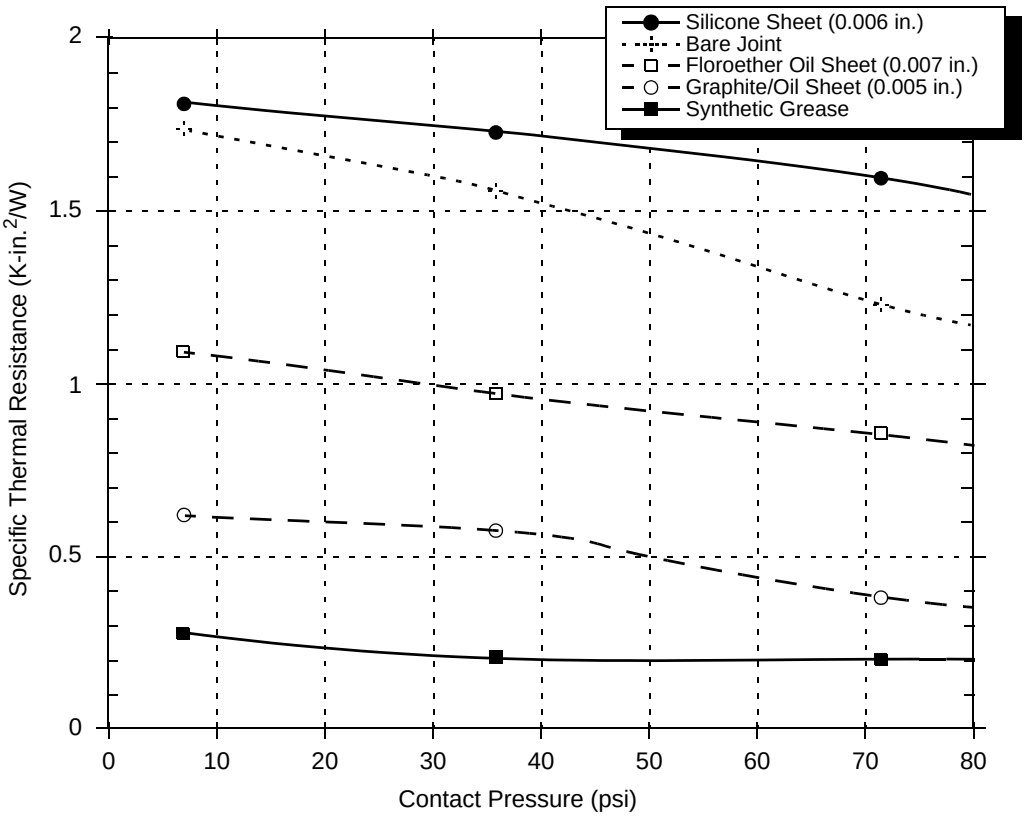


Figure 48. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

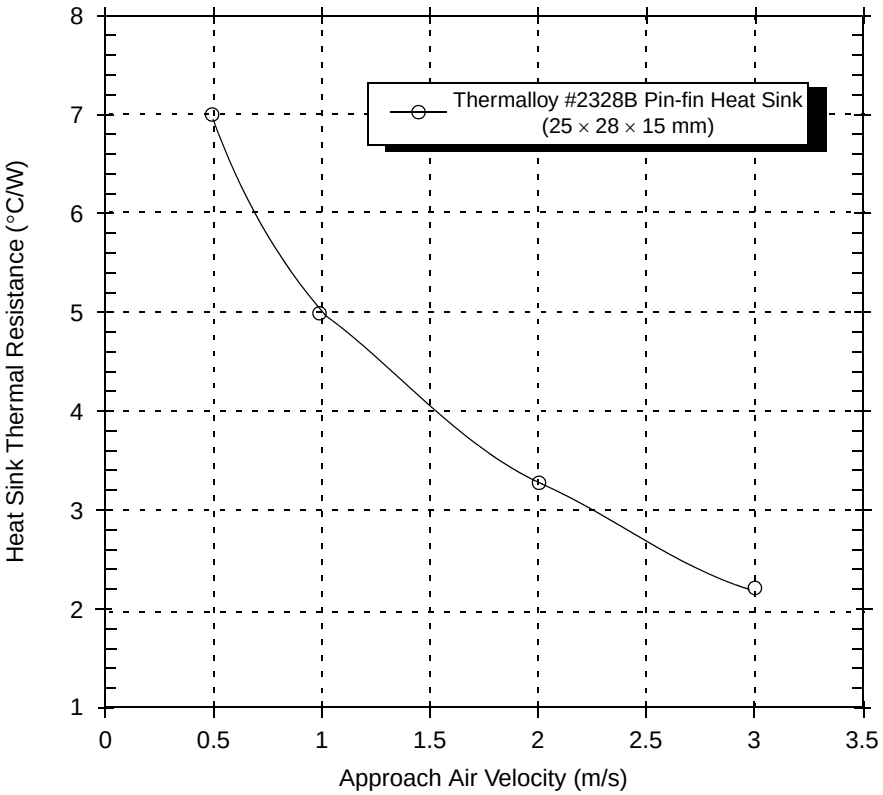


Figure 49. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

16.2.4.2 Case 2

Every system application has different conditions that the thermal management solution must solve. As an alternate example, assume that the air reaching the component is 85 C with an approach velocity of 1 m/sec. For a maximum junction temperature of 105 C at 7 W, the total thermal resistance of junction to case thermal resistance plus thermal interface material plus heat sink thermal resistance must be less than 2.8 C/W. The value of the junction to case thermal resistance in Table 59 includes the thermal interface resistance of a thin layer of thermal grease as documented in footnote 4 of the table. Assuming that the heat sink is flat enough to allow a thin layer of grease or phase change material, then the heat sink must be less than 2 C/W.

Millennium Electronics (MEI) has tooled a heat sink MTHERM-1051 for this requirement assuming a compactPCI environment at 1 m/sec and a heat sink height of 12 mm. The MEI solution is illustrated in Figure 50 and Figure 51. This design has several significant advantages:

- The heat sink is clipped to a plastic frame attached to the application board with screws or plastic inserts at the corners away from the primary signal routing areas.
- The heat sink clip is designed to apply the force holding the heat sink in place directly above the die at a maximum force of less than 10 lbs.
- For applications with significant vibration requirements, silicone damping material can be applied between the heat sink and plastic frame.

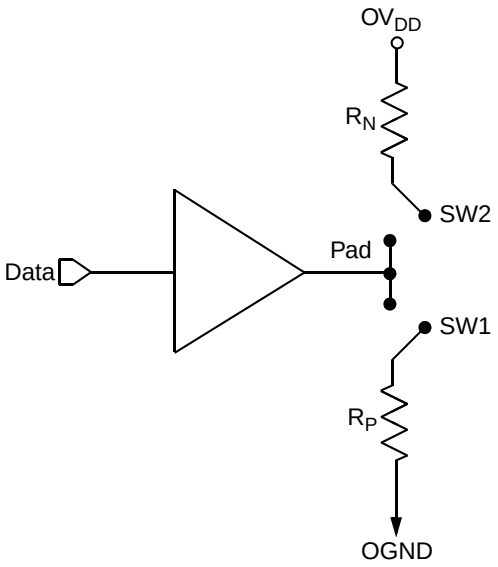


Figure 53. Driver Impedance Measurement

The output impedance of the RapidIO port drivers targets 200-Ω differential resistance. The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 60 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 60. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI/PCI-X	DDR DRAM	RapidIO	Symbol	Unit
R_N	43 Target	25 Target	20 Target	NA	Z_0	W
R_P	43 Target	25 Target	20 Target	NA	Z_0	W
Differential	NA	NA	NA	200 Target	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

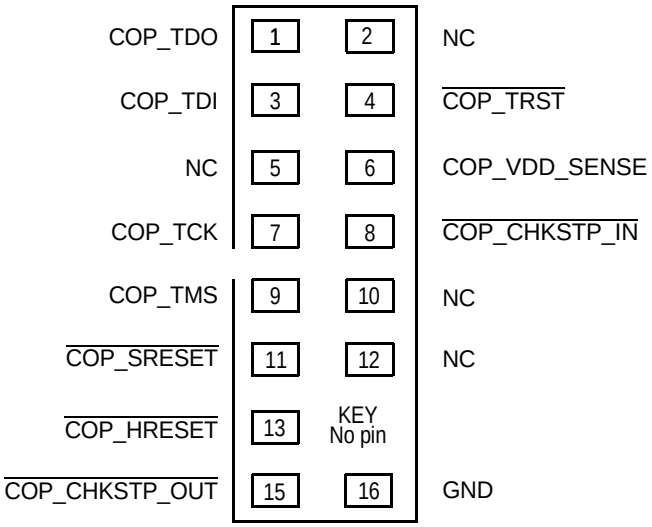


Figure 54. COP Connector Physical Pinout

17.8.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 55. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 kΩ resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

Table 61. Document Revision History (continued)

Rev. No.	Substantive Change(s)
2.0	Section 1.1—Updated features list to coincide with latest version of the reference manual Table 1 and Table 2—Addition of SYSCLK to OV_{IN} Table 2—Addition of notes 1 and 2 Table 3—Addition of note 1 Table 5—New Section 4—New Table 13—Addition of I_{VREF} Removed Figure 4 DDR SRAM Input TIming Diagram Table 15—Modified maximum values for t_{DISKEW} Table 16—Added MSYNC_OUT to tMCKSKEW2 Figure 5—New Section 6.2.1—Removed Figure 4, “DDR SDRAM Input Timing Diagram” Section 8.1—Removed references to 2.5 V from first paragraph Figure 8—New Table 21 and Table 22—Modified “conditions” for I_{IH} and I_{IL} Table 23—Addition of min and max for GTX_CLK125 reference clock duty cycle Table 27 —Addition of min and max for GTX_CLK125 reference clock duty cycle Table 29—Addition of min and max for GTX_CLK125 reference clock duty cycle Table 30—VOH min and conditions; I_{IH} and I_{IL} conditions Table 31—Min and max for t_{MTXR} and t_{MTXF} Table 32—Min and max for t_{MRXR} and t_{MRXF} Figure 23 and Figure 24—Changed LSYNC_IN to Internal clock at top of each figure Figure 18—New Figure 18—New Table 36—Removed row for tLBKHOX3 Table 43—New (AC timing of PCI-X at 66 MHz) Table 53—Addition of note 19 Figure 55—Addition of jumper and note at top of diagram Table 55: Changed max bus freq for 667 core to 166 Section 16.2.1—Modified first paragraph Figure 46—Modified Figure 47—New Table 59—Modified thermal resistance data Section 16.2.4.2—Modified first and second paragraphs