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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1), 10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8540pxaqfb

1 Overview

The following section provides a high-level overview of the MPC8540 features. Figure 1 shows the major functional units within the MPC8540.

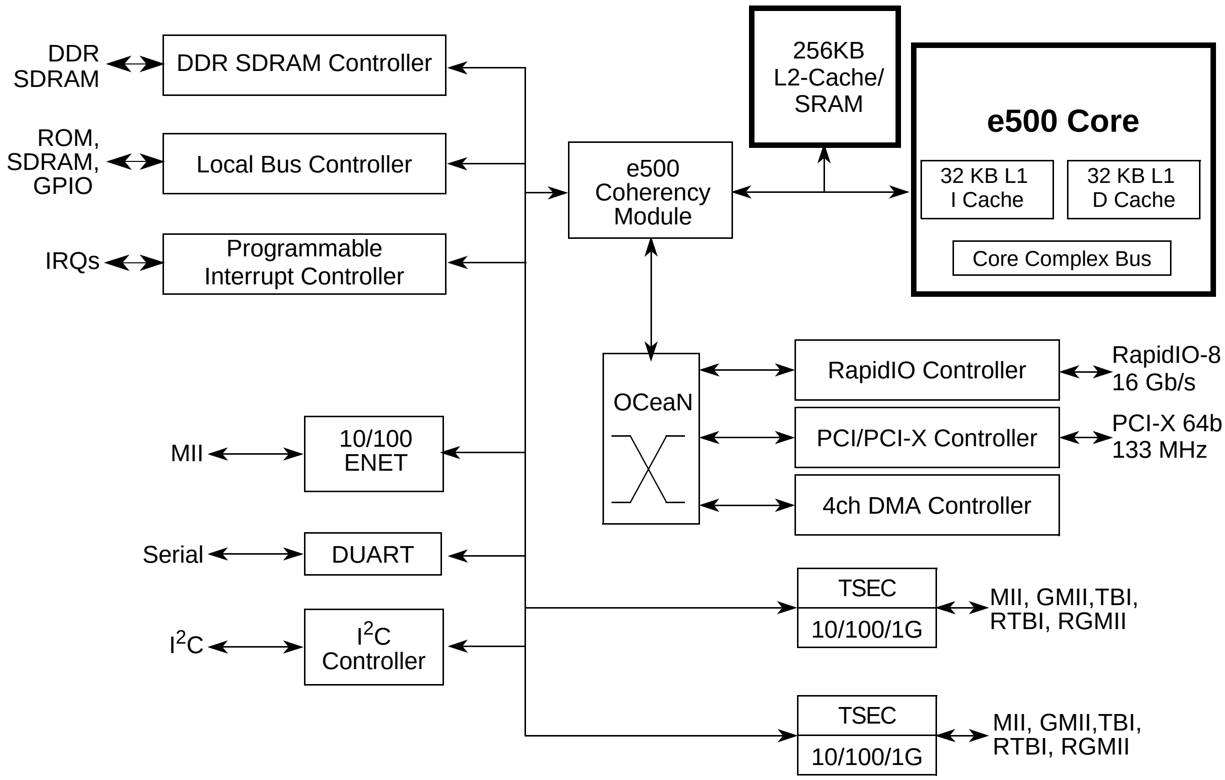


Figure 1. MPC8540 Block Diagram

1.1 Key Features

The following lists an overview of the MPC8540 feature set.

- High-performance, 32-bit Book E–enhanced core that implements the Power Architecture
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis. Separate locking for instructions and data
  - Memory management unit (MMU) especially designed for embedded applications
  - Enhanced hardware and software debug support
  - Performance monitor facility (similar to but different from the MPC8540 performance monitor described in Chapter 18, "Performance Monitor."

- 256 Kbyte L2 cache/SRAM
  - Can be configured as follows
    - Full cache mode (256-Kbyte cache).
    - Full memory-mapped SRAM mode (256-Kbyte SRAM mapped as a single 256-Kbyte block or two 128-Kbyte blocks)
    - Half SRAM and half cache mode (128-Kbyte cache and 128-Kbyte memory-mapped SRAM)
  - Full ECC support on 64-bit boundary in both cache and SRAM modes
  - Cache mode supports instruction caching, data caching, or both
  - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing)
  - Eight-way set-associative cache organization (1024 sets of 32-byte cache lines)
  - Supports locking the entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions
  - Global locking and flash clearing done through writes to L2 configuration registers
  - Instruction and data locks can be flash cleared separately
  - Read and write buffering for internal bus accesses
  - SRAM features include the following:
    - I/O devices access SRAM regions by marking transactions as snoopable (global)
    - Regions can reside at any aligned location in the memory map
    - Byte accessible ECC is protected using read-modify-write transactions accesses for smaller than cache-line accesses.
- Address translation and mapping unit (ATMU)
  - Eight local access windows define mapping within local 32-bit address space
  - Inbound and outbound ATMUs map to larger external address spaces
    - Three inbound windows plus a configuration window on PCI/PCI-X
    - Four inbound windows plus a default and configuration window on RapidIO
    - Four outbound windows plus default translation for PCI
    - Eight outbound windows plus default translation for RapidIO
- DDR memory controller
  - Programmable timing supporting DDR-1 SDRAM
  - 64-bit data interface, up to 333-MHz data rate
  - Four banks of memory supported, each up to 1 Gbyte
  - DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
  - Full ECC support
  - Page mode support (up to 16 simultaneous open pages)
  - Contiguous or discontiguous memory mapping

- Power management
  - Fully static 1.2-V CMOS design with 3.3- and 2.5-V I/O
  - Supports power saving modes: doze, nap, and sleep
  - Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle.
- System performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the 8 counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- System access port
  - Uses JTAG interface and a TAP controller to access entire system memory map
  - Supports 32-bit accesses to configuration registers
  - Supports cache-line burst accesses to main memory
  - Supports large block (4-Kbyte) uploads and downloads
  - Supports continuous bit streaming of entire block for fast upload and download
- IEEE 1149.1-compliant, JTAG boundary scan
- 783 FC-PBGA package

2 Electrical Characteristics

This section provides the electrical specifications and thermal characteristics for the MPC8540. The MPC8540 is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

Table 13. DDR SDRAM DC Electrical Characteristics (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
MV_{REF} input leakage current	I_{VREF}	—	100	μA	

Notes:

1.GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.

2.MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.

3.V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

4.V_{IH} can tolerate an overshoot of 1.2V over GV_{DD} for a pulse width of ≤3 ns, and the pulse width cannot be greater than t_{MCK}. V_{IL} can tolerate an undershoot of 1.2V below GND for a pulse width of ≤3 ns, and the pulse width cannot be greater than t_{MCK}.

5.Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 14 provides the DDR capacitance.

Table 14. DDR SDRAM Capacitance

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, MSYNC_IN	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

1.This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak to peak) = 0.2 V.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 15 provides the input AC timing specifications for the DDR SDRAM interface.

Table 15. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	
AC input high voltage	V_{IH}	MV_{REF} + 0.31	GV_{DD} + 0.3	V	
MDQS—MDQ/MECC input skew per byte For DDR = 333 MHz For DDR ≤ 266 MHz	t_{DISKEW}	 -750 -1125	 750 1125	ps	1, 2

Note:

1.Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 ≤ n ≤ 7) or ECC (MECC[{0...7}] if n=8).

2.For timing budget analysis, the MPC8540 consumes ±550 ps of the total budget.

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8540.

7.1 DUART DC Electrical Characteristics

Table 19 provides the DC electrical characteristics for the DUART interface of the MPC8540.

Table 19. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:

1.Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 20 provides the AC timing parameters for the DUART interface of the MPC8540.

Table 20. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{CCB_CLK} / 1048576	baud	3
Maximum baud rate	f_{CCB_CLK} / 16	baud	1, 3
Oversample rate	16	—	2, 3

Notes:

1.Actual attainable baud rate will be limited by the latency of interrupt processing.

2.The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

3.Guaranteed by design.

Figure 19 through Figure 24 show the local bus signals.

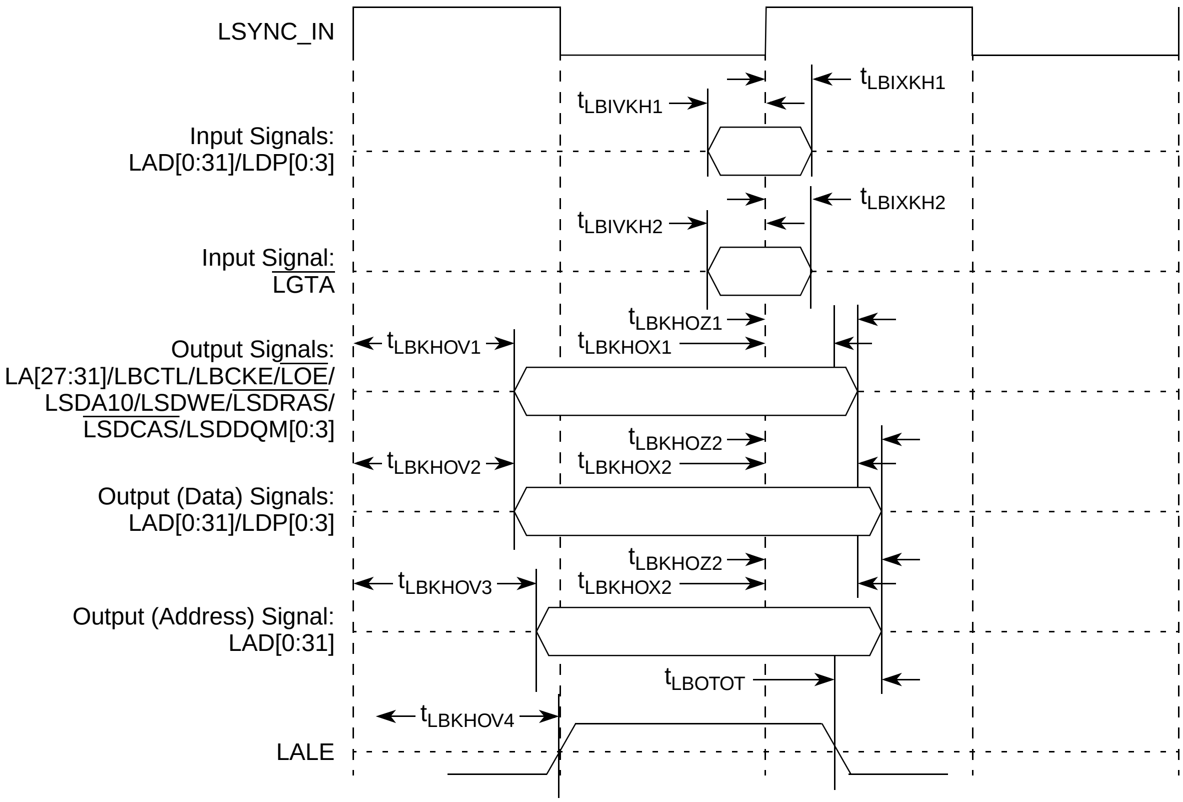


Figure 19. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

Figure 29 provides the test access port timing diagram.

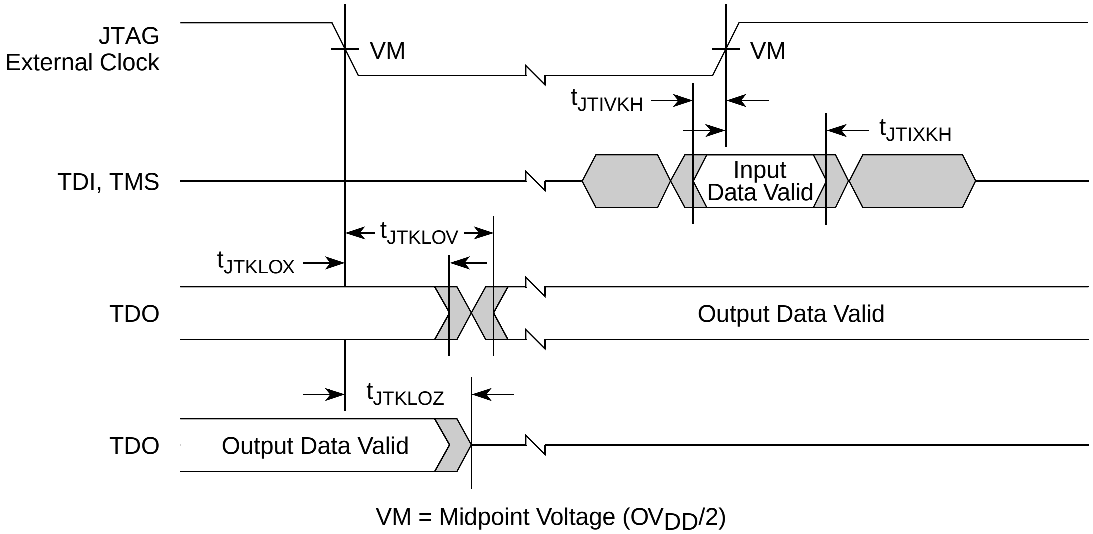


Figure 29. Test Access Port Timing Diagram

11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8540.

11.1 I²C DC Electrical Characteristics

Table 39 provides the DC electrical characteristics for the I²C interface of the MPC8540.

Table 39. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	0.7 × OV_{DD}	OV_{DD}+ 0.3	V	
Input low voltage level	V_{IL}	–0.3	0.3 × OV_{DD}	V	
Low level output voltage	V_{OL}	0	0.2 × OV_{DD}	V	1
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between 0.1 × OV_{DD} and 0.9 × OV_{DD}(max)	I_I	–10	10	μA	3
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8540 Integrated Processor Preliminary Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

Table 45. RapidIO 8/16 LP-LVDS Driver DC Electrical Characteristics (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Characteristic	Symbol	Min	Max	Unit	Notes
Common mode offset voltage	ΔV_{OSCM}	—	50	mV	1, 6
Differential termination	R_{TERM}	90	220	W	
Short circuit current (either output)	$\|I_{SS}\|$	—	24	mA	7
Bridged short circuit current	$\|I_{SB}\|$	—	12	mA	8

Notes:
1. Bridged 100-Ω load.
2. See Figure 35(a).
3. Differential offset voltage = $|V_{OHD}+V_{OLD}|$. See Figure 35(b).
4. $V_{OHCM} = (V_{OA} + V_{OB})/2$ when measuring V_{OHD}.
5. $V_{OLCM} = (V_{OA} + V_{OB})/2$ when measuring V_{OLD}.
6. Common mode offset $\Delta V_{OSCM} = |V_{OHCM} - V_{OLCM}|$. See Figure 35(c).
7. Outputs shorted to V_{DD} or GND.
8. Outputs shorted together.

Table 46. RapidIO 8/16 LP-LVDS Receiver DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit	Notes
Voltage at either input	V_I	0	2.4	V	
Differential input high voltage	V_{IHD}	100	600	mV	1
Differential input low voltage	V_{ILD}	–600	–100	mV	1
Common mode input range (referenced to receiver ground)	V_{ICM}	0.050	2.350	V	2
Input differential resistance	R_{IN}	90	110	W	

Notes:
1. Over the common mode range.
2. Limited by V_I. See Figure 42.

13.3.2 RapidIO Receiver AC Timing Specifications

The RapidIO receiver AC timing specifications are provided in Table 50. A receiver shall comply with the specifications for each data rate/frequency for which operation of the receiver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The specifications apply over the receiver common mode and differential input voltage ranges.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7])

Table 50. RapidIO Receiver AC Timing Specifications—500 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1, 5
Data valid	DV	1080		ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}	—	380	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–300	300	ps	4

Notes:
1.Measured at V_{ID} = 0 V.
2.Measured using the RapidIO receive mask shown in Figure 40.
3.See Figure 43.
4.See Figure 42 and Figure 43.
5.Guaranteed by design.

Table 51. RapidIO Receiver AC Timing Specifications—750 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1, 5
Data valid	DV	600	—	ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}	—	400	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–267	267	ps	4

Notes:
1.Measured at V_{ID} = 0 V.
2.Measured using the RapidIO receive mask shown in Figure 40.
3.See Figure 43.
4.See Figure 42 and Figure 43.
5.Guaranteed by design.

enough that increasing the length of the sequence does not cause the resulting eye pattern to change from one that complies with the RapidIO receive mask to one that does not comply with the mask. The data carried by any given data signal in the interface may not be correlated with the data carried by any other data signal in the interface. The zero-crossings of the clock associated with a data signal shall be used as the timing reference for aligning the multiple recordings of the data signal when the recordings are overlaid.

While the method used to make the recordings and overlay them to form the eye pattern is not specified, the method used shall be demonstrably equivalent to the following method. The signal under test is repeatedly recorded with a digital oscilloscope in infinite persistence mode. Each recording is triggered by a zero-crossing of the clock associated with the data signal under test. Roughly half of the recordings are triggered by positive-going clock zero-crossings and roughly half are triggered by negative-going clock zero-crossings. Each recording is at least 1.9 UI in length (to ensure that at least one complete eye is formed) and begins 0.5 UI before the trigger point (0.5 UI before the associated clock zero-crossing). Depending on the length of the individual recordings used to generate the eye pattern, one or more complete eyes will be formed. Regardless of the number of eyes, the eye whose center is immediately to the right of the trigger point is the eye used for compliance testing.

An example of an eye pattern generated using the above method with recordings 3 UI in length is shown in Figure 41. In this example, there is no skew between the signal under test and the associated clock used to trigger the recordings. If skew was present, the eye pattern would be shifted to the left or right relative to the oscilloscope trigger point.

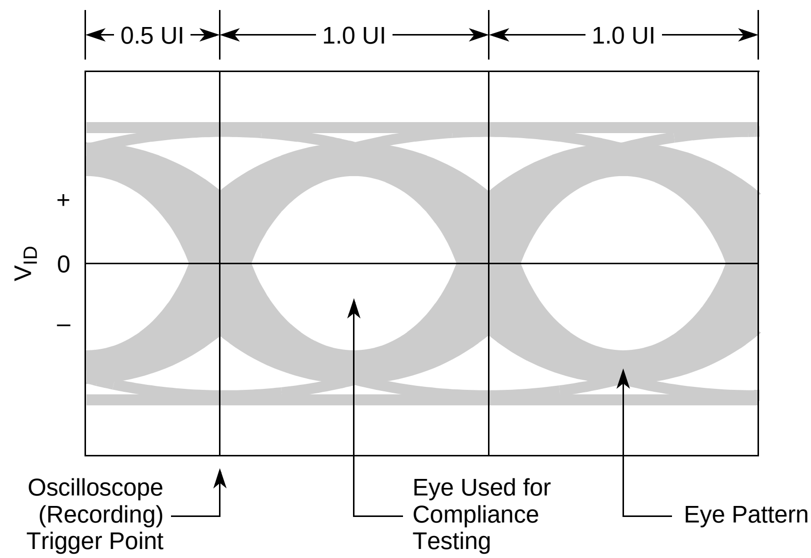


Figure 41. Example Receiver Input Eye Pattern

14.2 Mechanical Dimensions of the MPC8540 FC-PBGA

Figure 44 the mechanical dimensions and bottom surface nomenclature of the MPC8540, 783 FC-PBGA package.

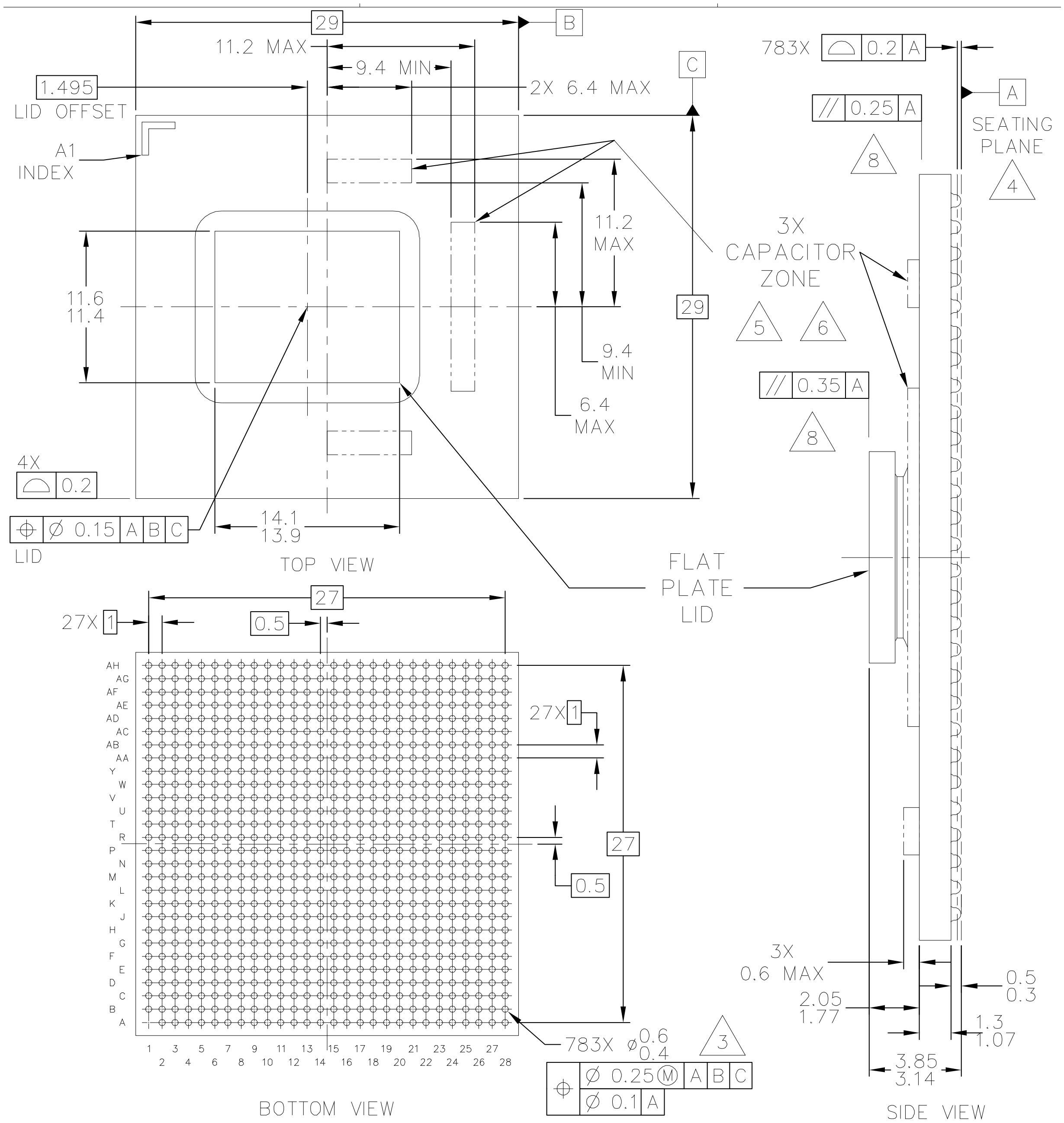


Figure 44. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8540 FC-PBGA

NOTES

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.

Table 53. MPC8540 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Power Management				
ASLEEP	AG18	I/O		9, 19
Power and Ground Signals				
$AV_{DD}1$	AH19	Power for e500 PLL (1.2 V)	$AV_{DD}1$	
$AV_{DD}2$	AH18	Power for CCB PLL (1.2 V)	$AV_{DD}2$	
GND	A12, A17, B3, B14, B20, B26, B27, C2, C4, C11,C17, C19, C22, C27, D8, E3, E12, E24, F11, F18, F23, G9, G12, G25, H4, H12, H14, H17, H20, H22, H27, J19, J24, K5, K9, K18, K23, K28, L6, L20, L25, M4, M12, M14, M16, M22, M27, N2, N13, N15, N17, P12, P14, P16, P23, R13, R15, R17, R20, R26, T3, T8, T10, T12, T14, T16, U6, U13, U15, U16, U17, U21, V7, V10, V26, W5, W18, W23, Y8, Y16, AA6, AA13, AB4, AB11, AB19, AC6, AC9, AD3, AD8, AD17, AF2, AF4, AF10, AF13, AF15, AF27, AG3, AG7, AG26	—	—	
GV_{DD}	A14, A20, A25, A26, A27, A28, B17, B22, B28, C12, C28, D16, D19, D21, D24, D28, E17, E22, F12, F15, F19, F25, G13, G18, G20, G23, G28, H19, H24, J12, J17, J22, J27, K15, K20, K25, L13, L23, L28, M25, N21	Power for DDR DRAM I/O Voltage (2.5 V)	GV_{DD}	
LV_{DD}	A4, C5, E7, H10	Reference Voltage; Three-Speed Ethernet I/O (2.5 V, 3.3 V)	LV_{DD}	
MV_{REF}	N27	Reference Voltage Signal; DDR	MV_{REF}	
No Connects	AH26, AH27, AH28, AG28, AF28, AE28, AH1, AG1, AH2, B1, B2, A2, A3, AH25, H1, H2, J1, J2, J3, J4, J5, J6, J7, J8, K8, K7, K6, K3, K2, K1, L1, L2, L3, L4, L5, L8, L9, L10, L11, M10, M9, M8, M7, M6, M3, M2, P7, P6, P5, P4, P3, P2, P1, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, T9, T6, T5, T4, T1, U1, U2, U3, U4, U8, U10, V5, V4, V3, V2, V1, W1, W2, W3, W6, W7, W8, W9, Y1, Y2, Y3, Y4, Y5, Y6, Y9, AA8, AA7, AA4, AA3, AA2, AA1, AB1, AB2, AB3, AB5, AB6, AC7, AC4, AC3, AC2, AC1	—	—	16
OV_{DD}	D1, E4, H3, K4, K10, L7, M5, N3, P22, R19, R25, T2, T7, U5, U20, U26, V8, W4, W13, W19, W21, Y7, Y23, AA5, AA12, AA16, AA20, AB7, AB9, AB26, AC5, AC11, AC17, AD4, AE1, AE8, AE10, AE15, AF7, AF12, AG27, AH4	PCI/PCI-X, RapidIO, 10/100 Ethernet, and other Standard (3.3 V)	OV_{DD}	

Table 53. MPC8540 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
RESERVED	C1, T11, U11, AF1	—	—	15
SENSEVDD	L12	Power for Core (1.2 V)	V_{DD}	13
SENSEVSS	K12	—	—	13
V_{DD}	M13, M15, M17, N14, N16, P13, P15, P17, R12, R14, R16, T13, T15, T17, U12, U14, AH17	Power for Core (1.2 V)	V_{DD}	

Notes:

1.All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5}}$/$\overline{\text{DMA\_REQ2}}$ is listed only once in the Local Bus Controller Interface section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA\_REQ2}}$.

2.Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.

3.This pin must always be tied to GND. .

4.This pin is an open drain signal.

5.This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the MPC8540 is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. If an external device connected to this pin might pull it down during reset, then a pull-up or active driver is needed if the signal is intended to be high during reset.

6.Treat these pins as no connects (NC) unless using debug address functionality.

7.The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 15.2, “Platform/System PLL Ratio.”

8.The value of LALE and LGPL2 at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 15.3, “e500 Core PLL Ratio.”

9.Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.

10.This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. Refer to the *PCI Specification*.

11.This output is actively driven during reset rather than being three-stated during reset.

12.These JTAG pins have weak internal pull-up P-FETs that are always enabled.

13.These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.

14.Internal thermally sensitive resistor.

15.No connections should be made to these pins.

16.These pins are not connected for any functional use.

17.PCI specifications recommend that a weak pull-up resistor (2–10 kΩ) be placed on the higher order pins to OV_{DD} when using 64-bit buffer mode (pins PCI_AD[63:32] and PCI_C_BE[7:4]).

18.Note that these signals are POR configurations for Rev. 1.x and notes 5 and 9 apply to these signals in Rev. 1.x but not in later revisions.

19 If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a logic –1 state during reset.

20.Recommend a pull-up resistor (~1 KΩ) b placed on this pin to OV_{DD}.

21.These are test signals for factory use only and must be pulled up (100 Ω - 1 kΩ) to OVDD for normal machine operation.

22.If this signal is used as both an input and an output, a weak pull-up (~10 kΩ) is required on this pin.

Table 59. Package Thermal Characteristics (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-case thermal	$R_{\theta JC}$	0.8	•C/W	4

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-6 with the board horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). Cold plate temperature is used for case temperature; measured value includes the thermal resistance of the interface layer.

16.2 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 45. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force.

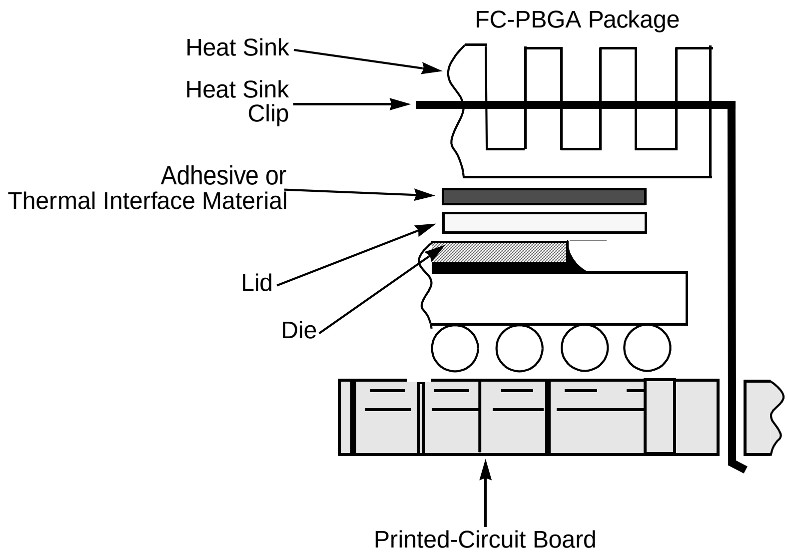


Figure 45. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the MPC8540. There are several commercially-available heat sinks from the following vendors:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-millennium.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the MPC8540 to function in various environments.

16.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8540 thermal model is shown in Figure 46. Five cuboids are used to represent this device. To simplify the model, the solder balls and substrate are modeled as a single block 29x29x1.47 mm with the conductivity adjusted accordingly. For modeling, the planar dimensions of the die are rounded to the nearest mm, so the die is modeled as 10x12 mm at a thickness of 0.76 mm. The bump/underfill layer is modeled as a collapsed resistance between the die and substrate assuming a conductivity of 0.6 in-plane and 1.9 W/m•K in the thickness dimension of 0.76 mm. The lid attach adhesive is also modeled as a collapsed resistance with dimensions of 10x12x0.050 mm and the conductivity of 1 W/m•K. The nickel plated copper lid is modeled as 12x14x1 mm. Note that the die and lid are not centered on the substrate; there is a 1.5 mm offset documented in the case outline drawing in Figure 44.

Conductivity	Value	Unit
Lid (12 × 14 × 1 mm)		
k_x	360	W/(m × K)
k_y	360	
k_z	360	
Lid Adhesive—Collapsed resistance (10 × 12 × 0.050 mm)		
k_x	1	
k_y	1	
k_z	1	
Die (10 × 12 × 0.76 mm)		
Bump/Underfill—Collapsed resistance (10 × 12 × 0.070 mm)		
k_x	0.6	
k_y	0.6	
k_z	1.9	
Substrate and Solder Balls (29 × 29 × 1.47 mm)		
k_x	10.2	
k_y	10.2	
k_z	1.6	

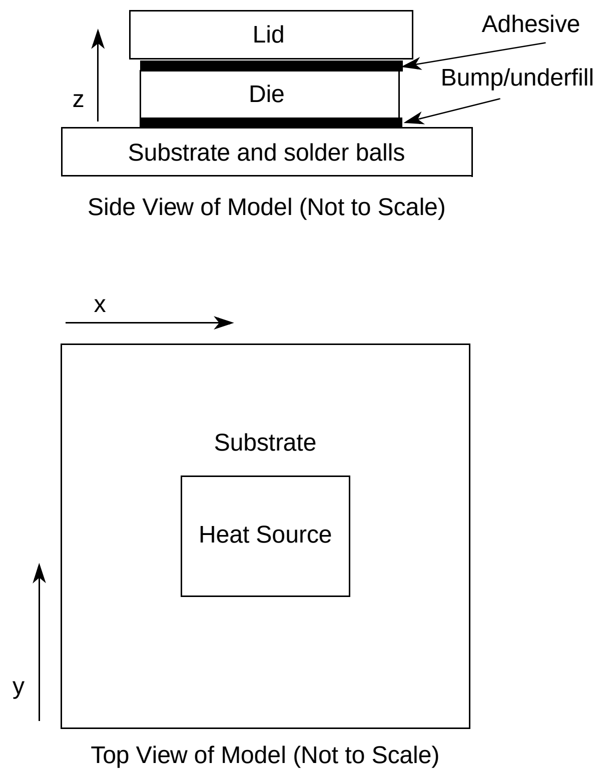


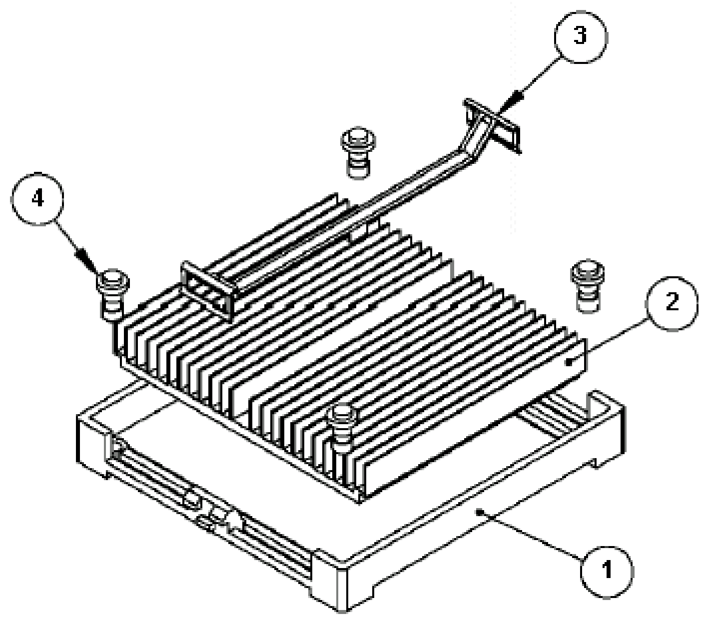
Figure 46. MPC8540 Thermal Model

16.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in Table 59, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Item No	QTY	MEI PN	Description
1	1	MFRAME-2000	HEATSINK FRAME
2	1	MSNK-1120	EXTRUDED HEATSINK
3	1	MCLIP-1013	CLIP
4	4	MPPINS-1000	FRAME ATTACHMENT PINS



Illustrative source provided by
Millennium Electronics (MEI)

Figure 51. Exploded Views (2) of a Heat Sink Attachment using a Plastic Fence

The die junction-to-ambient and the heat sink-to-ambient thermal resistances are common figure-of-merits used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature: airflow, board population (local heat flux of adjacent components), system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the boards, as well as, system-level designs.

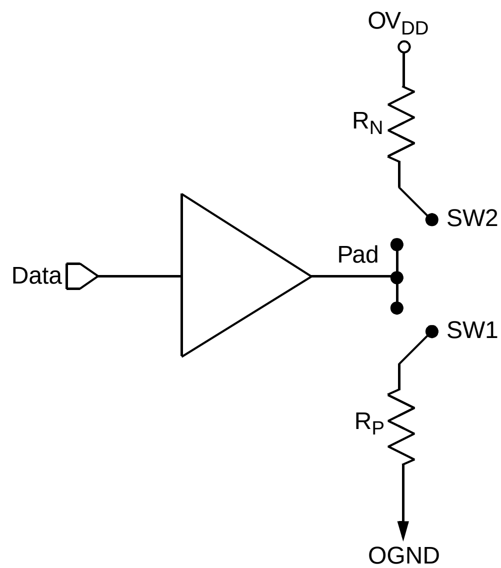


Figure 53. Driver Impedance Measurement

The output impedance of the RapidIO port drivers targets 200-Ω differential resistance. The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 60 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 60. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI/PCI-X	DDR DRAM	RapidIO	Symbol	Unit
R_N	43 Target	25 Target	20 Target	NA	Z_0	W
R_P	43 Target	25 Target	20 Target	NA	Z_0	W
Differential	NA	NA	NA	200 Target	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

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