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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	833MHz
Co-Processors/DSP	-
RAM Controllers	DDR, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1), 10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BFBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8540vt833lb

1 Overview

The following section provides a high-level overview of the MPC8540 features. Figure 1 shows the major functional units within the MPC8540.

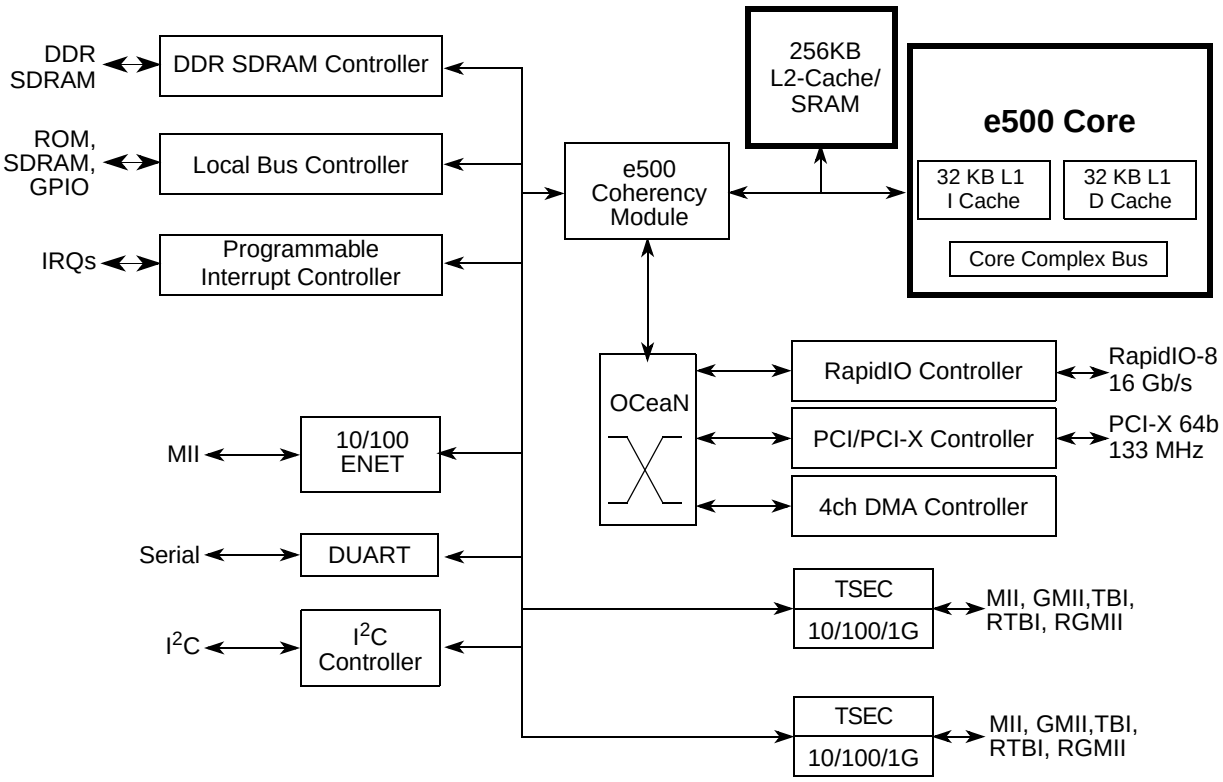

Figure 1. MPC8540 Block Diagram

1.1 Key Features

The following lists an overview of the MPC8540 feature set.

- High-performance, 32-bit Book E–enhanced core that implements the Power Architecture
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis. Separate locking for instructions and data
  - Memory management unit (MMU) especially designed for embedded applications
  - Enhanced hardware and software debug support
  - Performance monitor facility (similar to but different from the MPC8540 performance monitor described in Chapter 18, “Performance Monitor.”

  - Buffer descriptors are backward compatible with MPC8260 and MPC860T 10/100 programming models
  - 9.6-Kbyte jumbo frame support
  - RMON statistics support
  - 2-Kbyte internal transmit and receive FIFOs
  - MII management interface for control and status
  - Programmable CRC generation and checking
  - Ability to force allocation of header information and buffer descriptors into L2 cache.
- OCeaN switch fabric
  - Four-port crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
  - Four-channel controller
  - All channels accessible by both the local and remote masters
  - Extended DMA functions (advanced chaining and striding capability)
  - Support for scatter and gather transfers
  - Misaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Selectable hardware-enforced coherency (snoop/no-snoop)
  - Ability to start and flow control each DMA channel from external 3-pin interface
  - Ability to launch DMA from single write transaction
- PCI/PCI-X controller
  - PCI 2.2 and PCI-X 1.0 compatible
  - 64- or 32-bit PCI port supports at 16 to 66 MHz
  - 64-bit PCI-X support up to 133 MHz
  - Host and agent mode support
  - 64-bit dual address cycle (DAC) support
  - PCI-X supports multiple split transactions
  - Supports PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses
  - Supports posting of processor-to-PCI and PCI-to-memory writes
  - PCI 3.3-V compatible
  - Selectable hardware-enforced coherency

- Power management
  - Fully static 1.2-V CMOS design with 3.3- and 2.5-V I/O
  - Supports power saving modes: doze, nap, and sleep
  - Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle.
- System performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the 8 counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- System access port
  - Uses JTAG interface and a TAP controller to access entire system memory map
  - Supports 32-bit accesses to configuration registers
  - Supports cache-line burst accesses to main memory
  - Supports large block (4-Kbyte) uploads and downloads
  - Supports continuous bit streaming of entire block for fast upload and download
- IEEE 1149.1-compliant, JTAG boundary scan
- 783 FC-PBGA package

2 Electrical Characteristics

This section provides the electrical specifications and thermal characteristics for the MPC8540. The MPC8540 is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings [1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage For devices rated at 667 and 833 MHz For devices rated at 1 GHz		V_{DD}	 –0.3 to 1.32 –0.3 to 1.43	V	
PLL supply voltage For devices rated at 667 and 833 MHz For devices rated at 1 GHz		AV_{DD}	 –0.3 to 1.32 –0.3 to 1.43	V	
DDR DRAM I/O voltage		GV_{DD}	–0.3 to 3.63	V	
Three-speed Ethernet I/O voltage		LV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	
PCI/PCI-X, local bus, RapidIO, 10/100 Ethernet, MII management, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	3
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	4, 5
	Local bus, RapidIO, 10/100 Ethernet, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	5
	PCI/PCI-X	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	–55 to 150	•C	

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

2.1.2 Power Sequencing

The MPC8540 requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD}, AV_{DD}
2. GV_{DD}, LV_{DD}, OV_{DD} (I/O supplies)

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90 percent of their value before the voltage rails on the current step reach 10 percent of theirs.

NOTE

If the items on line 2 must precede items on line 1, please ensure that the delay will not exceed 500 ms and the power sequence is not done greater than once per day in production environment.

NOTE

From a system standpoint, if the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os on the MPC8540 may drive a logic one or zero during power-up.

2.1.3 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8540. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit
Core supply voltage For devices rated at 667 and 833 MHz For devices rated at 1 GHz	V_{DD}	 1.2 V ± 60 mV 1.3 V ± 50 mV	V
PLL supply voltage For devices rated at 667 and 833 MHz For devices rated at 1 GHz	AV_{DD}	 1.2 V ± 60 mV 1.3 V ± 50 mV	V
DDR DRAM I/O voltage	GV_{DD}	2.5 V ± 125 mV	V
Three-speed Ethernet I/O voltage	LV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V
PCI/PCI-X, local bus, RapidIO, 10/100 Ethernet, MII management, DUART, system control and power management, I^2C, and JTAG I/O voltage	OV_{DD}	3.3 V ± 165 mV	V

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8540 for the 3.3-V signals, respectively.

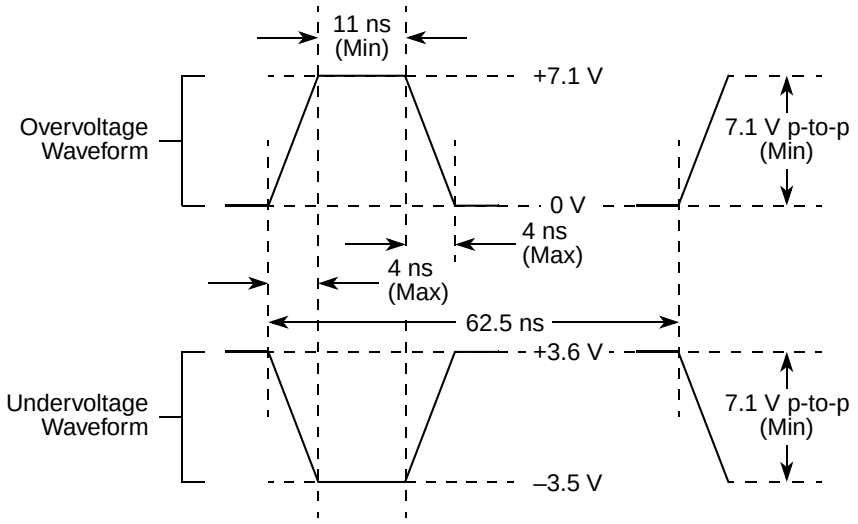

Figure 3. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

2.1.4 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25	OV_{DD} = 3.3 V	1
	42 (default)		
PCI signals	25		2
	42 (default)		
DDR signal	20	GV_{DD} = 2.5 V	
TSEC/10/100 signals	42	LV_{DD} = 2.5/3.3 V	
DUART, system control, I2C, JTAG	42	OV_{DD} = 3.3 V	
RapidIO N/A (LVDS signaling)	N/A		

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the $\overline{\text{PCI\_GNT1}}$ signal at reset.

8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

Table 25 provides the MII transmit AC timing specifications.

Table 25. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX} [2]	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise and fall time	t_{MTXR}, t_{MTXF} [2,3]	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 10 shows the MII transmit AC timing diagram.

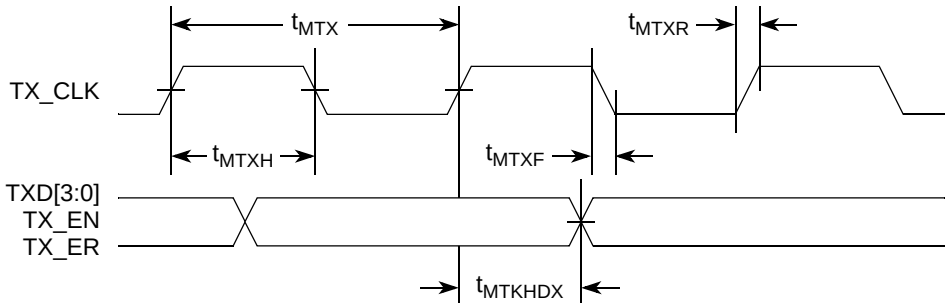

Figure 10. MII Transmit AC Timing Diagram

8.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.3.1 TBI Transmit AC Timing Specifications

Table 27 provides the TBI transmit AC timing specifications.

Table 27. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%, or LV_{DD}=2.5V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t_{TTKHDX}	1.0	—	—	ns
GTX_CLK clock rise and fall time	t_{TTXR}, t_{TTXF} [2,3]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7 V and 1.9 V voltage levels.
3. Guaranteed by design.

Figure 12 shows the TBI transmit AC timing diagram.

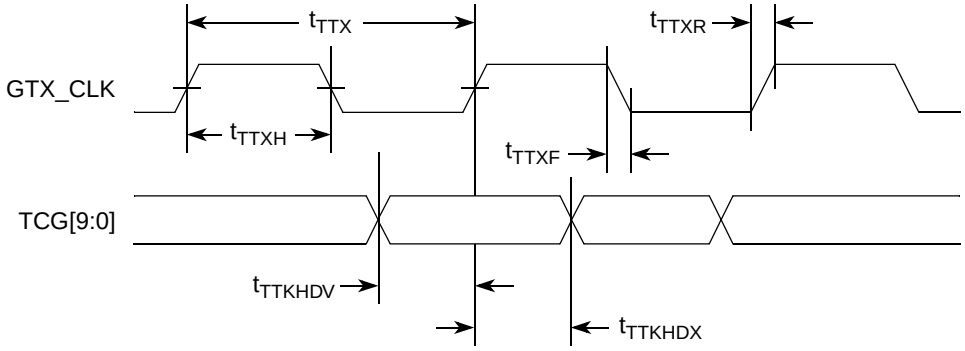

Figure 12. TBI Transmit AC Timing Diagram

8.2.4 RGMII and RTBI AC Timing Specifications

Table 29 presents the RGMII and RTBI AC timing specifications.

Table 29. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT} [5]	–500	0	500	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns
Clock period[3]	t_{RGT} [6]	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4]	t_{RGTH}/t_{RGT} [6]	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3]	t_{RGTH}/t_{RGT} [6]	40	50	60	%
Rise and fall time	t_{RGTR}, t_{RGTF} [6,7]	—	—	0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. The RGMII specification requires that PC board designer add 1.5 ns or greater in trace delay to the RX_CLK in order to meet this specification. However, as stated above, this device will function with only 1.0 ns of delay.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by characterization.
6. Guaranteed by design.
7. Signal timings are measured at 0.5 V and 2.0 V voltage levels.

The eye pattern for a data signal is generated by making a large number of recordings of the signal and then overlaying the recordings. The number of recordings used to generate the eye shall be large enough that further increasing the number of recordings used does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not. Each data signal in the interface shall be carrying random or pseudo-random data when the recordings are made. If pseudo-random data is used, the length of the pseudo-random sequence (repeat length) shall be long enough that increasing the length of the sequence does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not comply with the mask. The data carried by any given data signal in the interface may not be correlated with the data carried by any other data signal in the interface. The zero-crossings of the clock associated with a data signal shall be used as the timing reference for aligning the multiple recordings of the data signal when the recordings are overlaid.

While the method used to make the recordings and overlay them to form the eye pattern is not specified, the method used shall be demonstrably equivalent to the following method. The signal under test is repeatedly recorded with a digital oscilloscope in infinite persistence mode. Each recording is triggered by a zero-crossing of the clock associated with the data signal under test. Roughly half of the recordings are triggered by positive-going clock zero-crossings and roughly half are triggered by negative-going clock zero-crossings. Each recording is at least 1.9 UI in length (to ensure that at least one complete eye is formed) and begins 0.5 UI before the trigger point (0.5 UI before the associated clock zero-crossing). Depending on the length of the individual recordings used to generate the eye pattern, one or more complete eyes will be formed. Regardless of the number of eyes, the eye whose center is immediately to the right of the trigger point is the eye used for compliance testing.

An example of an eye pattern generated using the above method with recordings 3 UI in length is shown in Figure 39. In this example, there is no skew between the signal under test and the associated clock used to trigger the recordings. If skew was present, the eye pattern would be shifted to the left or right relative to the oscilloscope trigger point.

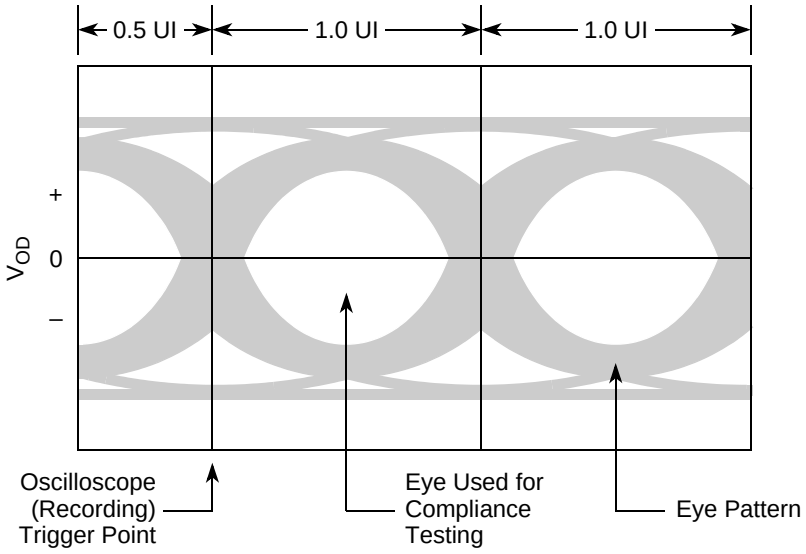

Figure 39. Example Driver Output Eye Pattern

enough that increasing the length of the sequence does not cause the resulting eye pattern to change from one that complies with the RapidIO receive mask to one that does not comply with the mask. The data carried by any given data signal in the interface may not be correlated with the data carried by any other data signal in the interface. The zero-crossings of the clock associated with a data signal shall be used as the timing reference for aligning the multiple recordings of the data signal when the recordings are overlaid.

While the method used to make the recordings and overlay them to form the eye pattern is not specified, the method used shall be demonstrably equivalent to the following method. The signal under test is repeatedly recorded with a digital oscilloscope in infinite persistence mode. Each recording is triggered by a zero-crossing of the clock associated with the data signal under test. Roughly half of the recordings are triggered by positive-going clock zero-crossings and roughly half are triggered by negative-going clock zero-crossings. Each recording is at least 1.9 UI in length (to ensure that at least one complete eye is formed) and begins 0.5 UI before the trigger point (0.5 UI before the associated clock zero-crossing). Depending on the length of the individual recordings used to generate the eye pattern, one or more complete eyes will be formed. Regardless of the number of eyes, the eye whose center is immediately to the right of the trigger point is the eye used for compliance testing.

An example of an eye pattern generated using the above method with recordings 3 UI in length is shown in Figure 41. In this example, there is no skew between the signal under test and the associated clock used to trigger the recordings. If skew was present, the eye pattern would be shifted to the left or right relative to the oscilloscope trigger point.

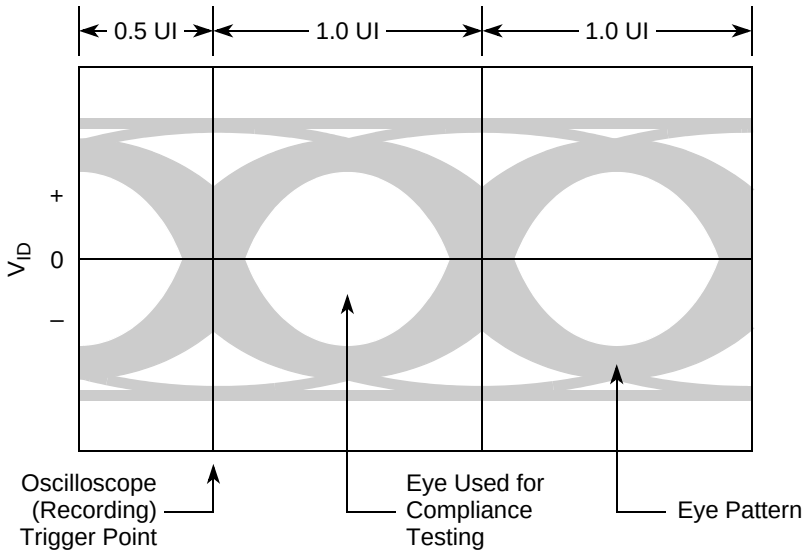

Figure 41. Example Receiver Input Eye Pattern

3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
7. The socket lid must always be oriented to A1.

14.3 Pinout Listings

Table 53 provides the pin-out listing for the MPC8540, 783 FC-PBGA package.

Table 53. MPC8540 Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI/PCI-X				
PCI_AD[63:0]	AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14, V15, W15, Y15, AA15, AB15, AC15, AD15, AG15, AH15, V16, W16, AB16, AC16, AD16, AE16, AF16, V17, W17, Y17, AA17, AB17, AE17, AF17, AF18, AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9, AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11, AG11, AH11, V12, W12, Y12, AB12, AD12, AE12, AG12, AH12, V13, Y13, AB13, AC13	I/O	OV_{DD}	17
PCI_C_$\overline{BE}$[7:0]	AG13, AH13, V14, W14, AH8, AB10, AD11, AC12	I/O	OV_{DD}	17
PCI_PAR	AA11	I/O	OV_{DD}	
PCI_PAR64	Y14	I/O	OV_{DD}	
$\overline{\text{PCI\_FRAME}}$	AC10	I/O	OV_{DD}	2
$\overline{\text{PCI\_TRDY}}$	AG10	I/O	OV_{DD}	2
$\overline{\text{PCI\_IRDY}}$	AD10	I/O	OV_{DD}	2
$\overline{\text{PCI\_STOP}}$	V11	I/O	OV_{DD}	2
$\overline{\text{PCI\_DEVSEL}}$	AH10	I/O	OV_{DD}	2
PCI_IDSEL	AA9	I	OV_{DD}	
$\overline{\text{PCI\_REQ64}}$	AE13	I/O	OV_{DD}	5, 10
$\overline{\text{PCI\_ACK64}}$	AD13	I/O	OV_{DD}	2
$\overline{\text{PCI\_PERR}}$	W11	I/O	OV_{DD}	2
$\overline{\text{PCI\_SERR}}$	Y11	I/O	OV_{DD}	2, 4
$\overline{\text{PCI\_REQ0}}$	AF5	I/O	OV_{DD}	
$\overline{\text{PCI\_REQ}}$[1:4]	AF3, AE4, AG4, AE5	I	OV_{DD}	
$\overline{\text{PCI\_GNT}}$[0]	AE6	I/O	OV_{DD}	
$\overline{\text{PCI\_GNT}}$[1:4]	AG5, AH5, AF6, AG6	O	OV_{DD}	5, 9

Table 53. MPC8540 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{IRQ\_OUT}}$	AB21	O	OV_{DD}	2, 4
Ethernet Management Interface				
EC_MDC	F1	O	OV_{DD}	5, 9
EC_MDIO	E1	I/O	OV_{DD}	
Gigabit Reference Clock				
EC_GTX_CLK125	E2	I	LV_{DD}	
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_TXD[7:4]	A6, F7, D7, C7	O	LV_{DD}	5, 9
TSEC1_TXD[3:0]	B7, A7, G8, E8	O	LV_{DD}	9, 19
TSEC1_TX_EN	C8	O	LV_{DD}	11
TSEC1_TX_ER	B8	O	LV_{DD}	
TSEC1_TX_CLK	C6	I	LV_{DD}	
TSEC1_GTX_CLK	B6	O	LV_{DD}	18
TSEC1_CRS	C3	I	LV_{DD}	
TSEC1_COL	G7	I	LV_{DD}	
TSEC1_RXD[7:0]	D4, B4, D3, D5, B5, A5, F6, E6	I	LV_{DD}	
TSEC1_RX_DV	D2	I	LV_{DD}	
TSEC1_RX_ER	E5	I	LV_{DD}	
TSEC1_RX_CLK	D6	I	LV_{DD}	
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_TXD[7:2]	B10, A10, J10, K11,J11, H11	O	LV_{DD}	5, 9
TSEC2_TXD[1:0]	G11, E11	O	LV_{DD}	
TSEC2_TX_EN	B11	O	LV_{DD}	11
TSEC2_TX_ER	D11	O	LV_{DD}	
TSEC2_TX_CLK	D10	I	LV_{DD}	
TSEC2_GTX_CLK	C10	O	LV_{DD}	18
TSEC2_CRS	D9	I	LV_{DD}	
TSEC2_COL	F8	I	LV_{DD}	
TSEC2_RXD[7:0]	F9, E9, C9, B9, A9, H9, G10, F10	I	LV_{DD}	
TSEC2_RX_DV	H8	I	LV_{DD}	
TSEC2_RX_ER	A8	I	LV_{DD}	

Table 53. MPC8540 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_RX_CLK	E10	I	LV_{DD}	
10/100 Ethernet (MII) Interface				
FEC_TXD[3:0]	M1, N1, N4, N5	O	OV_{DD}	
FEC_TX_EN	P11	O	OV_{DD}	
FEC_TX_ER	P10	O	OV_{DD}	
FEC_TX_CLK	V6	I	OV_{DD}	
FEC_CRS	N10	I	OV_{DD}	
FEC_COL	N11	I	OV_{DD}	
FEC_RXD[3:0]	N9, N8, N7, N6	I	OV_{DD}	
FEC_RX_DV	P8	I	OV_{DD}	
FEC_RX_ER	P9	I	OV_{DD}	
FEC_RX_CLK	V9	I	OV_{DD}	
RapidIO Interface				
RIO_RCLK	Y25	I	OV_{DD}	
$\overline{\text{RIO\_RCLK}}$	Y24	I	OV_{DD}	
RIO_RD[0:7]	T25, U25, V25, W25, AA25, AB25, AC25, AD25	I	OV_{DD}	
$\overline{\text{RIO\_RD}}$[0:7]	T24, U24, V24, W24, AA24, AB24, AC24, AD24	I	OV_{DD}	
RIO_RFRAME	AE27	I	OV_{DD}	
$\overline{\text{RIO\_RFRAME}}$	AE26	I	OV_{DD}	
RIO_TCLK	AC20	O	OV_{DD}	11
$\overline{\text{RIO\_TCLK}}$	AE21	O	OV_{DD}	11
RIO_TD[0:7]	AE18, AC18, AD19, AE20, AD21, AE22, AC22, AD23	O	OV_{DD}	
$\overline{\text{RIO\_TD}}$[0:7]	AD18, AE19, AC19, AD20, AC21, AD22, AE23, AC23	O	OV_{DD}	
RIO_TFRAME	AE24	O	OV_{DD}	
$\overline{\text{RIO\_TFRAME}}$	AE25	O	OV_{DD}	
RIO_TX_CLK_IN	AF24	I	OV_{DD}	
$\overline{\text{RIO\_TX\_CLK\_IN}}$	AF25	I	OV_{DD}	
I^2C interface				
IIC_SDA	AH22	I/O	OV_{DD}	4, 20
IIC_SCL	AH23	I/O	OV_{DD}	4, 20

15.4 Frequency Options

Table 58 shows the expected frequency values for the platform frequency when using a CCB to SYSCLK ratio in comparison to the memory bus speed.

Table 58. Frequency Options with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)								
	16.67	25	33.33	41.63	66.67	83	100	111	133.33
	Platform/CCB Frequency (MHz)								
2							200	222	267
3					200	250	300	333	
4					267	333			
5				208	333				
6			200	250					
8		200	267	333					
9		225	300						
10		250	333						
12	200	300							
16	267								

16 Thermal

This section describes the thermal specifications of the MPC8540.

16.1 Thermal Characteristics

Table 59 provides the package thermal characteristics for the MPC8540.

Table 59. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection on four layer board (2s2p)	$R_{\theta JMA}$	16	°C/W	1, 2
Junction-to-ambient (@100 ft/min or 0.5 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	14	°C/W	1, 2
Junction-to-ambient (@200 ft/min or 1 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	12	•C/W	1, 2
Junction-to-board thermal	$R_{\theta JB}$	7.5	•C/W	3

Table 59. Package Thermal Characteristics (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-case thermal	$R_{\theta JC}$	0.8	•C/W	4

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-6 with the board horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). Cold plate temperature is used for case temperature; measured value includes the thermal resistance of the interface layer.

16.2 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 45. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force.

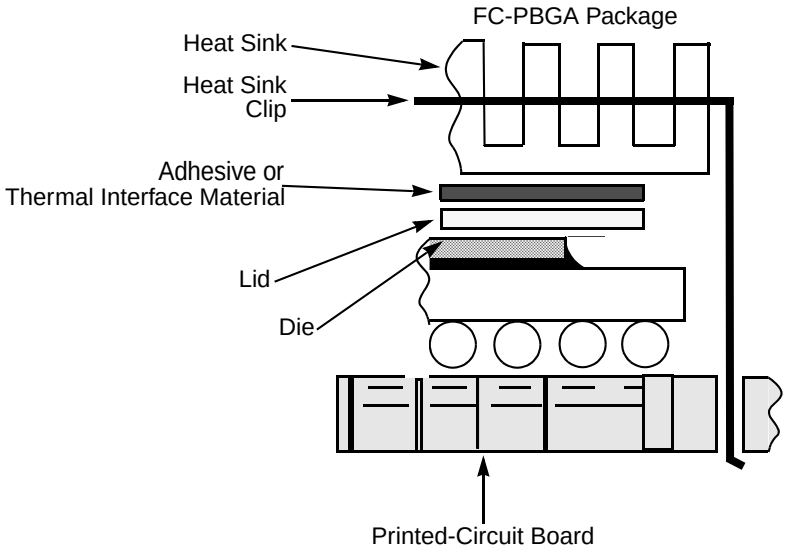

Figure 45. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the MPC8540. There are several commercially-available heat sinks from the following vendors:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

17 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8540.

17.1 System Clocking

The MPC8540includes two PLLs.

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 15.2, “Platform/System PLL Ratio.”
2. The e500 Core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 15.3, “e500 Core PLL Ratio.”

17.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}1$ and $AV_{DD}2$, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide three independent filter circuits as illustrated in Figure 52, one to each of the three AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias.

Figure 52 shows the PLL power supply filter circuit.

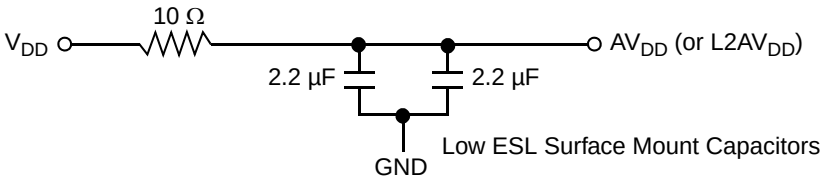

Figure 52. PLL Power Supply Filter Circuit

Table 61. Document Revision History (continued)

Rev. No.	Substantive Change(s)
3.2	Updated Table 1 and Table 2 with 1.0 GHz device parameter requirements. Added Section 2.1.2, “Power Sequencing”. Updated Table 4 with Maximum power data. Updated Table 4 and Table 5 with 1 GHz speed grade information. Updated Table 6 with corrected typical I/O power numbers. Updated Table 7 Note 2 lower voltage measurement point. Replaced Table 7 Note 5 with spread spectrum clocking guidelines. Added to Table 8 rise and fall time information. Added Section 4.4, “Real Time Clock Timing”. Added precharge information to Section 6.2.2, “DDR SDRAM Output AC Timing Specifications”. Updated Table 20 minimum and maximum baud rates. Removed V_{IL} and V_{IH} references from Table 23, Table 24, Table 25, and Table 26. Added reference level note to Table 23, Table 24, Table 25, Table 26, Table 27, Table 28, and Table 29. Updated TXD references to TCG in Section 8.2.3.1, “TBI Transmit AC Timing Specifications”. Updated PMA_RX_CLK references to RX_CLK in Section 8.2.3.2, “TBI Receive AC Timing Specifications”. Updated t_{TTKHDX} value in Table 27. Updated RXD references to RCG in Section 8.2.3.2, “TBI Receive AC Timing Specifications”. Updated Table 29 Note 2. Removed V_{IL} and V_{IH} references from Table 31, and Table 32. Added reference level note to Table 31, and Table 32. Corrected Figure 15 and Figure 16. Corrected Table 34 f_{MDC} and t_{MDC} to reflect the correct minimum operating frequency. Updated Table 34 t_{MDKHDV} and t_{MDKHDX} values for clarification. Added t_{LBKHKT} and updated Note 2 in Table 37. Corrected $\overline{\text{LGTA}}$ timing references in Figure 19. Updated Figure 20, Figure 22, and Figure 24. Updated Figure 44. Clarified Table 53 Note 5. Updated Table 54 and Table 55 with 1 GHz information. Added heat sink removal discussion to Section 16.2.3, “Thermal Interface Materials”. Corrected and added 1 GHz part number to Table 62.
3.1	Updated Table 4 and Table 5. Added Table 6. Added MCK duty cycle to Table 16. Updated f_{MDC}, t_{MDC}, t_{MDKHDV}, and t_{MDKHDX} parameters in Table 34. Added LALE to $t_{LBKHOV3}$ parameter in Table 36 and Table 37, and updated Figure 19 and Figure 20. Corrected active level designations of some of the pins in Table 53. Updated Table 62.

Table 61. Document Revision History (continued)

Rev. No.	Substantive Change(s)
1.2	Section 1.1.1—Updated feature list. Section 1.2.1.1—Updated notes for Table 1. Section 1.2.1.2—Removed 5-V PCI interface overshoot and undershoot figure. Section 1.2.1.3—Added this section to summarize impedance driver settings for various interfaces. Section 1.4—Updated rows in Reset Initialization timing specifications table. Added a table with DLL and PLL timing specifications. Section 1.5.2.2—Updated note 6 of DDR SDRAM Output AC Timing Specifications table. Section 1.7—Changed the minimum input low current from -600 to -15 μA for the RGMII DC electrical characteristics. Section 1.8.2—Changed LCS[3:4] to TSEC1_TXD[6:5] in. Updated notes regarding LCS[3:4]. Section 1.13.2—Updated the mechanical dimensions diagram for the package. Section 1.13.3—Updated the notes for LBCTL, TRIG_OUT, and ASLEEP. Corrected pin assignments for IIC_SDA and IIC_SCL. Corrected reserved pin assignment of V11 to U11. V11 is actually $\overline{\text{PCI\_STOP}}$. Section 1.14.1—Updated the table for frequency options with respect to platform/CCB frequencies. Section 1.14.4—Edited Frequency options with respect to memory bus speeds.
1.1	Section 1.6.1—Added symbols and note for the GTX_CLK125 timing parameters. Section 1.11.3—Updated pin list table: LGPL5/LSDAMUX to LGPL5, LA[27:29] and LA[30:31] to LA[27:31], FEC_TXD[0:3] to FEC_TXD[3:0], FEC_RXD[0:3] to FEC_RXD[3:0], TRST to $\overline{\text{TRST}}$, added GBE Clocking section and EC_GTX_CLK125 signal. Updated thermal model information to match current offering.
1	Original Customer Version.

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