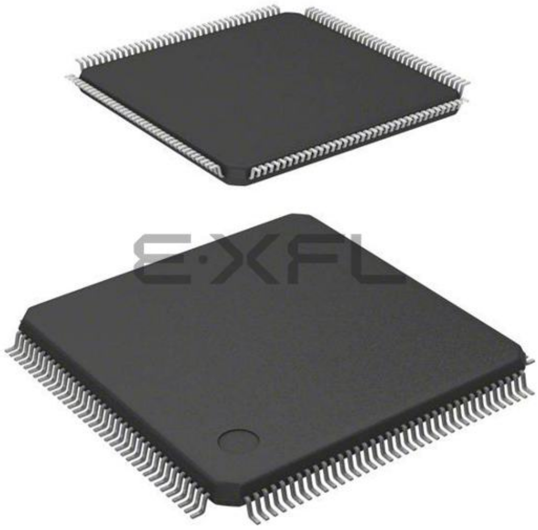
STMicroelectronics - SPC56EL70L5CBFR Datasheet



Details	
Product Status	Obsolete
Core Processor	e200z4d
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56el70l5cbfr

Table 1. SPC56XL70/SPC56X64 device summary (continued)

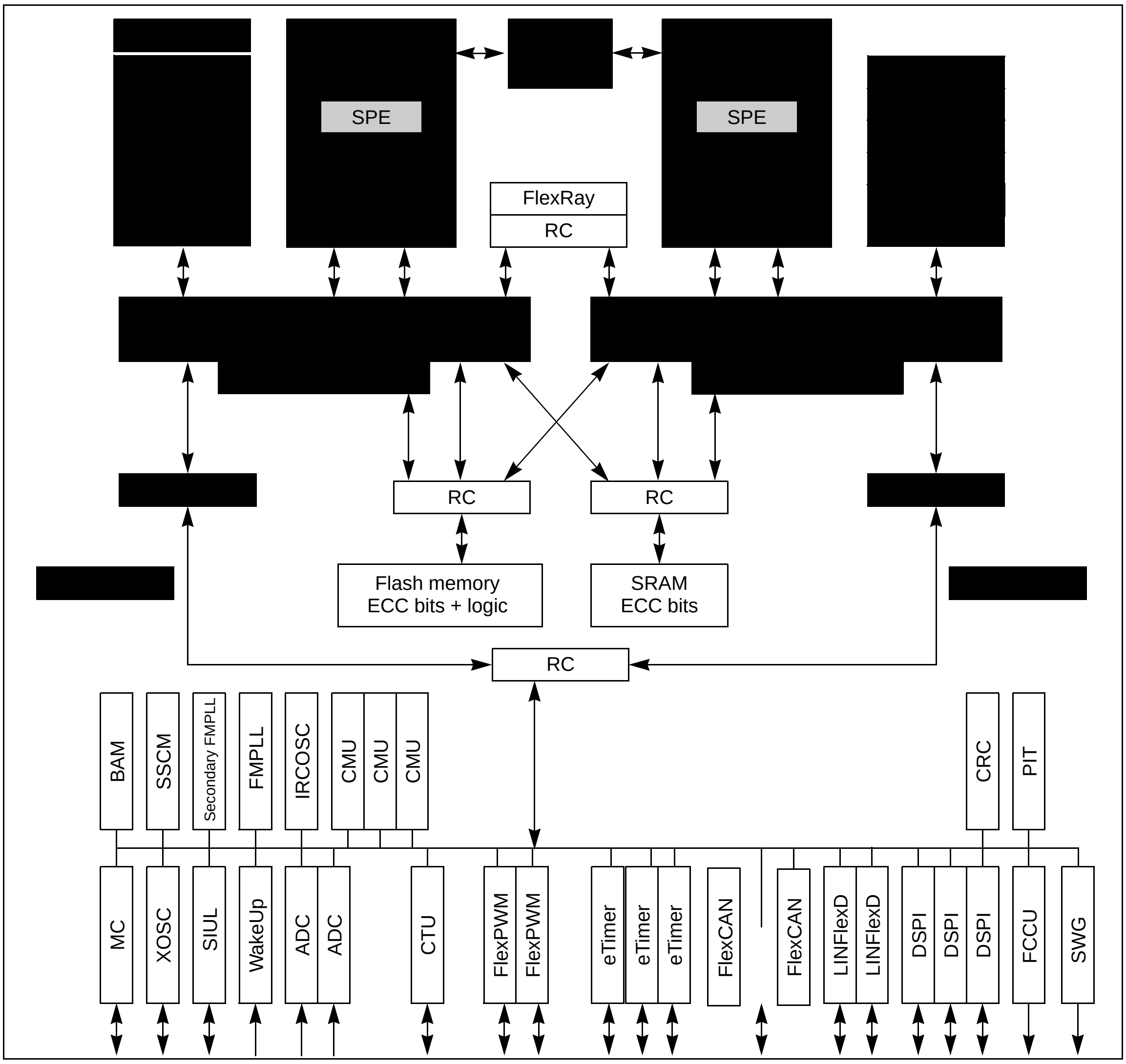
Feature		SPC56EL64	SPC56EL70	SPC564L64	SPC564L70
Modules (cont.)	Deserial Serial Peripheral Interface (DSPI)	3 × DSPI as many as 8 chip selects			
	Cyclic Redundancy Checker (CRC) unit	Yes			
	Junction temperature sensor (TSENS)	Yes, replicated module			
	Digital I/Os	t 16			
Supply	Device power supply	3.3 V with integrated bypassable ballast transistor External ballast transistor not needed for bare die			
	Analog reference voltage	3.0 V – 3.6 V and 4.5 V – 5.5 V			
Clocking	Frequency-modulated phase-locked loop (FMPLL)	2			
	Internal RC oscillator	16 MHz			
	External crystal oscillator	4 – 40 MHz			
Debug	Nexus	Level 3+			
Packages	LQFP	100 pins 144 pins			
Temperature	Temperature range (junction)	–40 to 150 °C			
	Ambient temperature range using external ballast transistor (LQFP)	–40 to 125 °C			

1. The third eTimer is not connected to any pins on the package. Its usage is confined internally to the device.
2. The second FlexPWM is not connected to any pins on the package. Its usage is confined internally to the device.

1.4 Block diagram

Figure 1 shows a top-level block diagram of the SPC56EL70x/SPC564L70x device.

Figure 1. SPC56EL70 block diagram



ADC	– Analog-to-Digital Converter
BAM	– Boot Assist Module
CMU	– Clock Monitoring Unit
CRC	– Cyclic Redundancy Check unit
CTU	– Cross Triggering Unit
DSPI	– Serial Peripherals Interface
ECC	– Error Correction Code
ECSM	– Error Correction Status Module
eDMA	– Enhanced Direct Memory Access controller
FCCU	– Fault Collection and Control Unit
FlexCAN	– Controller Area Network controller
FMPLL	– Frequency Modulated Phase Locked Loop
INTC	– Interrupt Controller
IRCOSC	– Internal RC Oscillator
JTAG	– Joint Test Action Group interface
LINFlexD	– LIN controller with DMA support
MC	– Mode Entry, Clock, Reset, & Power
PBRIDGE	– Peripheral bridge
PIT	– Periodic Interrupt Timer
PMU	– Power Management Unit
RC	– Redundancy Checker
RTC	– Real Time Clock
SEMA4	– Semaphore Unit
SIUL	– System Integration Unit Lite
SSCM	– System Status and Configuration Module
STM	– System Timer Module
SWG	– Sine Wave Generator
SWT	– Software Watchdog Timer
TSENS	– Temperature Sensor
XOSC	– Crystal Oscillator

1.5 Feature details

1.5.1 High-performance e200z4d core

The e200z4d Power Architecture® core provides the following features:

- 2 independent execution units, both supporting fixed-point and floating-point operations
- Dual issue 32-bit Power Architecture technology compliant
  - 5-stage pipeline (IF, DEC, EX1, EX2, WB)
  - In-order execution and instruction retirement
- Full support for Power Architecture instruction set and Variable Length Encoding (VLE)
  - Mix of classic 32-bit and 16-bit instruction allowed
  - Optimization of code size possible
- Thirty-two 64-bit general purpose registers (GPRs)
- Harvard bus (32-bit address, 64-bit data)
  - I-Bus interface capable of one outstanding transaction plus one piped with no wait-on-data return
  - D-Bus interface capable of two transactions outstanding to fill AHB pipe
- I-cache and I-cache controller
  - 4 KB, 256-bit cache line (programmable for 2- or 4-way)
- No data cache
- 16-entry MMU
- 8-entry branch table buffer
- Branch look-ahead instruction buffer to accelerate branching
- Dedicated branch address calculator
- 3 cycles worst case for missed branch
- Load/store unit
  - Fully pipelined
  - Single-cycle load latency
  - Big- and little-endian modes supported
  - Misaligned access support
  - Single stall cycle on load to use
- Single-cycle throughput (2-cycle latency) integer 32 × 32 multiplication
- 4 – 14 cycles integer 32 × 32 division (average division on various benchmark of nine cycles)
- Single precision floating-point unit
  - 1 cycle throughput (2-cycle latency) floating-point 32 × 32 multiplication
  - Target 9 cycles (worst case acceptable is 12 cycles) throughput floating-point 32 × 32 division
  - Special square root and min/max function implemented
- Signal processing support: APU-SPE 1.1
  - Support for vectorized mode: as many as two floating-point instructions per clock
- Vectored interrupt support
- Reservation instruction to support read-modify-write constructs

1.5.19 System timer module (STM)

The STM implements the following features:

- Up-counter with 4 output compare registers
- OS task protection and hardware tick implementation per AUTOSAR[a] requirement

The STM is replicated for each processor.

1.5.20 Software watchdog timer (SWT)

This module implements the following features:

- Fault tolerant output
- Safe internal RC oscillator as reference clock
- Windowed watchdog
- Program flow control monitor with 16-bit pseudorandom key generation
- Allows a high level of safety (SIL3 monitor)

The SWT module is replicated for each processor.

1.5.21 Fault collection and control unit (FCCU)

The FCCU module has the following features:

- Redundant collection of hardware checker results
- Redundant collection of error information and latch of faults from critical modules on the device
- Collection of self-test results
- Configurable and graded fault control
  - Internal reactions (no internal reaction, IRQ, Functional Reset, Destructive Reset, or Safe mode entered)
  - External reaction (failure is reported to the external/surrounding system via configurable output pins)

1.5.22 System Integration Unit Lite (SIUL)

The SIUL controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

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[a] Automotive Open System Architecture

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0 to 8 bytes data length
  - Programmable bit rate as fast as 1Mbit/s
- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as receive or transmit buffer, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a 6-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid FMPLL jitter

1.5.28 Serial communication interface module (LINFlexD)

The LINFlexD module (LINFlex with DMA support) on this device features the following:

- Supports LIN Master mode, LIN Slave mode and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 specifications
- Manages LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store as many as 8 data bytes
  - Supports messages as long as 64 bytes
  - Detection and flagging of LIN errors (Sync field, delimiter, ID parity, bit framing, checksum and Time-out errors)
  - Classic or extended checksum calculation
  - Configurable break duration of up to 50-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features (Loop back, LIN bus stuck dominant detection)
  - Interrupt driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format

3.17 SWG electrical characteristics

Table 29. SPC56XL70 SWG Specifications

Symbol	Parameter	Value		
		Minimum	Typical	Maximum
T	Input clock	12 MHz	16 MHz	20 MHz
T	Frequency Range	1KHz	—	50 KHz
T	Peak to Peak(1)	0.4 V	—	2.0V
T	Peak to Peak variation(2)	-6%	—	6%
T	Common Mode(3)	—	1.3 V	—
T	Common Mode variation	-6%	—	6%
T	SiNAD(4)	45 dB	—	—
T	Load C	25 pF	—	100 pF
T	Load I	0 µA	—	100 µA
T	ESD Pad Resistance(5)	230 :	—	360 :

1. Peak to Peak value is measured with no R or I load.
2. Peak to Peak excludes noise, SiNAD must be considered.
3. Common mode value is measured with no R or I load.
4. SiNAD is measured at Max Peak to Peak voltage.
5. Internal device routing resistance. ESD pad resistance is in series and must be considered for max Peak to Peak voltages, depending on application I load and/or R load.

3.18 AC specifications

3.18.1 Pad AC specifications

Table 30. Pad AC specifications (3.3 V, IPP_HVE = 0) (1)

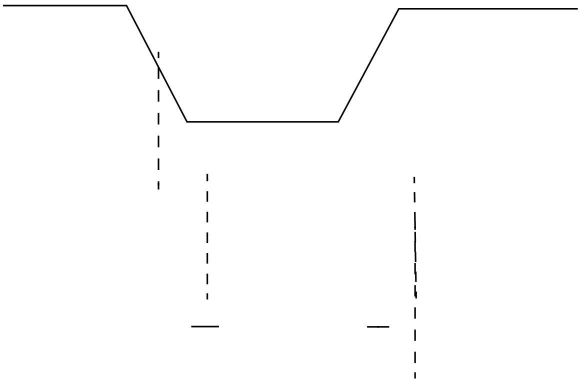
No	Pad		Tswitchon [1] (ns)			Rise/Fall (2) (ns)			Frequency (MHz)			Current slew (3) (mA/ns)			Load drive (pF)
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	T	3	—	40	—	—	40	—	—	4	0.01	—	2	25
			3	—	40	—	—	50	—	—	2	0.01	—	2	50
			3	—	40	—	—	75	—	—	2	0.01	—	2	100
			3	—	40	—	—	100	—	—	2	0.01	—	2	200
2	Medium	T	1	—	15	—	—	12	—	—	40	2.5	—	7	25
			1	—	15	—	—	25	—	—	20	2.5	—	7	50
			1	—	15	—	—	40	—	—	13	2.5	—	7	100
			1	—	15	—	—	70	—	—	7	2.5	—	7	200

Table 30. Pad AC specifications (3.3 V, IPP_HVE = 0)(1) (continued)

No	Pad		Tswitchon[1] (ns)			Rise/Fall(2) (ns)			Frequency (MHz)			Current slew(3) (mA/ns)			Load drive (pF)
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
3	Fast	T	1	—	6	—	—	4	—	—	72	3	—	40	25
			1	—	6	—	—	7	—	—	55	7	—	40	50
			1	—	6	—	—	12	—	—	40	7	—	40	100
			1	—	6	—	—	18	—	—	25	7	—	40	200
4	Symmetric	T	1	—	8	—	—	5	—	—	50	3	—	25	25

1. Propagation delay from $V_{DD\_HV\_IOx}/2$ of internal signal to Pchannel/Nchannel switch-on condition (i.e. t_PHL and t_PLH in *Figure 12: Pad output delay*).
2. Slope at rising/falling edge(i.e. t_F and t_R in *Figure 12: Pad output delay*).
3. Data based on characterization results, not tested in production.

Figure 12. Pad output delay



[1] t_F and t_R are transient times at the FAR END.
[2] t_{PHL} and t_{PLH} are measured at the pad.
[3] Core input slew = 1ns (0 to vdd).

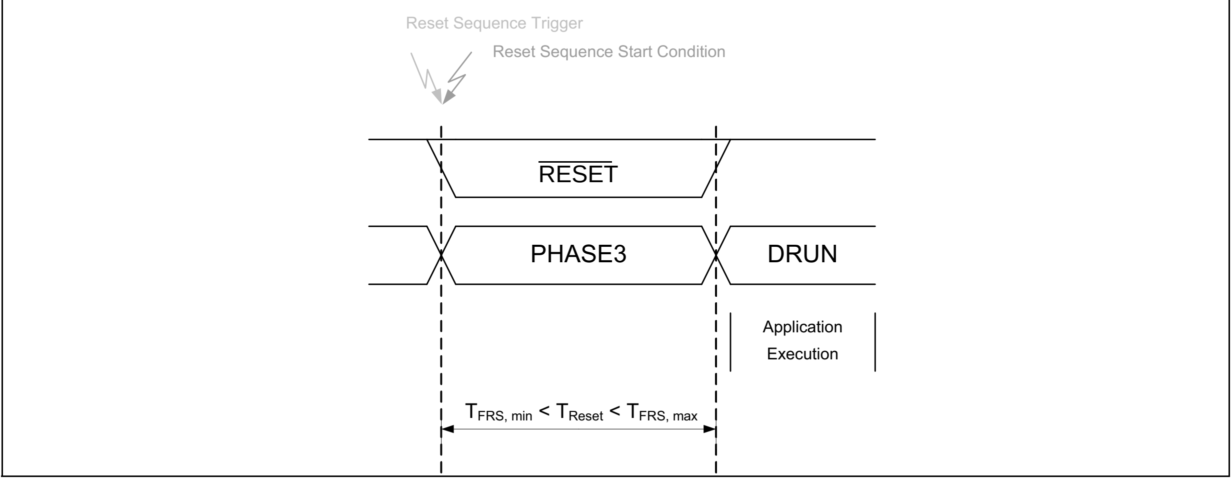
3.19 Reset sequence

This section shows the duration for different reset sequences. It describes the different reset sequences and it specifies the start conditions and the end indication for the reset sequences.

3.19.1 Reset sequence duration

Table 31 specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in *Section 3.19.2: Reset sequence description*.

Figure 17. Functional Reset Sequence Short



The reset sequences shown in *Figure 16* and *Figure 17* are triggered by functional reset events. $\overline{\text{RESET}}$ is driven low during these two reset sequences ***only if*** the corresponding functional reset source (which triggered the reset sequence) was enabled to drive $\overline{\text{RESET}}$ low for the duration of the internal reset sequence(c).

3.19.3 Reset sequence trigger mapping

The following table shows the possible trigger events for the different reset sequences. It specifies the reset sequence start conditions as well as the reset sequence end indications that are the basis for the timing data provided in *Table 31*.

Table 32. Reset sequence trigger — Reset sequence

			Reset Sequence		
Reset Sequence Trigger	**Reset Sequence Start Condition**	**Reset Sequence End Indication**	**Destructive reset sequence, bist enabled(1)**	**Destructive reset sequence, bisT disabled(1)**	**External reset sequence drure23 re23 re23 re23d(S114.sere23**

sss q67Tc.1

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c. See RGM_FBRE register for more details.

3. The system clock frequency needs to be four times faster than the TCK frequency.

Figure 26. Nexus output timing

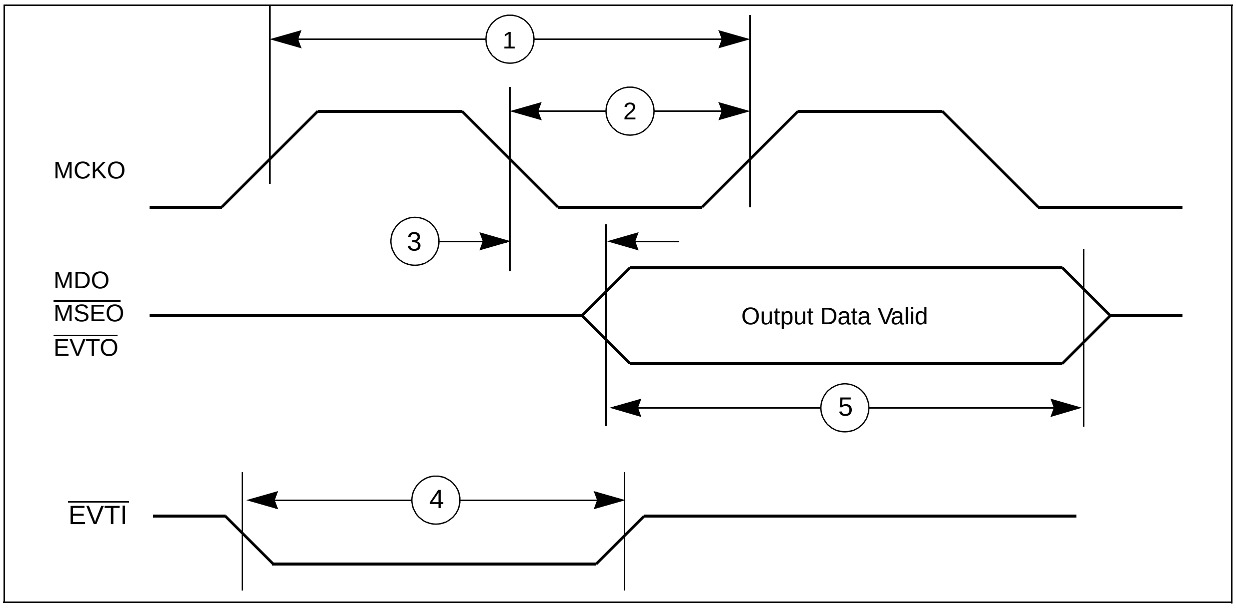

Figure 27. Nexus DDR Mode output timing

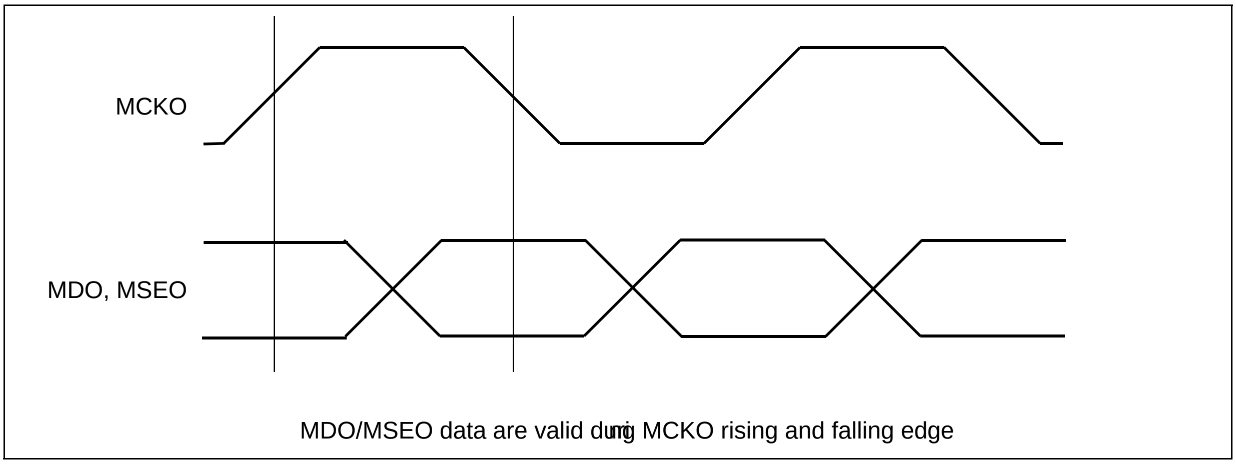

Figure 33. DSPI classic SPI timing — slave, CPHA = 1

Figure 34. DSPI modified transfer format timing — master, CPHA = 0