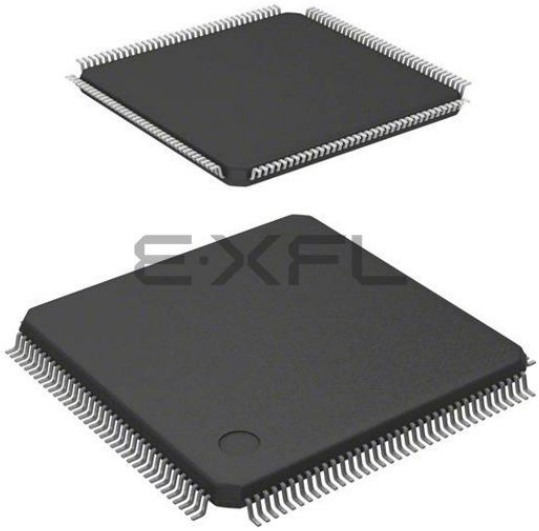

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56el70l5cbfsy

List of figures

1.3 Device comparison

Table 1. SPC56XL70/SPC56X64 device summary

Feature		SPC56EL64	SPC56EL70	SPC564L64	SPC564L70
CPU	Type	2 × e200z4 (in lock-step or decoupled operation)	2 × e200z4 (in lock-step or decoupled operation)	1 × e200z4	1 × e200z4
	Architecture	Harvard			
	Execution speed	0–120 MHz (+2% FM)			
	DMIPS intrinsic performance	>240 MIPS			
	SIMD (DSP + FPU)	Yes			
	MMU	16 entry			
	Instruction set PPC	Yes			
	Instruction set VLE	Yes			
	Instruction cache	4 KB, EDC			
	MPU-16 regions	Yes, replicated module			
	Semaphore unit (SEMA4)	Yes			
Buses	Core bus	AHB, 32-bit address, 64-bit data			
	Internal periphery bus	32-bit address, 32-bit data			
Crossbar	Master × slave ports	Lock Step Mode: 4 × 3 Decoupled Parallel Mode: 6 × 3		4 x 3	
Memory	Code/data flash	1.5 MB, ECC, RWW	2 MB, ECC, RWW	1.5 MB, ECC, RWW	2 MB, ECC, RWW
	Static RAM (SRAM)	160 KB, ECC	192 KB, ECC	160 KB, ECC	192 KB, ECC

The SIU provides the following features:

- Centralized pad control on a per-pin basis
  - Pin function selection
  - Configurable weak pull-up/down
  - Configurable slew rate control (slow/medium/fast)
  - Hysteresis on GPIO pins
  - Configurable automatic safe mode pad control
- Input filtering for external interrupts

1.5.23 Non-maskable interrupt (NMI)

The non-maskable interrupt with de-glitching filter supports high-priority core exceptions.

1.5.24 Boot assist module (BAM)

The BAM is a block of read-only memory with hard-coded content. The BAM program is executed only if serial booting mode is selected via boot configuration pins.

The BAM provides the following features:

- Enables booting via serial mode (FlexCAN or LINFlex-UART)
- Supports programmable 64-bit password protection for serial boot mode
- Supports serial bootloading of either Power Architecture code (default) or VLE code
- Automatic switch to serial boot mode if internal flash memory is blank or invalid

1.5.25 System status and configuration module (SSCM)

The SSCM on this device features the following:

- System configuration and status
- Debug port status and debug port enable
- Multiple boot code starting locations out of reset through implementation of search for valid Reset Configuration Half Word
- Sets up the MMU to allow user boot code to execute as either Power Architecture code (default) or as VLE code out of flash memory
- Triggering of device self-tests during reset phase of device boot

1.5.26 FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0 to 8 bytes data length
  - Programmable bit rate as fast as 1Mbit/s
- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as receive or transmit buffer, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a 6-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid FMPLL jitter

1.5.28 Serial communication interface module (LINFlexD)

The LINFlexD module (LINFlex with DMA support) on this device features the following:

- Supports LIN Master mode, LIN Slave mode and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 specifications
- Manages LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store as many as 8 data bytes
  - Supports messages as long as 64 bytes
  - Detection and flagging of LIN errors (Sync field, delimiter, ID parity, bit framing, checksum and Time-out errors)
  - Classic or extended checksum calculation
  - Configurable break duration of up to 50-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features (Loop back, LIN bus stuck dominant detection)
  - Interrupt driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit, 9-bit, or 16-bit words)
  - Configurable parity scheme: none, odd, even, always 0
  - Speed as fast as 2 Mbit/s
  - Error detection and flagging (Parity, Noise and Framing errors)
  - Interrupt driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods
- Support for DMA enabled transfers

A FlexPWM module implements the following features:

- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- Maximum operating frequency as high as 120 MHz
  - Clock source not modulated and independent from system clock (generated via secondary FMPLL)
- Fine granularity control for enhanced resolution of the PWM period
- PWM outputs can operate as complementary pairs or independent channels
- Ability to accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software control for each PWM output
- All outputs can be forced to a value simultaneously
- PWMX pin can optionally output a third signal from each channel
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual edge capture functionality
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - External digital pin
  - Internal timer channel
  - External ADC input, taking into account values set in ADC high- and low-limit registers
- DMA support

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
64	B[14]	SIUL	—	GPIO[30]
		eTimer_0	—	ETC[4]
		SIUL	—	EIRQ[19]
		ADC_1	—	AN[1]
65	E[11]	SIUL	—	GPIO[75]
		ADC_1	—	AN[4]
66	C[0]	SIUL	—	GPIO[32]
		ADC_1	—	AN[3]
67	E[12]	SIUL	—	GPIO[76]
		ADC_1	—	AN[6]
68	E[0]	SIUL	—	GPIO[64]
		ADC_1	—	AN[5]
69	BCTRL	—		
70	$V_{DD\_LV\_COR}$	—		
71	$V_{SS\_LV\_COR}$	—		
72	$V_{DD\_HV\_PMU}$	—		
73	A[0]	SIUL	GPIO[0]	GPIO[0]
		eTimer_0	ETC[0]	ETC[0]
		DSPI_2	SCK	SCK
		SIUL	—	EIRQ[0]
74	A[1]	SIUL	GPIO[1]	GPIO[1]
		eTimer_0	ETC[1]	ETC[1]
		DSPI_2	SOUT	—
		SIUL	—	EIRQ[1]
75	G[11]	SIUL	GPIO[107]	GPIO[107]
		FlexRay	DBG3	—
		FlexPWM_0	—	FAULT[3]
76	D[10]	SIUL	GPIO[58]	GPIO[58]
		FlexPWM_0	A[0]	A[0]
		eTimer_0	—	ETC[0]
77	G[10]	SIUL	GPIO[106]	GPIO[106]
		FlexRay	DBG2	—
		DSPI_2	CS3	—
		FlexPWM_0	—	FAULT[2]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
89	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—
90	$V_{SS\_HV\_IO}$	—		
91	$V_{DD\_HV\_IO}$	—		
92	A[3]	SIUL	GPIO[3]	GPIO[3]
		eTimer_0	ETC[3]	ETC[3]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[3]	B[3]
		MC_RGM	—	ABS[2]
		SIUL	—	EIRQ[3]
93	$V_{DD\_LV\_COR}$	—		
94	$V_{SS\_LV\_COR}$	—		
95	$V_{DD\_HV\_REG\_1}$	—		
96	$V_{SS\_HV\_FLA}$	—		
97	$V_{DD\_HV\_FLA}$	—		
98	G[6]	SIUL	GPIO[102]	GPIO[102]
		FlexPWM_0	A[3]	A[3]
99	D[12]	SIUL	GPIO[60]	GPIO[60]
		FlexPWM_0	X[1]	X[1]
		LINFlexD_1	—	RXD
100	G[4]	SIUL	GPIO[100]	GPIO[100]
		FlexPWM_0	B[2]	B[2]
		eTimer_0	—	ETC[5]
101	C[13]	SIUL	GPIO[45]	GPIO[45]
		eTimer_1	ETC[1]	ETC[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
102	G[2]	SIUL	GPIO[98]	GPIO[98]
		FlexPWM_0	X[2]	X[2]
		DSPI_1	CS1	—
103	C[14]	SIUL	GPIO[46]	GPIO[46]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
134	A[9]	SIUL	GPIO[9]	GPIO[9]
		DSPI_2	CS1	—
		FlexPWM_0	B[3]	B[3]
		FlexPWM_0	—	FAULT[0]
135	$V_{DD\_LV\_COR}$	—		
136	A[13]	SIUL	GPIO[13]	GPIO[13]
		FlexPWM_0	B[2]	B[2]
		DSPI_2	—	SIN
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[12]
137	$V_{SS\_LV\_COR}$	—		
138	B[6]	SIUL	GPIO[22]	GPIO[22]
		MC_CGM	clk_out	—
		DSPI_2	CS2	—
		SIUL	—	EIRQ[18]
139	F[3]	SIUL	GPIO[83]	GPIO[83]
		DSPI_0	CS6	—
140	D[2]	SIUL	GPIO[50]	GPIO[50]
		eTimer_1	ETC[3]	ETC[3]
		FlexPWM_0	X[3]	X[3]
		FlexRay	—	CB_RX
141	FCCU_F[1]	FCCU	F[1]	F[1]
142	C[6]	SIUL	GPIO[38]	GPIO[38]
		DSPI_0	SOUT	—
		FlexPWM_0	B[1]	B[1]
		SSCM	DEBUG[6]	—
		SIUL	—	EIRQ[24]
143	A[14]	SIUL	GPIO[14]	GPIO[14]
		FlexCAN_1	TXD	—
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[13]

Table 5. Supply pins (continued)

Supply		Pin #	
Symbol	**Description**	**100 Pkg**	**144 Pkg**
V_{SS} 1V2	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	93	132
V_{DD} 1V2	VDD_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	—	135
V_{SS} 1V2	VSS_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	—	137

2.3 System pins

Table 6. System pins

Symbol	Description	Direction	Pin #	
			100 pkg	**144 pkg**
Dedicated pins				
MDO0(1)	Nexus Message Data Output — line	Output only	—	9
NMI(2)	Non Maskable Interrupt	Input only	1	1
XTAL	Input for oscillator amplifier circuit and internal clock generator	Input only	18	29
EXTAL(3)	Oscillator amplifier output	Input/Output(4)	19	30
TMS(2)	JTAG state machine control	Input only	59	87
TCK(2)	JTAG clock	Input only	60	88
JCOMP(5)	JTAG compliance select	Input only	84	123
Reset pin				
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter. This pin has medium drive strength. Output drive is open drain and must be terminated by an external resistor of value 1KOhm.(6)	Bidirectional	20	31
Test pin				
VPP TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.		74	107

1. This pad is configured for Fast (F) pad speed.
2. This pad contains a weak pull-up.
3. EXTAL is an "Output" in "crystal" mode, and is an "Input" in "ext clock" mode.
4. In XOSC Bypass Mode, the analog portion of crystal oscillator (amplifier) is disabled. An external clock can be applied at EXTAL as an input. In XOSC Normal Mode, EXTAL is an output
5. This pad contains a weak pull-down.

6. RESET output shall be considered valid only after the 3.3V supply reaches its stable value.

None of system pins (except RESET) provides an open drain output.

2.4 Pin muxing

Table 7 defines the pin list and muxing for this device.

Each entry of *Table 7* shows all the possible configurations for each pin, via the alternate functions. The default function assigned to each pin after reset is indicated by ALT0.

Note: Pins labeled "NC" are to be left unconnected. Any connection to an external circuit or voltage may cause unpredictable device behavior or damage.

Pins labeled "Reserved" are to be tied to ground. Not doing so may cause unpredictable device behavior.

Table 7. Pin muxing

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
Port A											
A[0]	PCR[0]	SIUL	GPIO[0]	ALT0	GPIO[0]	—	Pull down	M	S	51	73
		eTimer_0	ETC[0]	ALT1	ETC[0]	PSMI[35]; PADSEL=0					
		DSPI_2	SCK	ALT2	SCK	PSMI[1]; PADSEL=0					
		SIUL	—	—	EIRQ[0]	—					
A[1]	PCR[1]	SIUL	GPIO[1]	ALT0	GPIO[1]	—	Pull down	M	S	52	74
		eTimer_0	ETC[1]	ALT1	ETC[1]	PSMI[36]; PADSEL=0					
		DSPI_2	SOUT	ALT2	—	—					
		SIUL	—	—	EIRQ[1]	—					
A[2]	PCR[2]	SIUL	GPIO[2]	ALT0	GPIO[2]	—	Pull down	M	S	57	84
		eTimer_0	ETC[2]	ALT1	ETC[2]	PSMI[37]; PADSEL=0					
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=0					
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=0					
		MC_RGM	—	—	ABS[0]	—					
		SIUL	—	—	EIRQ[2]	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
B[9]	PCR[25]	SIUL	—	ALT0	GPI[25]	—	—	—	—	35	52
		ADC_0 ADC_1	—	—	AN[11](3)	—					
B[10]	PCR[26]	SIUL	—	ALT0	GPI[26]	—	—	—	—	36	53
		ADC_0 ADC_1	—	—	AN[12](3)	—					
B[11]	PCR[27]	SIUL	—	ALT0	GPI[27]	—	—	—	—	37	54
		ADC_0 ADC_1	—	—	AN[13](3)	—					
B[12]	PCR[28]	SIUL	—	ALT0	GPI[28]	—	—	—	—	38	55
		ADC_0 ADC_1	—	—	AN[14](3)	—					
B[13]	PCR[29]	SIUL	—	ALT0	GPI[29]	—	—	—	—	43	60
		LINFlex_1	—	—	RXD	PSMI[32]; PADSEL=0					
		ADC_1	—	—	AN[0](3)	—					
B[14]	PCR[30]	SIUL	—	ALT0	GPI[30]	—	—	—	—	44	64
		eTimer_0	—	—	ETC[4]	PSMI[7]; PADSEL=2					
		SIUL	—	—	EIRQ[19]	—					
		ADC_1	—	—	AN[1](3)	—					
B[15]	PCR[31]	SIUL	—	ALT0	GPI[31]	—	—	—	—	—	62
		SIUL	—	—	EIRQ[20]	—					
		ADC_1	—	—	AN[2](3)	—					
Port C											
C[0]	PCR[32]	SIUL	—	ALT0	GPI[32]	—	—	—	—	45	66
		ADC_1	—	—	AN[3](3)	—					
C[1]	PCR[33]	SIUL	—	ALT0	GPI[33]	—	—	—	—	—	41
		ADC_0	—	—	AN[2](3)	—					
C[2]	PCR[34]	SIUL	—	ALT0	GPI[34]	—	—	—	—	—	45
		ADC_0	—	—	AN[3](3)	—					

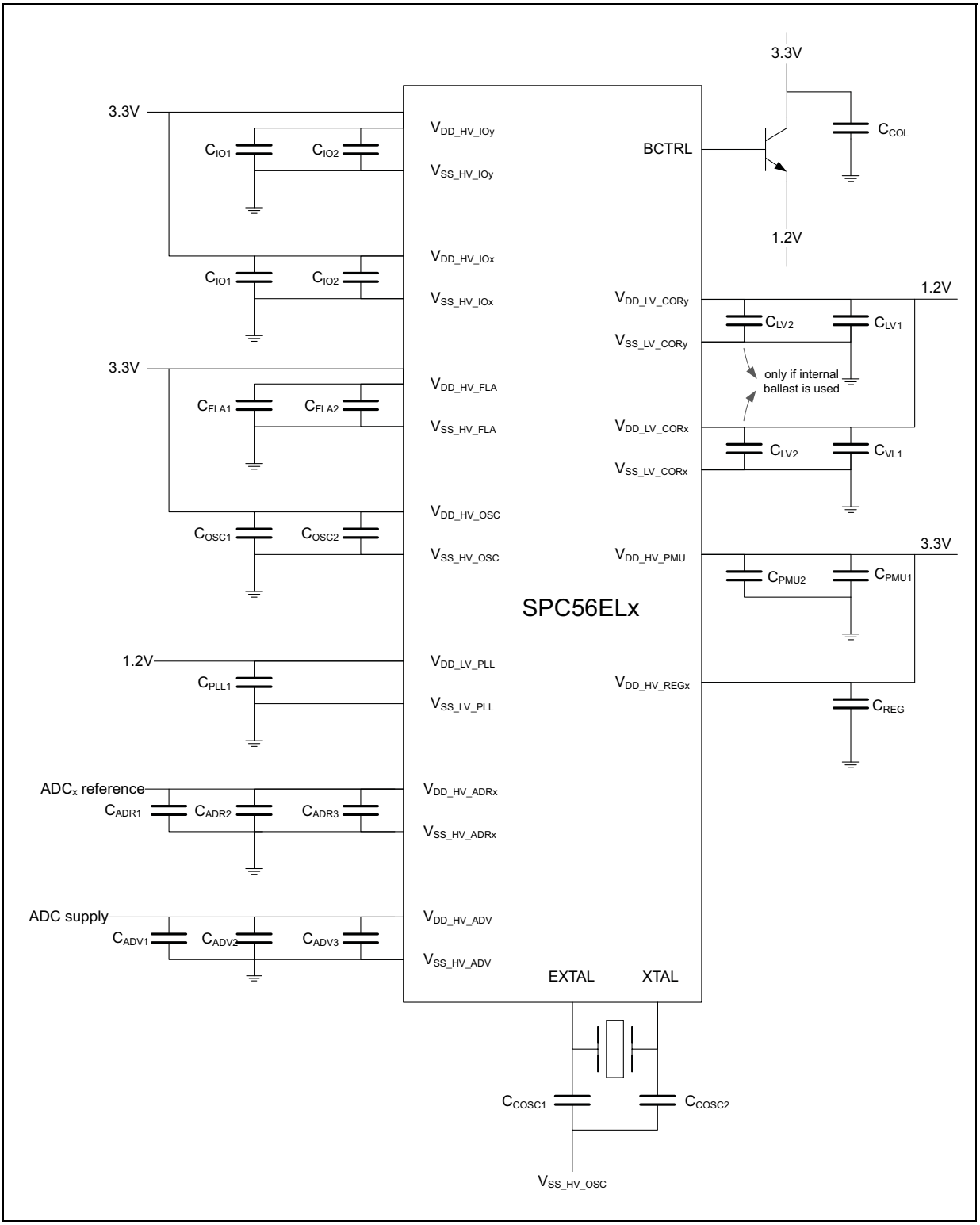
Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
C[12]	PCR[44]	SIUL	GPIO[44]	ALT0	GPIO[44]	—	Pull down	M	S	56	82
		eTimer_0	ETC[5]	ALT1	ETC[5]	PSMI[8]; PADSEL=0					
		DSPI_2	CS3	ALT2	—	—					
C[13]	PCR[45]	SIUL	GPIO[45]	ALT0	GPIO[45]	—	Pull down	M	S	71	101
		eTimer_1	ETC[1]	ALT1	ETC[1]	PSMI[10]; PADSEL=0					
		CTU_0	—	—	EXT_IN	PSMI[0]; PADSEL=0					
		FlexPWM_0	—	—	EXT_SYNC	PSMI[15]; PADSEL=0					
C[14]	PCR[46]	SIUL	GPIO[46]	ALT0	GPIO[46]	—	Pull down	M	S	72	103
		eTimer_1	ETC[2]	ALT1	ETC[2]	PSMI[11]; PADSEL=1					
		CTU_0	EXT_TGR	ALT2	—	—					
C[15]	PCR[47]	SIUL	GPIO[47]	ALT0	GPIO[47]	—	Pull down	SYM	S	85	124
		FlexRay	CA_TR_EN	ALT1	—	—					
		eTimer_1	ETC[0]	ALT2	ETC[0]	PSMI[9]; PADSEL=1					
		FlexPWM_0	A[1]	ALT3	A[1]	PSMI[21]; PADSEL=1					
		CTU_0	—	—	EXT_IN	PSMI[0]; PADSEL=1					
		FlexPWM_0	—	—	EXT_SYNC	PSMI[15]; PADSEL=1					
Port D											
D[0]	PCR[48]	SIUL	GPIO[48]	ALT0	GPIO[48]	—	Pull down	SYM	S	86	125
		FlexRay	CA_TX	ALT1	—	—					
		eTimer_1	ETC[1]	ALT2	ETC[1]	PSMI[10]; PADSEL=1					
		FlexPWM_0	B[1]	ALT3	B[1]	PSMI[25]; PADSEL=1					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
D[1]	PCR[49]	SIUL	GPIO[49]	ALT0	GPIO[49]	—	Pull down	M	S	3	3
		eTimer_1	ETC[2]	ALT2	ETC[2]	PSMI[11]; PADSEL=2					
		CTU_0	EXT_TGR	ALT3	—	—					
		FlexRay	—	—	CA_RX	—					
D[2]	PCR[50]	SIUL	GPIO[50]	ALT0	GPIO[50]	—	Pull down	M	S	—	140
		eTimer_1	ETC[3]	ALT2	ETC[3]	PSMI[12]; PADSEL=1					
		FlexPWM_0	X[3]	ALT3	X[3]	PSMI[30]; PADSEL=0					
		FlexRay	—	—	CB_RX	—					
D[3]	PCR[51]	SIUL	GPIO[51]	ALT0	GPIO[51]	—	Pull down	SYM	S	89	128
		FlexRay	CB_TX	ALT1	—	—					
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=1					
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=2					
D[4]	PCR[52]	SIUL	GPIO[52]	ALT0	GPIO[52]	—	Pull down	SYM	S	90	129
		FlexRay	CB_TR_EN	ALT1	—	—					
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=2					
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=2					
D[5]	PCR[53]	SIUL	GPIO[53]	ALT0	GPIO[53]	—	Pull down	M	S	22	33
		DSPI_0	CS3	ALT1	—	—					
		FlexPWM_0	—	—	FAULT[2]	PSMI[18]; PADSEL=0					
D[6]	PCR[54]	SIUL	GPIO[54]	ALT0	GPIO[54]	—	Pull down	M	S	23	34
		DSPI_0	CS2	ALT1	—	—					
		FlexPWM_0	X[3]	ALT3	X[3]	PSMI[30]; PADSEL=1					
		FlexPWM_0	—	—	FAULT[1]	PSMI[17]; PADSEL=1					

Figure 4. Decoupling capacitors



2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.
3. Data based on characterization results, not tested in production.

3.8 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 16. Latch-up results

No.	Symbol		Parameter	Conditions	Class
1	LU	SR	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.9 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- High power regulator HPREG1 (internal ballast to support core current)
- High power regulator HPREG2 (external NPN to support core current)
- Low voltage detector (LVD_MAIN_1) for 3.3 V supply to IO (V_{DDIO})
- Low voltage detector (LVD_MAIN_2) for 3.3 V supply (V_{DDREG})
- Low voltage detector (LVD_MAIN_3) for 3.3 V flash supply ($V_{DDFLASH}$)
- Low voltage detector (LVD_DIG_MAIN) for 1.2 V digital core supply (HPV_{DD})
- Low voltage detector (LVD_DIG_BKUP) for the self-test of LVD_DIG_MAIN
- High voltage detector (HVD_DIG_MAIN) for 1.2 V digital CORE supply (HPV_{DD})
- High voltage detector (HVD_DIG_BKUP) for the self-test of HVD_DIG_MAIN.
- Power on Reset (POR)

HPREG1 uses an internal ballast to support the core current. HPREG2 is used only when external NPN transistor is present on board to supply core current. The SPC56XL70 always powers up using HPREG1 if an external NPN transistor is present. Then the SPC56XL70 makes a transition from HPREG1 to HPREG2. This transition is dynamic. Once HPREG2 is fully operational, the controller part of HPREG1 is switched off. The following bipolar transistors are supported:

- BCP68 from ON Semiconductor
- BCX68 from Infineon

Table 17. Recommended operating characteristics

Symbol	Parameter	Value	Unit
$h_{FE}(\beta)$	DC current gain (Beta)	85 - 375	—
P_D	Maximum power dissipation @ T_A=25°C(1)	1.5	W

considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to *Equation 7*:

Equation 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Equation 9

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. *Equation 10* must be respected (charge balance assuming now C_S already charged at V_{A1}):

3.20.2 WKUP/NMI timing

Table 35. WKUP/NMI glitch filter

No.	Symbol		Parameter	Min	Typ	Max	Unit
1	W_{FNMI}	D	NMI pulse width that is rejected	—	—	45	ns
2	W_{NFNMI}	D	NMI pulse width that is passed	205	—	—	ns

3.20.3 IEEE 1149.1 JTAG interface timing

Table 36. JTAG pin AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time	—	62.5	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at $V_{DDE}/2$)	—	40	60	%
3	$t_{TCKRISE}$	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	D	TCK low to TDO data valid	—	—	20	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	D	TCK low to TDO high impedance	—	—	20	ns
11	t_{BSDV}	D	TCK falling edge to output valid	—	—	50	ns
12	t_{BSDVZ}	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
13	t_{BSDHZ}	D	TCK falling edge to output high impedance	—	—	50	ns
14	t_{BSDST}	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
15	t_{BSDHT}	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

Figure 23. JTAG test clock input timing

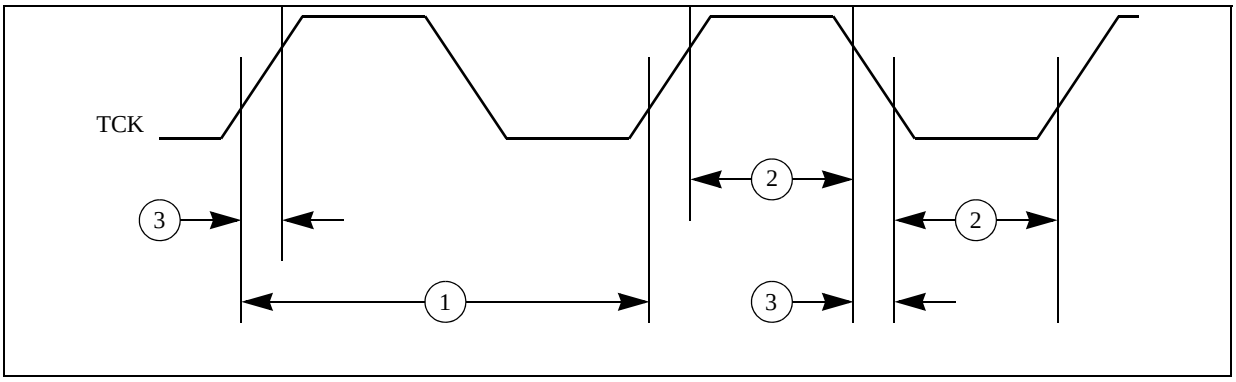
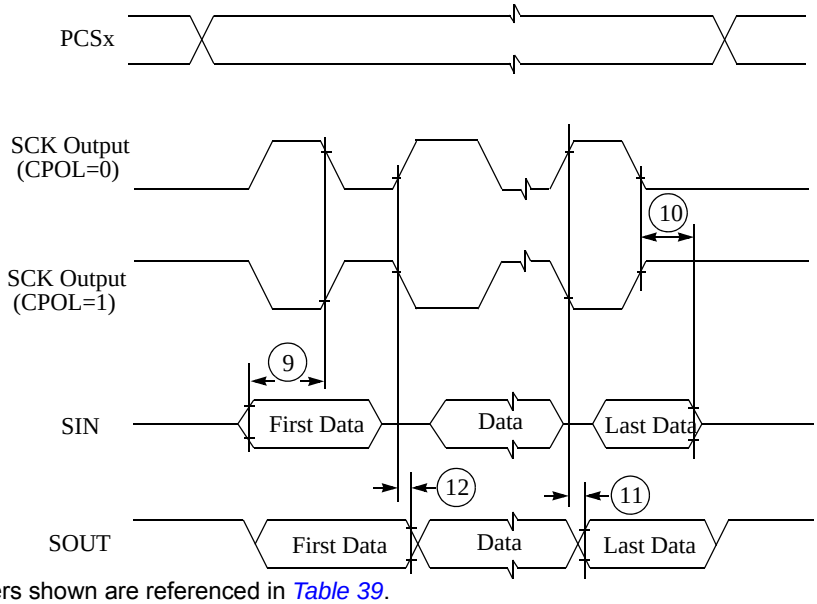
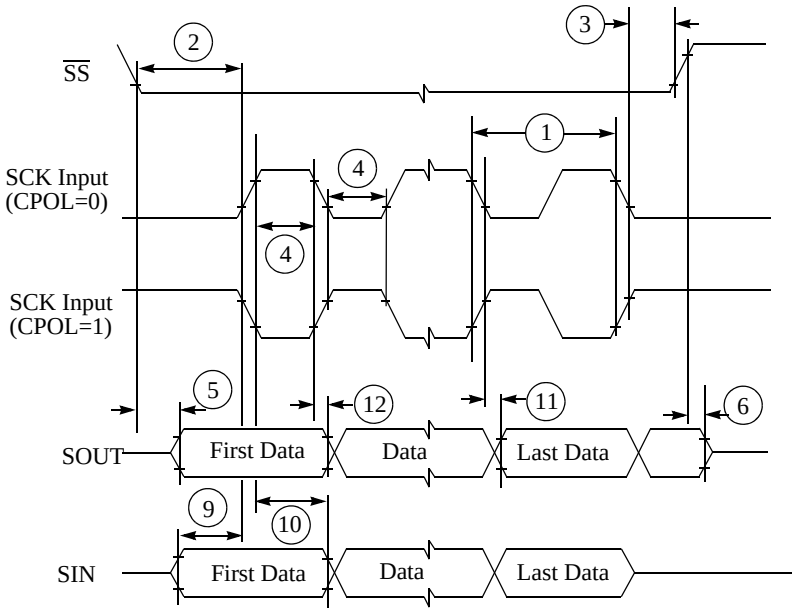


Figure 31. DSPI classic SPI timing — master, CPHA = 1



Note: The numbers shown are referenced in *Table 39*.

Figure 32. DSPI classic SPI timing — slave, CPHA = 0



Note: The numbers shown are referenced in *Table 39*.