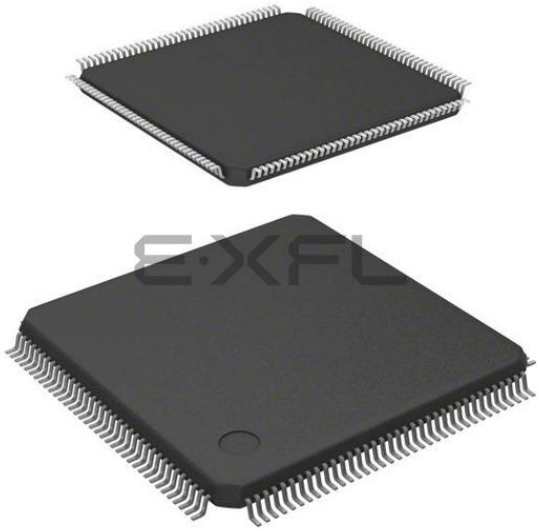

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56el70l5cbfy

1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the devices.

This document provides electrical specifications, pin assignments, and package diagrams for the SPC56EL70x/SPC564L70x series of microcontroller units (MCUs). For functional characteristics, see the SPC56XL70 Microcontroller Reference Manual. For use of the SPC56XL70 in a fail-safe system according to safety standard ISO26262, see the Safety Application Guide for SPCEL70.

1.2 Description

The SPC56EL70x/SPC564L70x series microcontrollers are system-on-chip devices that are built on Power Architecture technology and contain enhancements that improve the architecture's fit in embedded applications, include additional instruction support for digital signal processing (DSP) and integrate technologies such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system.

The SPC56EL70x/SPC564L70x family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address electrical hydraulic power steering (EHPS), electric power steering (EPS) and airbag applications. The advanced and cost-efficient host processor core of the SPC56XL70 automotive controller family complies with the Power Architecture embedded category. It operates at speeds as high as 120 MHz and offers high-performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users' implementations.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0 to 8 bytes data length
  - Programmable bit rate as fast as 1Mbit/s
- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as receive or transmit buffer, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
-

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
64	B[14]	SIUL	—	GPIO[30]
		eTimer_0	—	ETC[4]
		SIUL	—	EIRQ[19]
		ADC_1	—	AN[1]
65	E[11]	SIUL	—	GPIO[75]
		ADC_1	—	AN[4]
66	C[0]	SIUL	—	GPIO[32]
		ADC_1	—	AN[3]
67	E[12]	SIUL	—	GPIO[76]
		ADC_1	—	AN[6]
68	E[0]	SIUL	—	GPIO[64]
		ADC_1	—	AN[5]
69	BCTRL	—		
70	$V_{DD_LV_COR}$	—		
71	$V_{SS_LV_COR}$	—		
72	$V_{DD_HV_PMU}$	—		
73	A[0]	SIUL	GPIO[0]	GPIO[0]
		eTimer_0	ETC[0]	ETC[0]
		DSPI_2	SCK	SCK
		SIUL	—	EIRQ[0]
74	A[1]	SIUL	GPIO[1]	GPIO[1]
		eTimer_0	ETC[1]	ETC[1]
		DSPI_2	SOUT	—
		SIUL	—	EIRQ[1]
75	G[11]	SIUL	GPIO[107]	GPIO[107]
		FlexRay	DBG3	—
		FlexPWM_0	—	FAULT[3]
76	D[10]	SIUL	GPIO[58]	GPIO[58]
		FlexPWM_0	A[0]	A[0]
		eTimer_0	—	ETC[0]
77	G[10]	SIUL	GPIO[106]	GPIO[106]
		FlexRay	DBG2	—
		DSPI_2	CS3	—
		FlexPWM_0	—	FAULT[2]

		SIUL	GPIO[59]	GPIO[59]
78	D[11]	FlexPWM_0	B[0]	B[0]
		eTimer_0	—	ETC[1]
		SIUL	GPIO[105]	GPIO[105]
		FlexRay	DBG1	—
79	G[9]	DSPI_1	CS1	—
		FlexPWM_0	—	FAULT[1]
		SIUL	—	EIRQ[29]
		SIUL	GPIO[43]	GPIO[43]
80	C[11]	eTimer_0	ETC[4]	ETC[4]
		DSPI_2	CS2	—
		SIUL	GPIO[104]	GPIO[104]
		FlexRay	DBG0	—
81	G[8]	DSPI_0	CS1	—
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[21]
		SIUL	GPIO[44]	GPIO[44]
82	C[12]	eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
83	G[7]	SIUL	GPIO[103]	GPIO[103]
		FlexPWM_0	B[3]	B[3]
		SIUL	GPIO[2]	GPIO[2]
		eTimer_0	ETC[2]	ETC[2]
84	A[2]	FlexPWM_0	A[3]	A[3]
		DSPI_2	—	SIN
		MC_RGM	—	ABS[0]
		SIUL	—	EIRQ[2]
		SIUL	GPIO[101]	GPIO[101]
85	G[5]	FlexPWM_0	X[3]	X[3]
		DSPI_2	CS3	—
86	B[5]	SIUL	GPIO[21]	GPIO[21]
		JTAGC	—	TDI

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
D[1]	PCR[49]	SIUL	GPIO[49]	ALT0	GPIO[49]	—	Pull down	M	S	3	3
		eTimer_1	ETC[2]	ALT2	ETC[2]	PSMI[11]; PADSEL=2					
		CTU_0	EXT_TGR	ALT3	—	—					
		FlexRay	—	—	CA_RX	—					
D[2]	PCR[50]	SIUL	GPIO[50]	ALT0	GPIO[50]	—	Pull down	M	S	—	140
		eTimer_1	ETC[3]	ALT2	ETC[3]	PSMI[12]; PADSEL=1					
		FlexPWM_0	X[3]	ALT3	X[3]	PSMI[30]; PADSEL=0					
		FlexRay	—	—	CB_RX	—					
D[3]	PCR[51]	SIUL	GPIO[51]	ALT0	GPIO[51]	—	Pull down	SYM	S	89	128
		FlexRay	CB_TX	ALT1	—	—					
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=1					
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=2					
D[4]	PCR[52]	SIUL	GPIO[52]	ALT0	GPIO[52]	—	Pull down	SYM	S	90	129
		FlexRay	CB_TR_EN	ALT1	—	—					
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=2					
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=2					
D[5]	PCR[53]	SIUL	GPIO[53]	ALT0	GPIO[53]	—	Pull down	M	S	22	33
		DSPI_0	CS3	ALT1	—	—					
		FlexPWM_0	—	—	FAULT[2]	PSMI[18]; PADSEL=0					
D[6]	PCR[54]	SIUL	GPIO[54]	ALT0	GPIO[54]	—	Pull down	M	S	23	34
		DSPI_0	CS2	ALT1	—	—					
		FlexPWM_0	X[3]	ALT3	X[3]	PSMI[30]; PADSEL=1					
		FlexPWM_0	—	—	FAULT[1]	PSMI[17]; PADSEL=1					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
Port H											
H[0]	PCR[112]	SIUL	GPIO[112]	ALT0	GPIO[112]	—	Pull down	F	S	—	—
		NPC	MDO[7]	ALT2	—	—					
H[1]	PCR[113]	SIUL	GPIO[113]	ALT0	GPIO[113]	—	Pull down	F	S	—	—
		NPC	MDO[6]	ALT2	—	—					
H[2]	PCR[114]	SIUL	GPIO[114]	ALT0	GPIO[114]	—	Pull down	F	S	—	—
		NPC	MDO[5]	ALT2	—	—					
H[3]	PCR[115]	SIUL	GPIO[115]	ALT0	GPIO[115]	—	Pull down	F	S	—	—
		NPC	MDO[4]	ALT2	—	—					
H[4]	PCR[116]	SIUL	GPIO[116]	ALT0	GPIO[116]	—	Pull down	M	S	—	—
		FlexPWM_1	X[0]	ALT1	X[0]	—					
		eTimer_2	ETC[0]	ALT2	ETC[0]	PSMI[39]; PADSEL=0					
H[5]	PCR[117]	SIUL	GPIO[117]	ALT0	GPIO[117]	—	Pull down	M	S	—	—
		FlexPWM_1	A[0]	ALT1	A[0]	—					
		DSPI_0	CS4	ALT3	—	—					
H[6]	PCR[118]	SIUL	GPIO[118]	ALT0	GPIO[118]	—	Pull down	M	S	—	—
		FlexPWM_1	B[0]	ALT1	B[0]	—					
		DSPI_0	CS5	ALT3	—	—					
H[7]	PCR[119]	SIUL	GPIO[119]	ALT0	GPIO[119]	—	Pull down	M	S	—	—
		FlexPWM_1	X[1]	ALT1	X[1]	—					
		eTimer_2	ETC[1]	ALT2	ETC[1]	PSMI[40]; PADSEL=0					
H[8]	PCR[120]	SIUL	GPIO[120]	ALT0	GPIO[120]	—	Pull down	M	S	—	—
		FlexPWM_1	A[1]	ALT1	A[1]	—					
		DSPI_0	CS6	ALT3	—	—					
H[9]	PCR[121]	SIUL	GPIO[121]	ALT0	GPIO[121]	—	Pull down	M	S	—	—
		FlexPWM_1	B[1]	ALT1	B[1]	—					
		DSPI_0	CS7	ALT3	—	—					
H[10]	PCR[122]	SIUL	GPIO[122]	ALT0	GPIO[122]	—	Pull down	M	S	—	—
		FlexPWM_1	X[2]	ALT1	X[2]	—					
		eTimer_2	ETC[2]	ALT2	ETC[2]	—					

Table 8. Absolute maximum ratings(1) (continued)

Symbol		Parameter	Conditions	Min	Max	Unit
$V_{SS_HV_ADR0}$ $V_{SS_HV_ADR1}$	SR	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	–0.1	0.1	V
$V_{DD_HV_ADV}$	SR	3.3 V ADC supply voltage	—	–0.3	4.5(3), (4)	V
$V_{SS_HV_ADV}$	SR	3.3 V ADC supply ground	—	–0.1	0.1	V
TV_{DD}	SR	Supply ramp rate	—	3.0×10^{-6} (3.0 V/sec)	0.5 V/µs	V/µs
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS_HV_IOx}$)or $V_{ss_HV_ADRx}$	Valid only for ADC pins	–0.3	6.0(4)	V
			Relative to V_{DD}	–0.3	V_{DD} + 0.3(4), (5)	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{STG}	SR	Storage temperature	—	–55	150	°C

1. Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability or cause permanent damage to the device.
2. Any voltage between operating condition and absolute max rating can be sustained for maximum cumulative time of 10 hours.
3. Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
4. Internal structures hold the input voltage less than the maximum voltage on all pads powered by VDDE supplies, if the maximum injection current specification is met (2 mA for all pins) and VDDE is within the operating voltage specifications.
5. V_{DD} has to be considered equal to $V_{DD_HV_ADRx}$ in case of ADC pins, whilst it is $V_{DD_HV_IOx}$ for any other pin.

3.3 Recommended operating conditions

Table 9. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Min(1)	Max	Unit
$V_{DD_HV_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.63	V
$V_{SS_HV_REG}$	SR	3.3 V voltage regulator reference voltage	—	0	0	V
$V_{DD_HV_IOx}$	SR	3.3 V input/output supply voltage	—	3.0	3.63	V
$V_{SS_HV_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD_HV_FLA}$	SR	3.3 V flash supply voltage	—	3.0	3.63	V
$V_{SS_HV_FLA}$	SR	Flash memory ground	—	0	0	V
$V_{DD_HV_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.63	V
$V_{SS_HV_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD_HV_ADR0}$(2),(3) $V_{DD_HV_ADR1}$	SR	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	4.5 to 5.5 or 3.0 to 3.63		V

Table 9. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Min(1)	Max	Unit
$V_{DD_HV_ADV}$	SR	3.3 V ADC supply voltage	—	3.0	3.63	V
$V_{SS_HV_AD0}$ $V_{SS_HV_AD1}$	SR	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	0	0	V
$V_{SS_HV_ADV}$	SR	3.3 V ADC supply ground	—	0	0	V
$V_{DD_LV_REGCOR}$(4)	SR	Internal supply voltage	—	—	—	V
$V_{SS_LV_REGCOR}$(5)	SR	Internal reference voltage	—	0	0	V
$V_{DD_LV_CORx}$(2)	SR	Internal supply voltage	—	—	—	V
$V_{SS_LV_CORx}$(3)	SR	Internal reference voltage	—	0	0	V
$V_{DD_LV_PLL}$(2)	SR	Internal supply voltage	—	—	—	V
$V_{SS_LV_PLL}$(3)	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	f_{CPU} 120 MHz	–40	125	°C
T_J	SR	Junction temperature under bias	—	–40	150	°C

1. Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. $V_{DD_HV_ADR0}$ and $V_{DD_HV_ADR1}$ cannot be operated at different voltages, and need to be supplied by the same voltage source.
3. VDD_HV_ADRx must always be applied and should be stable before LBIST starts. If this supply is not above its absolute minimum level, LBIST operations can fail.
4. Can be connected to emitter of external NPN. Low voltage supplies are not under user control. They are produced by an on-chip voltage regulator.
5. For the device to function properly, the low voltage grounds ($V_{SS_LV_xxx}$) must be shorted to high voltage grounds ($V_{SS_HV_xxx}$) and the low voltage supply pins ($V_{DD_LV_xxx}$) must be connected to the external ballast emitter, if one is used.

3.4 Decoupling capacitors

The internal voltage regulator requires an external NPN ballast and some additional decoupling capacitors. These capacitors shall be placed on the board as close as possible to the associated pin.

Table 10. Decoupling capacitors

Symbol		Parameter	Conditions(1)	Value			Unit
				Min	Typ	Max	
C_{COL}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Max ESR = 100 mΩ.		20		µF
C_{LV1}	SR	External decoupling / stability capacitor	Sum of C_{LV1} placed close to $V_{DD}/V_{SS_LV_CORy}$ pairs(2).	12µF		40µF	µF
C_{LV2}	SR	External decoupling / stability capacitor	Sum of C_{LV2} placed close to $V_{DD}/V_{SS_LV_CORy}$ pairs shall be between 300 nF and 900 nF.		100(2)		nF
C_{PMU1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		10		µF

Table 18. Voltage regulator electrical specifications (continued)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
—	D	Digital supply high voltage detector upper threshold	Before a destructive reset initialization phase completion	1.355	—	1.495	V
			After a destructive reset initialization phase completion	1.39	—	1.47	
—	D	Digital supply high voltage detector lower threshold	Before a destructive reset initialization phase completion	1.315	—	1.455	V
			After a destructive reset initialization phase completion	1.35	—	1.38	
—	D	Digital supply low voltage detector lower threshold	Before a destructive reset initialization phase completion	1.080	—	1.226	V
—	D	Digital supply low voltage detector lower threshold	After a destructive reset initialization phase completion	1.080	—	1.140	V
—	D	Digital supply low voltage detector upper threshold	After a destructive reset initialization phase completion	1.16	—	1.22	V
—	D	Digital supply low voltage detector upper threshold	Before a destructive reset initialization phase completion	1.16	—	1.306	V
—	D	POR rising/ falling supply threshold voltage	—	1.6	—	2.6	V
—	SR	Supply ramp rate	—	3	—	0.5×10^6	V/s
—	D	LVD_MAIN: Time constant of RC filter at LVD input	3.3V noise rejection at the input of LVD comparator	1.1	—	—	µs
—	D	HVD_DIG: Time constant of RC filter at LVD input	1.2V noise rejection at the input of LVD comparator	0.1	—	—	µs
—	D	LVD_DIG: Time constant of RC filter at LVD input	1.2V noise rejection at the input of LVD comparator	0.1	—	—	µs

Figure 7. Main oscillator electrical characteristics

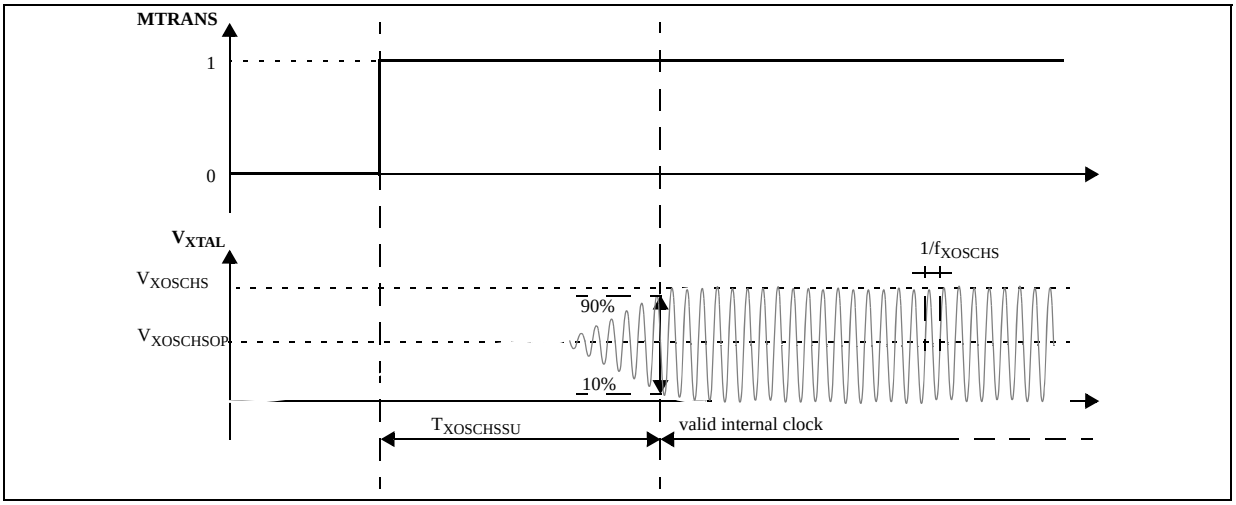
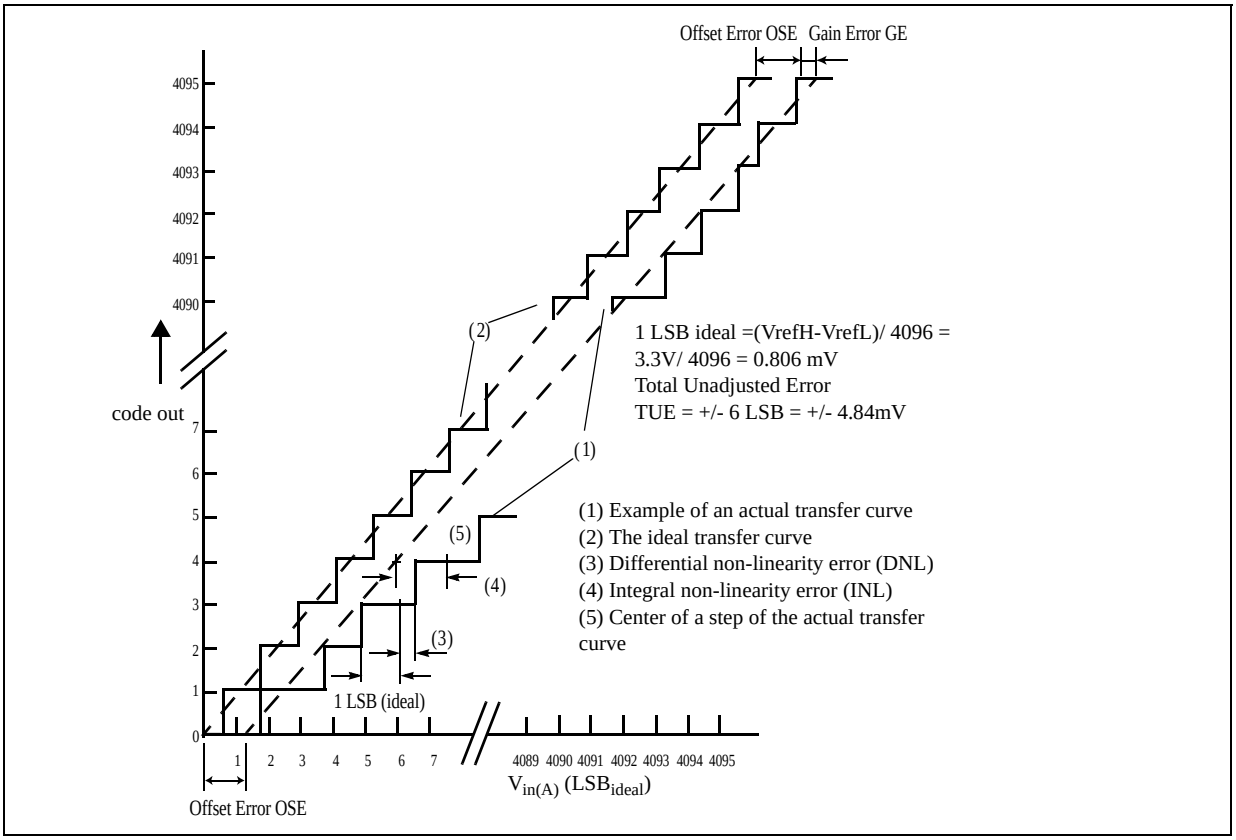


Table 22. Main oscillator electrical characteristics

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
f_{XOSCHS}	SR	Oscillator frequency	—	4.0	—	40.0	MHz
$g_{mXOSCHS}$	P	Oscillator transconductance	V_{DD} = 3.3 V ±10%	4.5	—	13.25	mA/V
V_{XOSCHS}	D	Oscillation amplitude	f_{OSC} = 4, 8, 10, 12, 16 MHz	1.3	—	—	V
			f_{OSC} = 40 MHz	1.1	—	—	
$V_{XOSCHSOP}$	D	Oscillation operating point	—	—	0.82	—	V
I_{XOSCHS}	D	Oscillator consumption	—	—	—	3.5	mA
$T_{XOSCHSSU}$	T	Oscillator start-up time	f_{OSC} = 4, 8, 10, 12 MHz[2]	—	—	6	ms
			f_{OSC} = 16, 40 MHz[2]	—	—	2	
V_{IH}	SR	Input high level CMOS Schmitt Trigger	Oscillator bypass mode	0.65 × V_{DD}	—	V_{DD} + 0.4	V
V_{IL}	SR	Input low level CMOS Schmitt Trigger	Oscillator bypass mode	–0.4	—	0.35 × V_{DD}	V

1. V_{DD} = 3.3 V ±10%, T_J = –40 to +150 °C, unless otherwise specified.
2. The recommended configuration for maximizing the oscillator margin are:
   XOSC_MARGIN = 0 for 4 MHz quartz
   XOSC_MARGIN = 1 for 8/16/40 MHz quartz

Figure 8. ADC characteristics and error definitions



3.15.1 Input Impedance and ADC Accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 k is obtained (R_{EQ} = 1 / (fS C_{P2} + C_S), where fs represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of R_S + R_F + R_L + R_{SW} + R_{AD}, the external circuit must be designed to respect the *Equation 4*:

considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$_1 = R_{SW} + R_{AD} \quad \frac{C_P \quad C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Equation 6

$$_1 \quad R_{SW} + R_{AD} \quad C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to *Equation 7*:

Equation 7

$$V_{A1} \quad C_S + C_{P1} + C_{P2} \quad = V_A \quad C_{P1} + C_{P2}$$

A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$_2 \quad R_L \quad C_S + C_{P1} + C_{P2}$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Equation 9

$$10 \quad _2 = 10 \quad R_L \quad C_S + C_{P1} + C_{P2} \quad T_S$$

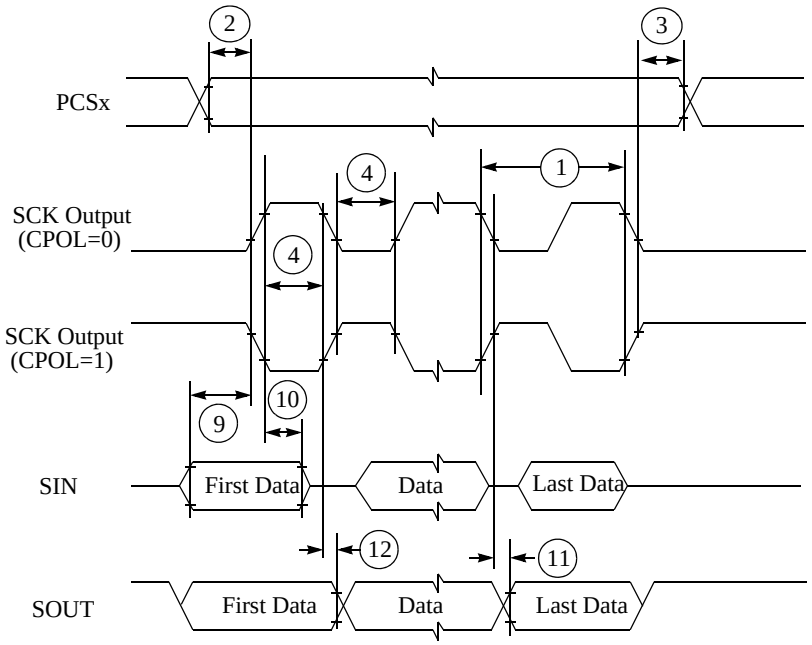
Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. *Equation 10* must be respected (charge balance assuming now C_S already charged at V_{A1}):

Table 39. DSPI timing (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
12	t_{HO}	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
				Slave	6	—	
				Master (MTFE = 1, CPHA = 0)	6	—	
				Master (MTFE = 1, CPHA = 1)	–2	—	

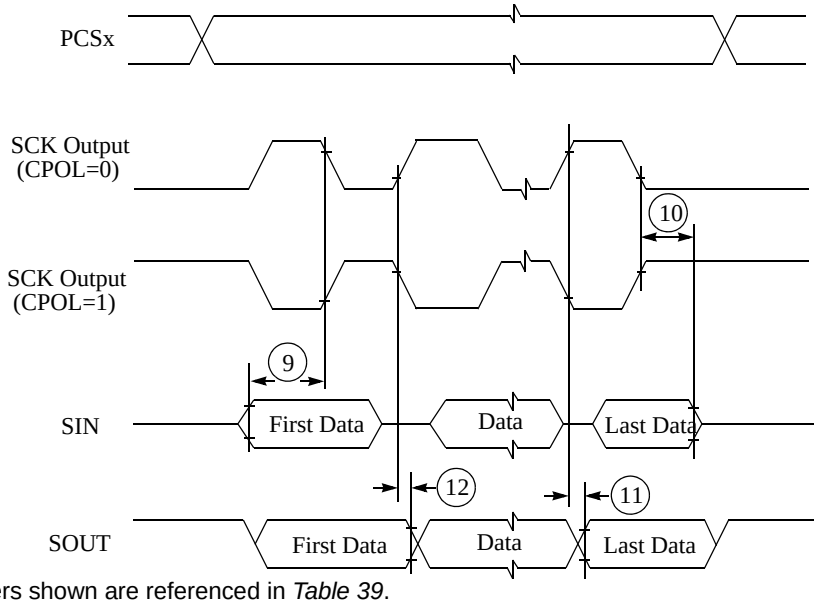
1. Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. In this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.

Figure 30. DSPI classic SPI timing — master, CPHA = 0



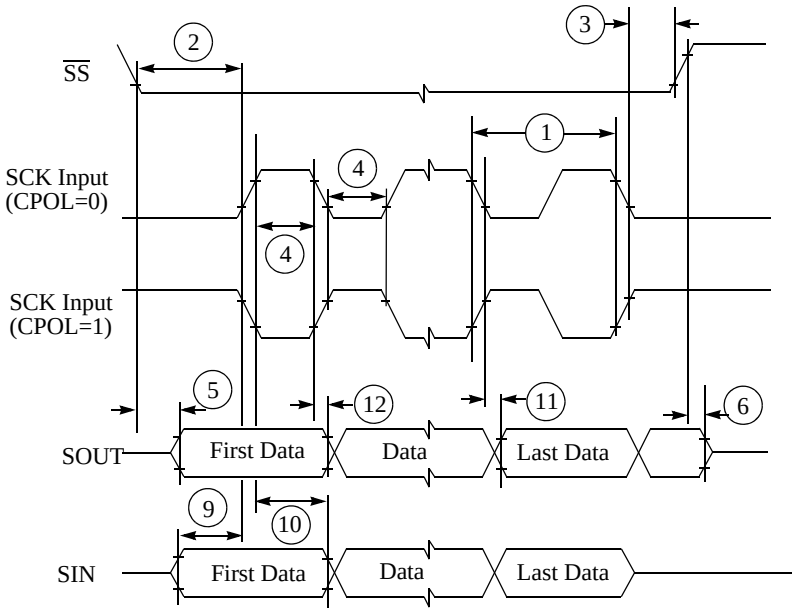
Note: The numbers shown are referenced in *Table 39*.

Figure 31. DSPI classic SPI timing — master, CPHA = 1



Note: The numbers shown are referenced in *Table 39*.

Figure 32. DSPI classic SPI timing — slave, CPHA = 0



Note: The numbers shown are referenced in *Table 39*.