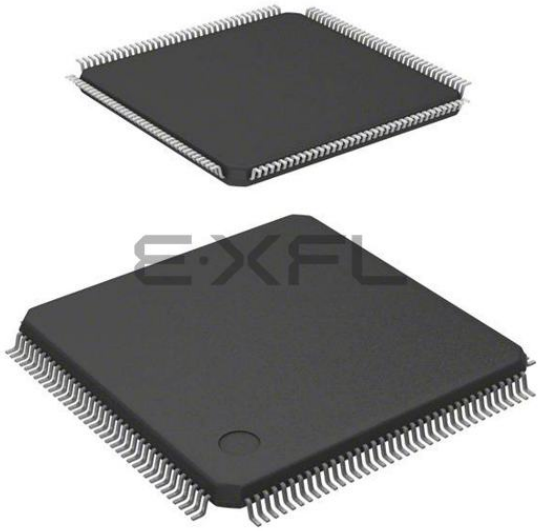

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56el70l5cbosr

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The eDMA module provides the following features:

- 16 channels supporting 8-, 16-, and 32-bit value single or block transfers
- Support variable sized queues and circular buffered queue
- Source and destination address registers independently configured to post-increment or stay constant
- Support major and minor loop offset
- Support minor and major loop done signals
- DMA task initiated either by hardware requestor or by software
- Each DMA task can optionally generate an interrupt at completion and retirement of the task
- Signal to indicate closure of last minor loop
- Transfer control descriptors mapped inside the SRAM

The eDMA controller is replicated for each processing channel.

1.5.5 On-chip flash memory with ECC

This device includes programmable, non-volatile flash memory. The non-volatile memory (NVM) can be used for instruction storage or data storage, or both. The flash memory module interfaces with the system bus through a dedicated flash memory array controller. It supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit prefetch buffers. Prefetch buffer hits allow no-wait responses. Buffer misses incur a 3 wait state response at 120 MHz.

The flash memory module provides the following features:

- 2 MB of flash memory in unique multi-partitioned hard macro
- Sectorization:
  - Partition 1 (low address): 16 KB + 16 KB + 16 KB + 16 KB
  - Partition 2 (low address): 16 KB + 16 KB + 16 KB + 16 KB
  - Partition 3 (low address): 64 KB + 64 KB
  - Partition 4 (mid address): 128 KB + 128 KB
  - Partition 5 (high address): 256 KB + 256 KB
  - Partition 6 (high address): 256 KB + 256 KB
  - Partition 7 (high address): 256 KB + 256 KB
- EEPROM emulation (in software) within same module but on different partition
- 16 KB test sector and 16 KB shadow sector for test, censorship device and user option bits
- Wait states:
  - Access time less or equal to 3 WS at 120 MHz + 4% FM (4-1-2-1 access)
  - Access time less or equal to 2 WS at 80 MHz + 4% FM
- Flash memory line 128-bit wide with 8-bit ECC on 64-bit word (total 144 bits)
- Accessed via a 64-bit wide bus for write and a 128-bit wide array for read operations
- 1-bit error correction, 2-bit error detection

1.5.6 On-chip SRAM with ECC

The SPC56XL70 SRAM provides a general-purpose single port memory.

The SIU provides the following features:

- Centralized pad control on a per-pin basis
  - Pin function selection
  - Configurable weak pull-up/down
  - Configurable slew rate control (slow/medium/fast)
  - Hysteresis on GPIO pins
  - Configurable automatic safe mode pad control
- Input filtering for external interrupts

1.5.23 Non-maskable interrupt (NMI)

The non-maskable interrupt with de-glitching filter supports high-priority core exceptions.

1.5.24 Boot assist module (BAM)

The BAM is a block of read-only memory with hard-coded content. The BAM program is executed only if serial booting mode is selected via boot configuration pins.

The BAM provides the following features:

- Enables booting via serial mode (FlexCAN or LINFlex-UART)
- Supports programmable 64-bit password protection for serial boot mode
- Supports serial bootloading of either Power Architecture code (default) or VLE code
- Automatic switch to serial boot mode if internal flash memory is blank or invalid

1.5.25 System status and configuration module (SSCM)

The SSCM on this device features the following:

- System configuration and status
- Debug port status and debug port enable
- Multiple boot code starting locations out of reset through implementation of search for valid Reset Configuration Half Word
- Sets up the MMU to allow user boot code to execute as either Power Architecture code (default) or as VLE code out of flash memory
- Triggering of device self-tests during reset phase of device boot

1.5.26 FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth.

The CTU implements the following features:

- Cross triggering between ADC, FlexPWM, eTimer, and external pins
- Double buffered trigger generation unit with as many as 8 independent triggers generated from external triggers
- Maximum operating frequency less than or equal to 120 MHz
- Trigger generation unit configurable in sequential mode or in triggered mode
- Trigger delay unit to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with as many as 24 ADC commands
- Each trigger capable of generating consecutive commands
- ADC conversion command allows control of ADC channel from each ADC, single or synchronous sampling, independent result queue selection
- DMA support with safety features

1.5.35 Cyclic redundancy checker (CRC) unit

The CRC module is a configurable multiple data flow unit to compute CRC signatures on data written to its input register.

The CRC unit has the following features:

- 3 sets of registers to allow 3 concurrent contexts with possibly different CRC computations, each with a selectable polynomial and seed
- Computes 16- or 32-bit wide CRC on the fly (single-cycle computation) and stores result in internal register.
  The following standard CRC polynomials are implemented:
  - $x^8 + x^4 + x^3 + x^2 + 1$ [8-bit CRC]
  - $x^{16} + x^{12} + x^5 + 1$ [16-bit CRC-CCITT]
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$ [32-bit CRC-ethernet(32)]
- Key engine to be coupled with communication periphery where CRC application is added to allow implementation of safe communication protocol
- Offloads core from cycle-consuming CRC and helps checking configuration signature for safe start-up or periodic procedures
- CRC unit connected as peripheral bus on internal peripheral bus
- DMA support

1.5.36 Redundancy control and checker unit (RCCU)

The RCCU checks all outputs of the sphere of replication (addresses, data, control signals). It has the following features:

- Duplicated module to guarantee highest possible diagnostic coverage (check of checker)
- Multiple times replicated IPs are used as checkers on the SoR outputs

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
89	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—
90	$V_{SS\_HV\_IO}$	—		
91	$V_{DD\_HV\_IO}$	—		
92	A[3]	SIUL	GPIO[3]	GPIO[3]
		eTimer_0	ETC[3]	ETC[3]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[3]	B[3]
		MC_RGM	—	ABS[2]
		SIUL	—	EIRQ[3]
93	$V_{DD\_LV\_COR}$	—		
94	$V_{SS\_LV\_COR}$	—		
95	$V_{DD\_HV\_REG\_1}$	—		
96	$V_{SS\_HV\_FLA}$	—		
97	$V_{DD\_HV\_FLA}$	—		
98	G[6]	SIUL	GPIO[102]	GPIO[102]
		FlexPWM_0	A[3]	A[3]
99	D[12]	SIUL	GPIO[60]	GPIO[60]
		FlexPWM_0	X[1]	X[1]
		LINFlexD_1	—	RXD
100	G[4]	SIUL	GPIO[100]	GPIO[100]
		FlexPWM_0	B[2]	B[2]
		eTimer_0	—	ETC[5]
101	C[13]	SIUL	GPIO[45]	GPIO[45]
		eTimer_1	ETC[1]	ETC[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
102	G[2]	SIUL	GPIO[98]	GPIO[98]
		FlexPWM_0	X[2]	X[2]
		DSPI_1	CS1	—
103	C[14]	SIUL	GPIO[46]	GPIO[46]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—

Table 5. Supply pins (continued)

Supply		Pin #	
Symbol	**Description**	**100 Pkg**	**144 Pkg**
V_{SS} 1V2	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	93	132
V_{DD} 1V2	VDD_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	—	135
V_{SS} 1V2	VSS_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	—	137

2.3 System pins

Table 6. System pins

Symbol	Description	Direction	Pin #	
			100 pkg	**144 pkg**
Dedicated pins				
MDO0(1)	Nexus Message Data Output — line	Output only	—	9
NMI(2)	Non Maskable Interrupt	Input only	1	1
XTAL	Input for oscillator amplifier circuit and internal clock generator	Input only	18	29
EXTAL(3)	Oscillator amplifier output	Input/Output(4)	19	30
TMS(2)	JTAG state machine control	Input only	59	87
TCK(2)	JTAG clock	Input only	60	88
JCOMP(5)	JTAG compliance select	Input only	84	123
Reset pin				
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter. This pin has medium drive strength. Output drive is open drain and must be terminated by an external resistor of value 1KOhm.(6)	Bidirectional	20	31
Test pin				
VPP TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.		74	107

1. This pad is configured for Fast (F) pad speed.
2. This pad contains a weak pull-up.
3. EXTAL is an "Output" in "crystal" mode, and is an "Input" in "ext clock" mode.
4. In XOSC Bypass Mode, the analog portion of crystal oscillator (amplifier) is disabled. An external clock can be applied at EXTAL as an input. In XOSC Normal Mode, EXTAL is an output
5. This pad contains a weak pull-down.

6. RESET output shall be considered valid only after the 3.3V supply reaches its stable value.

None of system pins (except RESET) provides an open drain output.

2.4 Pin muxing

Table 7 defines the pin list and muxing for this device.

Each entry of *Table 7* shows all the possible configurations for each pin, via the alternate functions. The default function assigned to each pin after reset is indicated by ALT0.

Note: Pins labeled "NC" are to be left unconnected. Any connection to an external circuit or voltage may cause unpredictable device behavior or damage.

Pins labeled "Reserved" are to be tied to ground. Not doing so may cause unpredictable device behavior.

Table 7. Pin muxing

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
Port A											
A[0]	PCR[0]	SIUL	GPIO[0]	ALT0	GPIO[0]	—	Pull down	M	S	51	73
		eTimer_0	ETC[0]	ALT1	ETC[0]	PSMI[35]; PADSEL=0					
		DSPI_2	SCK	ALT2	SCK	PSMI[1]; PADSEL=0					
		SIUL	—	—	EIRQ[0]	—					
A[1]	PCR[1]	SIUL	GPIO[1]	ALT0	GPIO[1]	—	Pull down	M	S	52	74
		eTimer_0	ETC[1]	ALT1	ETC[1]	PSMI[36]; PADSEL=0					
		DSPI_2	SOUT	ALT2	—	—					
		SIUL	—	—	EIRQ[1]	—					
A[2]	PCR[2]	SIUL	GPIO[2]	ALT0	GPIO[2]	—	Pull down	M	S	57	84
		eTimer_0	ETC[2]	ALT1	ETC[2]	PSMI[37]; PADSEL=0					
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=0					
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=0					
		MC_RGM	—	—	ABS[0]	—					
		SIUL	—	—	EIRQ[2]	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
A[9]	PCR[9]	SIUL	GPIO[9]	ALT0	GPIO[9]	—	Pull down	M	S	94	134
		DSPI_2	CS1	ALT1	—	—					
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=1					
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=0					
A[10]	PCR[10]	SIUL	GPIO[10]	ALT0	GPIO[10]	—	Pull down	M	S	81	118
		DSPI_2	CS0	ALT1	CS0	PSMI[3]; PADSEL=1					
		FlexPWM_0	B[0]	ALT2	B[0]	PSMI[24]; PADSEL=0					
		FlexPWM_0	X[2]	ALT3	X[2]	PSMI[29]; PADSEL=0					
		SIUL	—	—	EIRQ[9]	—					
A[11]	PCR[11]	SIUL	GPIO[11]	ALT0	GPIO[11]	—	Pull down	M	S	82	120
		DSPI_2	SCK	ALT1	SCK	PSMI[1]; PADSEL=1					
		FlexPWM_0	A[0]	ALT2	A[0]	PSMI[20]; PADSEL=0					
		FlexPWM_0	A[2]	ALT3	A[2]	PSMI[22]; PADSEL=0					
		SIUL	—	—	EIRQ[10]	—					
A[12]	PCR[12]	SIUL	GPIO[12]	ALT0	GPIO[12]	—	Pull down	M	S	83	122
		DSPI_2	SOUT	ALT1	—	—					
		FlexPWM_0	A[2]	ALT2	A[2]	PSMI[22]; PADSEL=1					
		FlexPWM_0	B[2]	ALT3	B[2]	PSMI[26]; PADSEL=0					
		SIUL	—	—	EIRQ[11]	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
Port E											
E[0]	PCR[64]	SIUL	—	ALT0	GPI[64]	—	—	—	—	46	68
		ADC_1	—	—	AN[5](3)	—					
E[2]	PCR[66]	SIUL	—	ALT0	GPI[66]	—	—	—	—	32	49
		ADC_0	—	—	AN[5](3)	—					
E[4]	PCR[68]	SIUL	—	ALT0	GPI[68]	—	—	—	—	—	42
		ADC_0	—	—	AN[7](3)	—					
E[5]	PCR[69]	SIUL	—	ALT0	GPI[69]	—	—	—	—	—	44
		ADC_0	—	—	AN[8](3)	—					
E[6]	PCR[70]	SIUL	—	ALT0	GPI[70]	—	—	—	—	—	46
		ADC_0	—	—	AN[4](3)	—					
E[7]	PCR[71]	SIUL	—	ALT0	GPI[71]	—	—	—	—	—	48
		ADC_0	—	—	AN[6](3)	—					
E[9]	PCR[73]	SIUL	—	ALT0	GPI[73]	—	—	—	—	—	61
		ADC_1	—	—	AN[7](3)	—					
E[10]	PCR[74]	SIUL	—	ALT0	GPI[74]	—	—	—	—	—	63
		ADC_1	—	—	AN[8](3)	—					
E[11]	PCR[75]	SIUL	—	ALT0	GPI[75]	—	—	—	—	—	65
		ADC_1	—	—	AN[4](3)	—					
E[12]	PCR[76]	SIUL	—	ALT0	GPI[76]	—	—	—	—	—	67
		ADC_1	—	—	AN[6](3)	—					
E[13]	PCR[77]	SIUL	GPIO[77]	ALT0	GPIO[77]	—	Pull down	M	S	—	117
		eTimer_0	ETC[5]	ALT1	ETC[5]	PSMI[8]; PADSEL=1					
		DSPI_2	CS3	ALT2	—	—					
		SIUL	—	—	EIRQ[25]	—					
E[14]	PCR[78]	SIUL	GPIO[78]	ALT0	GPIO[78]	—	Pull down	M	S	—	119
		eTimer_1	ETC[5]	ALT1	ETC[5]	PSMI[14]; PADSEL=3					
		SIUL	—	—	EIRQ[26]	—					
E[15]	PCR[79]	SIUL	GPIO[79]	ALT0	GPIO[79]	—	Pull down	M	S	—	121
		DSPI_0	CS1	ALT1	—	—					
		SIUL	—	—	EIRQ[27]	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
I[3]	PCR[131]	SIUL	GPIO[131]	ALT0	GPIO[131]	—	Pull down	M	S	—	—
		eTimer_2	ETC[3]	ALT1	ETC[3]	PSMI[42]; PADSEL=1					
		DSPI_0	CS7	ALT2	—	—					
		CTU_0	EXT_TGR	ALT3	—	—					
		FlexPWM_1	—	—	FAULT[3]	—					
$\overline{\text{RDY}}$	PCR[132]	SIUL	GPIO[132]	ALT0	GPIO[132]	—	Pull down	F	S	—	—
		NPC	RDY	ALT2	—	—					

1. Programmable via the SRC (Slew Rate Control) bit in the respective Pad Configuration Register; S = Slow, M = Medium, F = Fast, SYM = Symmetric (for FlexRay).
2. The default function of this pin out of reset is ALT1 (TDO).
3. Analog.

Table 8. Absolute maximum ratings(1) (continued)

Symbol		Parameter	Conditions	Min	Max	Unit
$V_{SS\_HV\_ADR0}$ $V_{SS\_HV\_ADR1}$	SR	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADV}$	SR	3.3 V ADC supply voltage	—	–0.3	4.5(3), (4)	V
$V_{SS\_HV\_ADV}$	SR	3.3 V ADC supply ground	—	–0.1	0.1	V
TV_{DD}	SR	Supply ramp rate	—	3.0×10^{-6} (3.0 V/sec)	0.5 V/µs	V/µs
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS\_HV\_IOx}$)or $V_{ss\_HV\_ADRx}$	Valid only for ADC pins	–0.3	6.0(4)	V
			Relative to V_{DD}	–0.3	V_{DD} + 0.3(4), (5)	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{STG}	SR	Storage temperature	—	–55	150	°C

1. Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability or cause permanent damage to the device.
2. Any voltage between operating condition and absolute max rating can be sustained for maximum cumulative time of 10 hours.
3. Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
4. Internal structures hold the input voltage less than the maximum voltage on all pads powered by VDDE supplies, if the maximum injection current specification is met (2 mA for all pins) and VDDE is within the operating voltage specifications.
5. V_{DD} has to be considered equal to $V_{DD\_HV\_ADRx}$ in case of ADC pins, whilst it is $V_{DD\_HV\_IOx}$ for any other pin.

3.3 Recommended operating conditions

Table 9. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Min(1)	Max	Unit
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.63	V
$V_{SS\_HV\_REG}$	SR	3.3 V voltage regulator reference voltage	—	0	0	V
$V_{DD\_HV\_IOx}$	SR	3.3 V input/output supply voltage	—	3.0	3.63	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FLA}$	SR	3.3 V flash supply voltage	—	3.0	3.63	V
$V_{SS\_HV\_FLA}$	SR	Flash memory ground	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.63	V
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD\_HV\_ADR0}$(2),(3) $V_{DD\_HV\_ADR1}$	SR	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	4.5 to 5.5 or 3.0 to 3.63		V

Table 10. Decoupling capacitors (continued)

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
C_{PMU2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{REG}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		20		µF
C_{IO1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{IO2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		470		pF
C_{FLA1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{FLA2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		10		nF
C_{OSC1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		100		nF
C_{OSC2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%.		10		nF
C_{PLL1}	SR	External decoupling / stability capacitor		22		100	nF
C_{ADR1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		10		nF
C_{ADR2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		47		nF
C_{ADR3}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Electrolytic or tantalum capacitor.		1		µF
C_{ADV1}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		10		nF
C_{ADV2}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Ceramic capacitor.		47		nF
C_{ADV3}	SR	External decoupling / stability capacitor	Accuracy -50%/+35%. Electrolytic or tantalum capacitor.		1		µF

1. Capacitors shall be placed as close as possible to the respective pads.
2. Total ESR considering all decoupling capacitor close to the $V_{DD}/V_{SS\_LV\_CORy}$ pairs shall be between 1 mΩ and 100 mΩ.

3.5.1.1 References

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134 USA
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB in JEDEC site.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.6 Electromagnetic Interference (EMI) characteristics

The characteristics in *Table 14* were measured using:

- Device configuration, test conditions, and EM testing per standard IEC61967-2
- Supply voltage of 3.3 V DC
- Ambient temperature of 25 °C

The configuration information referenced in *Table 14* is explained in *Table 13*.

Table 13. EMI configuration summary

Configuration name	Description
Configuration A	– High emission = all pads have max slew rate, LVDS pads running at 40 MHz – Oscillator frequency = 40 MHz – System bus frequency = 120 MHz – No PLL frequency modulation – IEC level K (≤ 30 dBµV)
Configuration B	– Reference emission = pads use min, mid and max slew rates, LVDS pads disabled – Oscillator frequency = 40 MHz – System bus frequency = 120 MHz – 2% PLL frequency modulation – IEC level K(≤ 30 dBµV)

considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to *Equation 7*:

Equation 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Equation 9

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. *Equation 10* must be respected (charge balance assuming now C_S already charged at V_{A1}):

Figure 14. Destructive Reset Sequence, BIST disabled

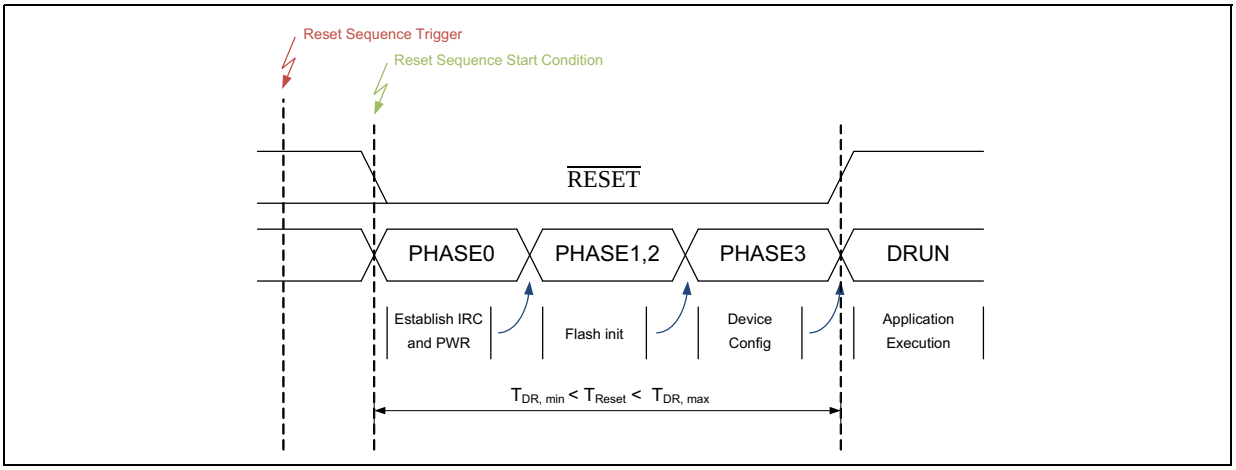


Figure 15. External Reset Sequence Long, BIST enabled

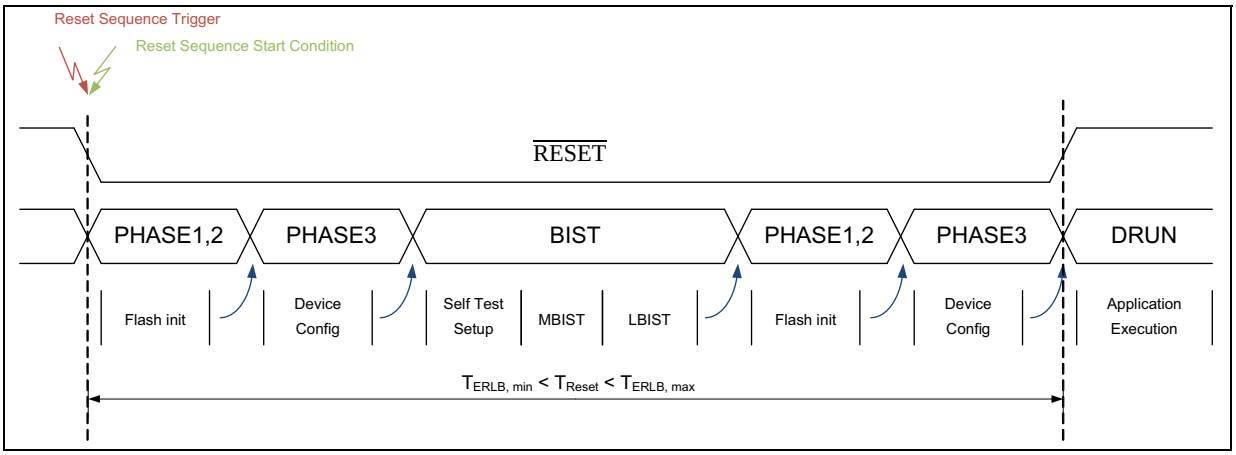


Figure 16. Functional Reset Sequence Long

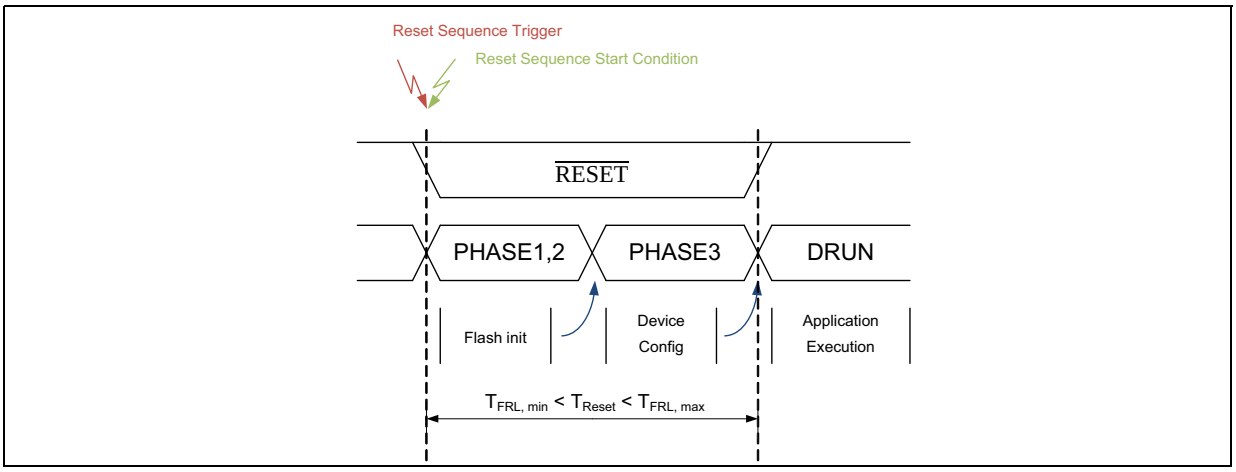
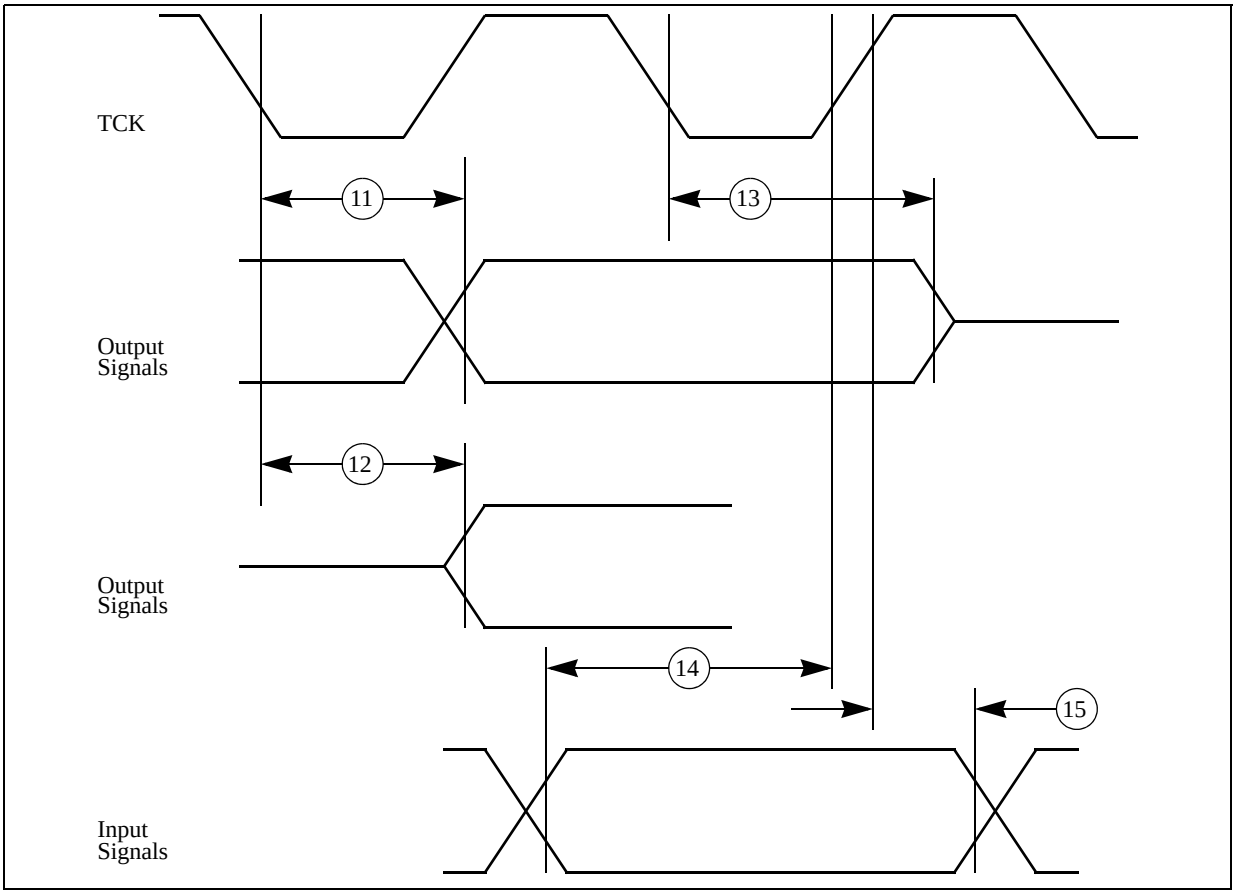


Figure 25. JTAG boundary scan timing



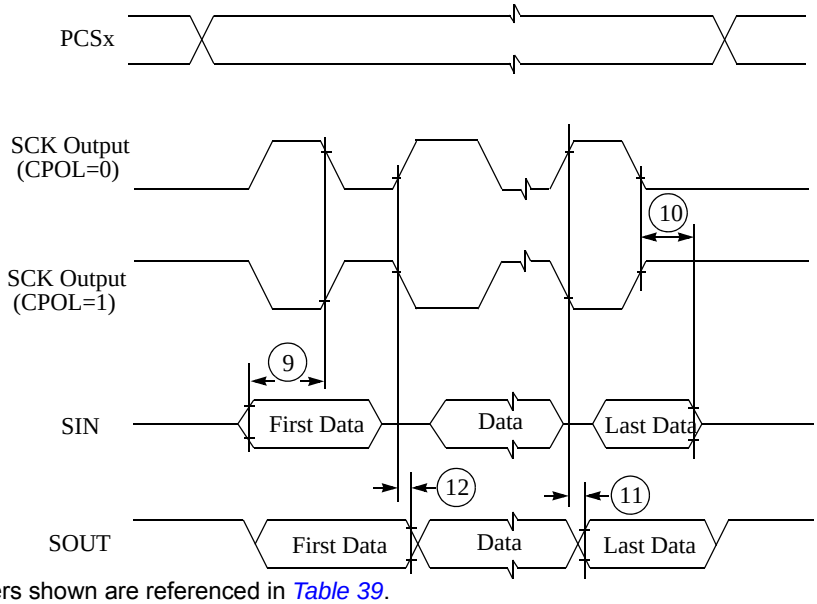
3.20.4 Nexus timing

Table 37. Nexus debug port timing(1)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{MCYC}	D	MCKO Cycle Time	—	15.6	—	ns
2	t_{MDC}	D	MCKO Duty Cycle	—	40	60	%
3	t_{MDOV}	D	MCKO Low to MDO, $\overline{MSEO}$, $\overline{EVTO}$ Data Valid(2)	—	–0.1	0.25	t_{MCYC}
4	t_{EVTIPW}	D	$\overline{EVTI}$ Pulse Width	—	4.0	—	t_{TCYC}
5	t_{EVTOPW}	D	$\overline{EVTO}$ Pulse Width	—	1		t_{MCYC}
6	t_{TCYC}	D	TCK Cycle Time(3)	—	62.5	—	ns
7	t_{TDC}	D	TCK Duty Cycle	—	40	60	%
8	t_{NTDIS}, t_{NTMSS}	D	TDI, TMS Data Setup Time	—	8	—	ns
9	t_{NTDIH}, t_{NTMSH}	D	TDI, TMS Data Hold Time	—	5	—	ns
10	t_{JOV}	D	TCK Low to TDO Data Valid	—	0	25	ns

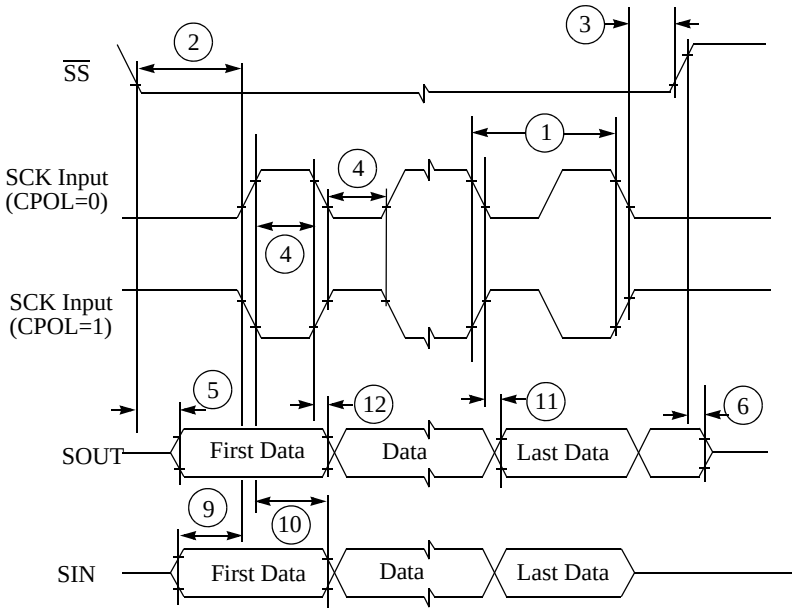
1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. For all Nexus modes except DDR mode, MDO, $\overline{MSEO}$, and $\overline{EVTO}$ data is held valid until next MCKO low cycle.

Figure 31. DSPI classic SPI timing — master, CPHA = 1



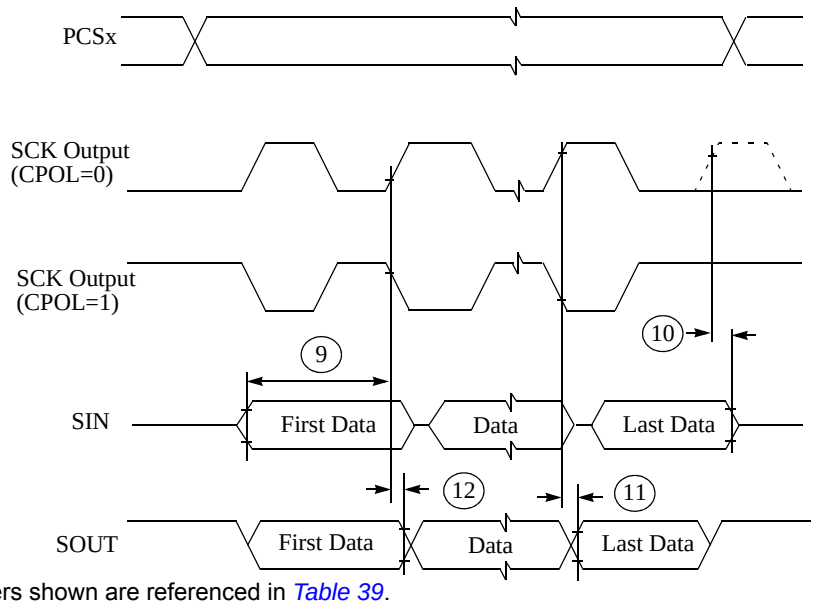
Note: The numbers shown are referenced in *Table 39*.

Figure 32. DSPI classic SPI timing — slave, CPHA = 0



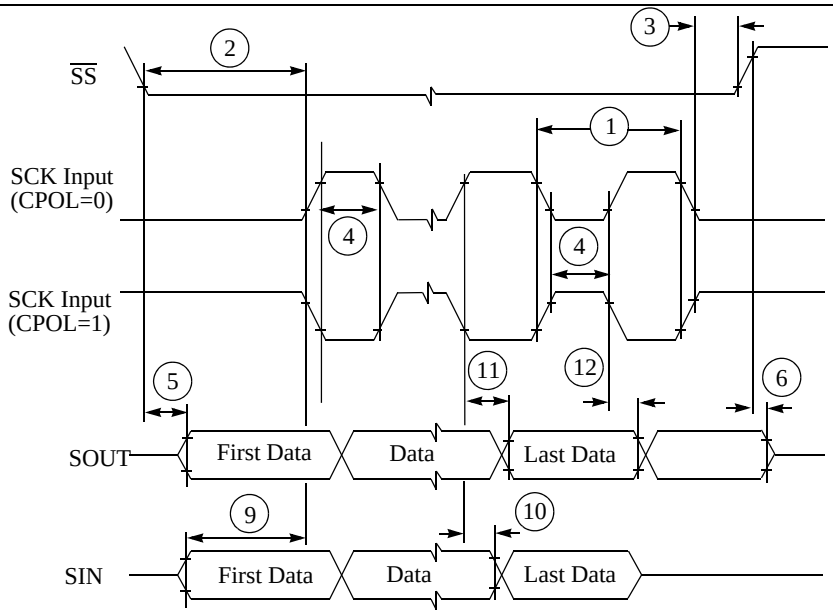
Note: The numbers shown are referenced in *Table 39*.

Figure 35. DSPI modified transfer format timing — master, CPHA = 1



Note: The numbers shown are referenced in *Table 39*.

Figure 36. DSPI modified transfer format timing – slave, CPHA = 0



Note: The numbers shown are referenced in *Table 39*.