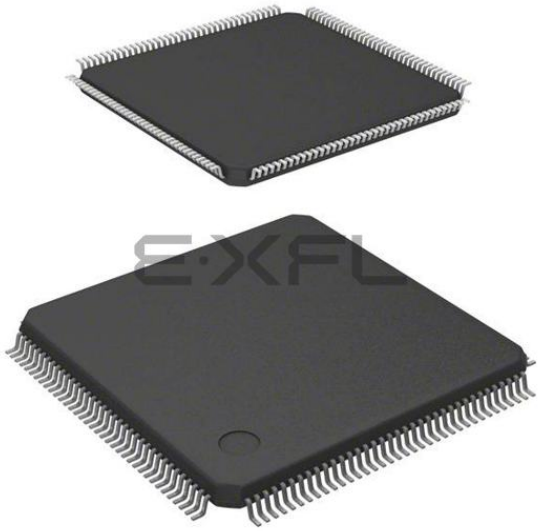


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56el70l5cbosy

The SIU provides the following features:

- Centralized pad control on a per-pin basis
  - Pin function selection
  - Configurable weak pull-up/down
  - Configurable slew rate control (slow/medium/fast)
  - Hysteresis on GPIO pins
  - Configurable automatic safe mode pad control
- Input filtering for external interrupts

1.5.23 Non-maskable interrupt (NMI)

The non-maskable interrupt with de-glitching filter supports high-priority core exceptions.

1.5.24 Boot assist module (BAM)

The BAM is a block of read-only memory with hard-coded content. The BAM program is executed only if serial booting mode is selected via boot configuration pins.

The BAM provides the following features:

- Enables booting via serial mode (FlexCAN or LINFlex-UART)
- Supports programmable 64-bit password protection for serial boot mode
- Supports serial bootloading of either Power Architecture code (default) or VLE code
- Automatic switch to serial boot mode if internal flash memory is blank or invalid

1.5.25 System status and configuration module (SSCM)

The SSCM on this device features the following:

- System configuration and status
- Debug port status and debug port enable
- Multiple boot code starting locations out of reset through implementation of search for valid Reset Configuration Half Word
- Sets up the MMU to allow user boot code to execute as either Power Architecture code (default) or as VLE code out of flash memory
- Triggering of device self-tests during reset phase of device boot

1.5.26 FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth.

1.5.29 Deserial serial peripheral interface (DSPI)

The DSPI modules provide a synchronous serial interface for communication between the SPC56XL70 and external devices.

A DSPI module provides these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- As many as 8 chip select lines available, depending on package and pin multiplexing
- 4 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for de-glitching
- FIFOs for buffering as many as 5 transfers on the transmit and receive side
- Queueing operation possible through use of the eDMA
- General purpose I/O functionality on pins when not used for SPI

1.5.30 FlexPWM

The pulse width modulator module (FlexPWM) contains four PWM channels, each of which is configured to control a single half-bridge power stage. One module is present in LQFP144 package. Additionally, four fault input channels are provided per FlexPWM module.

This PWM is capable of controlling most motor types, including:

- AC induction motors (ACIM)
- Permanent Magnet AC motors (PMAC)
- Brushless (BLDC) and brush DC motors (BDC)
- Switched (SRM) and variable reluctance motors (VRM)
- Stepper motors

A FlexPWM module implements the following features:

- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- Maximum operating frequency as high as 120 MHz
  - Clock source not modulated and independent from system clock (generated via secondary FMPLL)
- Fine granularity control for enhanced resolution of the PWM period
- PWM outputs can operate as complementary pairs or independent channels
- Ability to accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software control for each PWM output
- All outputs can be forced to a value simultaneously
- PWMX pin can optionally output a third signal from each channel
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual edge capture functionality
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - External digital pin
  - Internal timer channel
  - External ADC input, taking into account values set in ADC high- and low-limit registers
- DMA support

1.5.41 Built-In self-test (BIST) capability

This device includes the following protection against latent faults:

- Boot-time Memory Built-In Self-Test (MBIST)
- Boot-time scan-based Logic Built-In Self-Test (LBIST)
- Run-time ADC Built-In Self-Test (BIST)
- Run-time Built-In Self Test of LVDs

2 Package pinouts and signal descriptions

2.1 Package pinouts

Figure 2 shows the SPC56XL70 in the LQFP100 package.

Figure 2. SPC56XL70 LQFP100 package

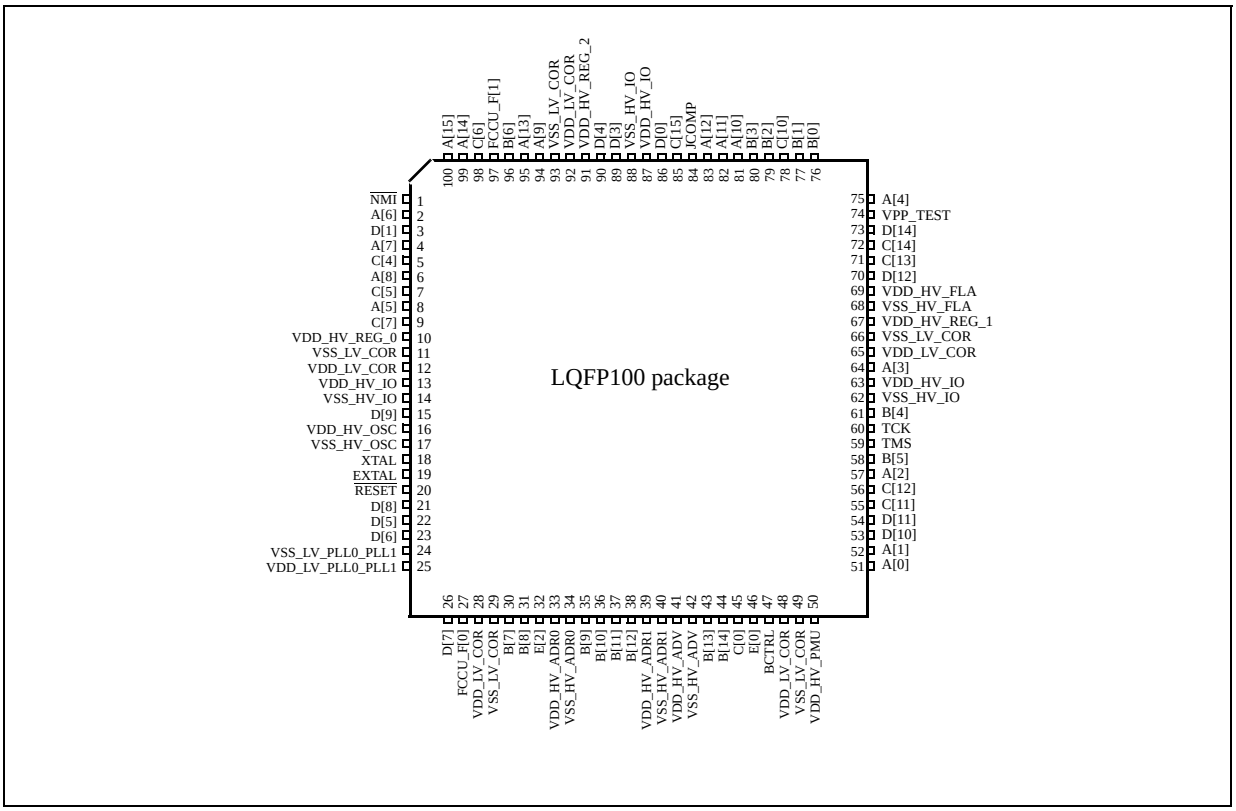


Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
14	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]
15	C[7]	SIUL	GPIO[39]	GPIO[39]
		FlexPWM_0	A[1]	A[1]
		SSCM	DEBUG[7]	—
		DSPI_0	—	SIN
16	$V_{DD\_HV\_REG\_0}$	—		
17	$V_{SS\_LV\_COR}$	—		
18	$V_{DD\_LV\_COR}$	—		
19	F[7]	SIUL	GPIO[87]	GPIO[87]
		NPC	MCKO	—
20	F[8]	SIUL	GPIO[88]	GPIO[88]
		NPC	MSEO[1]	—
21	$V_{DD\_HV\_IO}$	—		
22	$V_{SS\_HV\_IO}$	—		
23	F[9]	SIUL	GPIO[89]	GPIO[89]
		NPC	MSEO[0]	—
24	F[10]	SIUL	GPIO[90]	GPIO[90]
		NPC	EVTO	—
25	F[11]	SIUL	GPIO[91]	GPIO[91]
		NPC	EVTI	—
26	D[9]	SIUL	GPIO[57]	GPIO[57]
		FlexPWM_0	X[0]	X[0]
		LINFlexD_1	TXD	—
27	$V_{DD\_HV\_OSC}$	—		
28	$V_{SS\_HV\_OSC}$	—		
29	XTALIN	—		
30	XTALOUT	—		
31	RESET	—		

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
89	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—
90	$V_{SS\_HV\_IO}$	—		
91	$V_{DD\_HV\_IO}$	—		
92	A[3]	SIUL	GPIO[3]	GPIO[3]
		eTimer_0	ETC[3]	ETC[3]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[3]	B[3]
		MC_RGM	—	ABS[2]
		SIUL	—	EIRQ[3]
93	$V_{DD\_LV\_COR}$	—		
94	$V_{SS\_LV\_COR}$	—		
95	$V_{DD\_HV\_REG\_1}$	—		
96	$V_{SS\_HV\_FLA}$	—		
97	$V_{DD\_HV\_FLA}$	—		
98	G[6]	SIUL	GPIO[102]	GPIO[102]
		FlexPWM_0	A[3]	A[3]
99	D[12]	SIUL	GPIO[60]	GPIO[60]
		FlexPWM_0	X[1]	X[1]
		LINFlexD_1	—	RXD
100	G[4]	SIUL	GPIO[100]	GPIO[100]
		FlexPWM_0	B[2]	B[2]
		eTimer_0	—	ETC[5]
101	C[13]	SIUL	GPIO[45]	GPIO[45]
		eTimer_1	ETC[1]	ETC[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
102	G[2]	SIUL	GPIO[98]	GPIO[98]
		FlexPWM_0	X[2]	X[2]
		DSPI_1	CS1	—
103	C[14]	SIUL	GPIO[46]	GPIO[46]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
122	A[12]	SIUL	GPIO[12]	GPIO[12]
		DSPI_2	SOUT	—
		FlexPWM_0	A[2]	A[2]
		FlexPWM_0	B[2]	B[2]
		SIUL	—	EIRQ[11]
123	JCOMP	—	—	JCOMP
124	C[15]	SIUL	GPIO[47]	GPIO[47]
		FlexRay	CA_TR_EN	—
		eTimer_1	ETC[0]	ETC[0]
		FlexPWM_0	A[1]	A[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
125	D[0]	SIUL	GPIO[48]	GPIO[48]
		FlexRay	CA_TX	—
		eTimer_1	ETC[1]	ETC[1]
		FlexPWM_0	B[1]	B[1]
126	$V_{DD\_HV\_IO}$	—		
127	$V_{SS\_HV\_IO}$	—		
128	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
129	D[4]	SIUL	GPIO[52]	GPIO[52]
		FlexRay	CB_TR_EN	—
		eTimer_1	ETC[5]	ETC[5]
		FlexPWM_0	B[3]	B[3]
130	$V_{DD\_HV\_REG\_2}$	—		
131	$V_{DD\_LV\_COR}$	—		
132	$V_{SS\_LV\_COR}$	—		
133	F[0]	SIUL	GPIO[80]	GPIO[80]
		FlexPWM_0	A[1]	A[1]
		eTimer_0	—	ETC[2]
		SIUL	—	EIRQ[28]

Table 5. Supply pins (continued)

Supply		Pin #	
Symbol	**Description**	**100 Pkg**	**144 Pkg**
$V_{DD\_HV\_REG\_1}$	VDD_HV_REG_1	67	95
$V_{SS\_HV\_FLA}$	VSS_HV_FLA	68	96
$V_{DD\_HV\_FLA}$	VDD_HV_FLA	69	97
$V_{DD\_HV\_IO}$	VDD_HV_IO	87	126
$V_{SS\_HV\_IO}$	VSS_HV_IO	88	127
$V_{DD\_HV\_REG\_2}$	VDD_HV_REG_2	91	130
Power supply pins (1.2 V)			
$V_{SS\_LV\_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	11	17
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	12	18
V_{SS} 1V2	VSS_LV_PLL0_PLL1 / 1.2 V Decoupling pins for on-chip FMPLL modules. Decoupling capacitor must be connected between this pin and $V_{DD\_LV\_PLL}$.	24	35
V_{DD} 1V2	VDD_LV_PLL0_PLL1 Decoupling pins for on-chip FMPLL modules. Decoupling capacitor must be connected between this pin and $V_{SS\_LV\_PLL}$.	25	36
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	28	39
$V_{SS\_LV\_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	29	40
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS\_LV\_REGCOR}$.	—	70
$V_{SS\_LV\_COR}$	VSS_LV_REGCOR0 Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD\_LV\_REGCOR}$.	—	71
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	65	93
$V_{SS\_LV\_COR}$	VSS_LV_COR / 1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	66	94
V_{DD} 1V2	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	92	131

Table 5. Supply pins (continued)

Supply		Pin #	
Symbol	**Description**	**100 Pkg**	**144 Pkg**
V_{SS} 1V2	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	93	132
V_{DD} 1V2	VDD_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	—	135
V_{SS} 1V2	VSS_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	—	137

2.3 System pins

Table 6. System pins

Symbol	Description	Direction	Pin #	
			100 pkg	**144 pkg**
Dedicated pins				
MDO0(1)	Nexus Message Data Output — line	Output only	—	9
NMI(2)	Non Maskable Interrupt	Input only	1	1
XTAL	Input for oscillator amplifier circuit and internal clock generator	Input only	18	29
EXTAL(3)	Oscillator amplifier output	Input/Output(4)	19	30
TMS(2)	JTAG state machine control	Input only	59	87
TCK(2)	JTAG clock	Input only	60	88
JCOMP(5)	JTAG compliance select	Input only	84	123
Reset pin				
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter. This pin has medium drive strength. Output drive is open drain and must be terminated by an external resistor of value 1KOhm.(6)	Bidirectional	20	31
Test pin				
VPP TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.		74	107

1. This pad is configured for Fast (F) pad speed.
2. This pad contains a weak pull-up.
3. EXTAL is an "Output" in "crystal" mode, and is an "Input" in "ext clock" mode.
4. In XOSC Bypass Mode, the analog portion of crystal oscillator (amplifier) is disabled. An external clock can be applied at EXTAL as an input. In XOSC Normal Mode, EXTAL is an output
5. This pad contains a weak pull-down.

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
B[9]	PCR[25]	SIUL	—	ALT0	GPI[25]	—	—	—	—	35	52
		ADC_0 ADC_1	—	—	AN[11](3)	—					
B[10]	PCR[26]	SIUL	—	ALT0	GPI[26]	—	—	—	—	36	53
		ADC_0 ADC_1	—	—	AN[12](3)	—					
B[11]	PCR[27]	SIUL	—	ALT0	GPI[27]	—	—	—	—	37	54
		ADC_0 ADC_1	—	—	AN[13](3)	—					
B[12]	PCR[28]	SIUL	—	ALT0	GPI[28]	—	—	—	—	38	55
		ADC_0 ADC_1	—	—	AN[14](3)	—					
B[13]	PCR[29]	SIUL	—	ALT0	GPI[29]	—	—	—	—	43	60
		LINFlex_1	—	—	RXD	PSMI[32]; PADSEL=0					
		ADC_1	—	—	AN[0](3)	—					
B[14]	PCR[30]	SIUL	—	ALT0	GPI[30]	—	—	—	—	44	64
		eTimer_0	—	—	ETC[4]	PSMI[7]; PADSEL=2					
		SIUL	—	—	EIRQ[19]	—					
		ADC_1	—	—	AN[1](3)	—					
B[15]	PCR[31]	SIUL	—	ALT0	GPI[31]	—	—	—	—	—	62
		SIUL	—	—	EIRQ[20]	—					
		ADC_1	—	—	AN[2](3)	—					
Port C											
C[0]	PCR[32]	SIUL	—	ALT0	GPI[32]	—	—	—	—	45	66
		ADC_1	—	—	AN[3](3)	—					
C[1]	PCR[33]	SIUL	—	ALT0	GPI[33]	—	—	—	—	—	41
		ADC_0	—	—	AN[2](3)	—					
C[2]	PCR[34]	SIUL	—	ALT0	GPI[34]	—	—	—	—	—	45
		ADC_0	—	—	AN[3](3)	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
Port E											
E[0]	PCR[64]	SIUL	—	ALT0	GPI[64]	—	—	—	—	46	68
		ADC_1	—	—	AN[5](3)	—					
E[2]	PCR[66]	SIUL	—	ALT0	GPI[66]	—	—	—	—	32	49
		ADC_0	—	—	AN[5](3)	—					
E[4]	PCR[68]	SIUL	—	ALT0	GPI[68]	—	—	—	—	—	42
		ADC_0	—	—	AN[7](3)	—					
E[5]	PCR[69]	SIUL	—	ALT0	GPI[69]	—	—	—	—	—	44
		ADC_0	—	—	AN[8](3)	—					
E[6]	PCR[70]	SIUL	—	ALT0	GPI[70]	—	—	—	—	—	46
		ADC_0	—	—	AN[4](3)	—					
E[7]	PCR[71]	SIUL	—	ALT0	GPI[71]	—	—	—	—	—	48
		ADC_0	—	—	AN[6](3)	—					
E[9]	PCR[73]	SIUL	—	ALT0	GPI[73]	—	—	—	—	—	61
		ADC_1	—	—	AN[7](3)	—					
E[10]	PCR[74]	SIUL	—	ALT0	GPI[74]	—	—	—	—	—	63
		ADC_1	—	—	AN[8](3)	—					
E[11]	PCR[75]	SIUL	—	ALT0	GPI[75]	—	—	—	—	—	65
		ADC_1	—	—	AN[4](3)	—					
E[12]	PCR[76]	SIUL	—	ALT0	GPI[76]	—	—	—	—	—	67
		ADC_1	—	—	AN[6](3)	—					
E[13]	PCR[77]	SIUL	GPIO[77]	ALT0	GPIO[77]	—	Pull down	M	S	—	117
		eTimer_0	ETC[5]	ALT1	ETC[5]	PSMI[8]; PADSEL=1					
		DSPI_2	CS3	ALT2	—	—					
		SIUL	—	—	EIRQ[25]	—					
E[14]	PCR[78]	SIUL	GPIO[78]	ALT0	GPIO[78]	—	Pull down	M	S	—	119
		eTimer_1	ETC[5]	ALT1	ETC[5]	PSMI[14]; PADSEL=3					
		SIUL	—	—	EIRQ[26]	—					
E[15]	PCR[79]	SIUL	GPIO[79]	ALT0	GPIO[79]	—	Pull down	M	S	—	121
		DSPI_0	CS1	ALT1	—	—					
		SIUL	—	—	EIRQ[27]	—					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #	
								SRC = 1	SRC = 0	100 pkg	144 pkg
Port F											
F[0]	PCR[80]	SIUL	GPIO[80]	ALT0	GPIO[80]	—	Pull down	M	S	—	133
		FlexPWM_0	A[1]	ALT1	A[1]	PSMI[21]; PADSEL=2					
		eTimer_0	—	—	ETC[2]	PSMI[37]; PADSEL=1					
		SIUL	—	—	EIRQ[28]	—					
F[3]	PCR[83]	SIUL	GPIO[83]	ALT0	GPIO[83]	—	Pull down	M	S	—	139
		DSPI_0	CS6	ALT1	—	—					
F[4]	PCR[84]	SIUL	GPIO[84]	ALT0	GPIO[84]	—	Pull down	F	S	—	4
		NPC	MDO[3]	ALT2	—	—					
F[5]	PCR[85]	SIUL	GPIO[85]	ALT0	GPIO[85]	—	Pull down	F	S	—	5
		NPC	MDO[2]	ALT2	—	—					
F[6]	PCR[86]	SIUL	GPIO[86]	ALT0	GPIO[86]	—	Pull down	F	S	—	8
		NPC	MDO[1]	ALT2	—	—					
F[7]	PCR[87]	SIUL	GPIO[87]	ALT0	GPIO[87]	—	Pull down	F	S	—	19
		NPC	MCKO	ALT2	—	—					
F[8]	PCR[88]	SIUL	GPIO[88]	ALT0	GPIO[88]	—	Pull down	F	S	—	20
		NPC	MSEO[1]	ALT2	—	—					
F[9]	PCR[89]	SIUL	GPIO[89]	ALT0	GPIO[89]	—	Pull down	F	S	—	23
		NPC	MSEO[0]	ALT2	—	—					
F[10]	PCR[90]	SIUL	GPIO[90]	ALT0	GPIO[90]	—	Pull down	F	S	—	24
		NPC	EVTO	ALT2	—	—					
F[11]	PCR[91]	SIUL	GPIO[91]	ALT0	GPIO[91]	—	Pull down	M	S	—	25
		NPC	EVTI	ALT2	—	—					
F[12]	PCR[92]	SIUL	GPIO[92]	ALT0	GPIO[92]	—	Pull down	M	S	—	106
		eTimer_1	ETC[3]	ALT1	ETC[3]	PSMI[12]; PADSEL=2					
		SIUL	—	—	EIRQ[30]	—					
F[13]	PCR[93]	SIUL	GPIO[93]	ALT0	GPIO[93]	—	Pull down	M	S	—	112
		eTimer_1	ETC[4]	ALT1	ETC[4]	PSMI[13]; PADSEL=3					
		SIUL	—	—	EIRQ[31]	—					

Table 8. Absolute maximum ratings(1) (continued)

Symbol		Parameter	Conditions	Min	Max	Unit
$V_{SS\_HV\_ADR0}$ $V_{SS\_HV\_ADR1}$	SR	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADV}$	SR	3.3 V ADC supply voltage	—	–0.3	4.5(3), (4)	V
$V_{SS\_HV\_ADV}$	SR	3.3 V ADC supply ground	—	–0.1	0.1	V
TV_{DD}	SR	Supply ramp rate	—	3.0×10^{-6} (3.0 V/sec)	0.5 V/µs	V/µs
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS\_HV\_IOx}$)or $V_{ss\_HV\_ADRx}$	Valid only for ADC pins	–0.3	6.0(4)	V
			Relative to V_{DD}	–0.3	V_{DD} + 0.3(4), (5)	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{STG}	SR	Storage temperature	—	–55	150	°C

1. Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability or cause permanent damage to the device.
2. Any voltage between operating condition and absolute max rating can be sustained for maximum cumulative time of 10 hours.
3. Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
4. Internal structures hold the input voltage less than the maximum voltage on all pads powered by VDDE supplies, if the maximum injection current specification is met (2 mA for all pins) and VDDE is within the operating voltage specifications.
5. V_{DD} has to be considered equal to $V_{DD\_HV\_ADRx}$ in case of ADC pins, whilst it is $V_{DD\_HV\_IOx}$ for any other pin.

3.3 Recommended operating conditions

Table 9. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Min(1)	Max	Unit
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.63	V
$V_{SS\_HV\_REG}$	SR	3.3 V voltage regulator reference voltage	—	0	0	V
$V_{DD\_HV\_IOx}$	SR	3.3 V input/output supply voltage	—	3.0	3.63	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FLA}$	SR	3.3 V flash supply voltage	—	3.0	3.63	V
$V_{SS\_HV\_FLA}$	SR	Flash memory ground	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.63	V
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD\_HV\_ADR0}$(2),(3) $V_{DD\_HV\_ADR1}$	SR	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	4.5 to 5.5 or 3.0 to 3.63		V

Table 17. Recommended operating characteristics (continued)

Symbol	Parameter	Value	Unit
I_{CMaxDC}	Maximum peak collector current	1.0	A
VCE_{SAT}	Collector-to-emitter saturation voltage(Max)	600(2)	mV
V_{BE}	Base-to-emitter voltage (Max)	1.0	V

1. Derating factor 12mW/degC.
2. Adjust resistor at bipolar transistor collector for 3.3V to avoid VCE<$VCE_{SAT.}$

The recommended external ballast transistor is the bipolar transistor BCP68 with the gain range of 85 up to 375 (for IC=500mA, VCE=1V) provided by several suppliers. This includes the gain variations BCP68-10, BCP68-16 and BCP68-25.The most important parameters for the interoperability with the integrated voltage regulator are the DC current gain (hFE) and the temperature coefficient of the gain (XTB). While the specified gain range of most BCP68 vendors is the same, there are slight variations in the temperature coefficient parameter. Voltage regulator operation was simulated against the typical variation on temperature coefficient and against the specified gain range to have a robust design.

Table 18. Voltage regulator electrical specifications

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
C_{ext}		External decoupling/ stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	12	—	40	µF
	SR	Combined ESR of external capacitor	—	1	—	100	mΩ
	SR	Number of pins for external decoupling/ stability capacitor	—	5	—	—	—
C_{V1V2}	SR	Total capacitance on 1.2 V pins	Ceramic capacitors, taking into account tolerance, aging, voltage and temperature variation	300	—	900	nF
t_{SU}		Start-up time after main supply stabilization	C_{load} = 10 µF × 4	—	—	2.5	ms
—		Main High Voltage Power - Low Voltage Detection, upper threshold	—	—	—	2.93	V
—	D	Main supply low voltage detector, lower threshold	—	2.6	—	—	V

3.13 FMPLL electrical characteristics

Table 23. FMPLL electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
$f_{REF\_CRYSTAL}$ f_{REF_EXT}	D	FMPLL reference frequency range(1)	Crystal reference	4	—	40	MHz
f_{PLL_IN}	D	Phase detector input frequency range (after pre-divider)	—	4	—	16	MHz
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode	—	4	—	120(2)	MHz
f_{FREE}	P	Free running frequency	Measured using clock division (typically ÷16)	20	—	150	MHz
f_{sys}	D	On-chip FMPLL frequency(2)	—	16	—	120	MHz
t_{CYC}	D	System clock period	—	—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	D	Loss of reference frequency window(3)	Lower limit	1.6	—	3.7	MHz
			Upper limit	24	—	56	
f_{SCM}	D	Self-clocked mode frequency(4),(5)	—	20	—	150	MHz
t_{LOCK}	P	Lock time	Stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}	—	—	200	µs
t_{lpll}	D	FMPLL lock time (6), (7)	—	—	—	200	µs
t_{dc}	D	Duty cycle of reference	—	40	—	60	%
C_{JITTER}	T	CLKOUT period jitter(8),(9),(10),(11)	Long-term jitter (avg. over 2 ms interval), $f_{FMPLLOUT}$ maximum	–6	—	6	ns
Δt_{PKJIT}	T	Single period jitter (peak to peak)	PHI @ 120 MHz, Input clock @ 4 MHz	—	—	175	ps
			PHI @ 100 MHz, Input clock @ 4 MHz	—	—	185	ps
			PHI @ 80 MHz, Input clock @ 4 MHz	—	—	200	ps
Δt_{LTJIT}	T	Long term jitter	PHI @ 16 MHz, Input clock @ 4 MHz	—	—	±6	ns
f_{LCK}	D	Frequency LOCK range	—	–6	—	6	% $f_{FMPLLOUT}$
f_{UL}	D	Frequency un-LOCK range	—	–18	—	18	% $f_{FMPLLOUT}$
f_{CS} f_{DS}	D	Modulation depth	Center spread	±0.25	—	±2.0	% $f_{FMPLLOUT}$
			Down spread	–0.5	—	-8.0	
f_{MOD}	D	Modulation frequency(12)	—	—	—	100	KHz

1. Considering operation with FMPLL not bypassed.
2. With FM; the value does not include a possible +2% modulation
3. “Loss of Reference Frequency” window is the reference frequency range outside of which the FMPLL is in self clocked mode.

Table 28. Flash memory module life

No.	Symbol		Parameter	Value			Unit
				Min	Typ	Max	
1	P/E	C	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 KB blocks over the operating temperature range(1)	100000	—	—	cycles
2	P/E	C	Number of program/erase cycles per block for 128 KB and 256 KB blocks over the operating temperature range(1)	1000	100000(2)	—	cycles
3	Retention	C	Minimum data retention at 85 °C average ambient temperature(3) Blocks with 0–1,000 P/E cycles Blocks with 1,001–10,000 P/E cycles Blocks with 10,001–100,000 P/E cycles	 20 10 5	 — — —	 — — —	years

1. Operating temperature range is T_J from –40 °C to 150 °C. Typical endurance is evaluated at 25 °C.
2. Typical P/E cycles is 100,000 cycles for 128 KB and 256 KB blocks.
3. Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

3.20.2 WKUP/NMI timing

Table 35. WKUP/NMI glitch filter

No.	Symbol		Parameter	Min	Typ	Max	Unit
1	W_{FNMI}	D	NMI pulse width that is rejected	—	—	45	ns
2	W_{NFNMI}	D	NMI pulse width that is passed	205	—	—	ns

3.20.3 IEEE 1149.1 JTAG interface timing

Table 36. JTAG pin AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time	—	62.5	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at $V_{DDE}/2$)	—	40	60	%
3	$t_{TCKRISE}$	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	D	TCK low to TDO data valid	—	—	20	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	D	TCK low to TDO high impedance	—	—	20	ns
11	t_{BSDV}	D	TCK falling edge to output valid	—	—	50	ns
12	t_{BSDVZ}	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
13	t_{BSDHZ}	D	TCK falling edge to output high impedance	—	—	50	ns
14	t_{BSDST}	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
15	t_{BSDHT}	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

Figure 23. JTAG test clock input timing

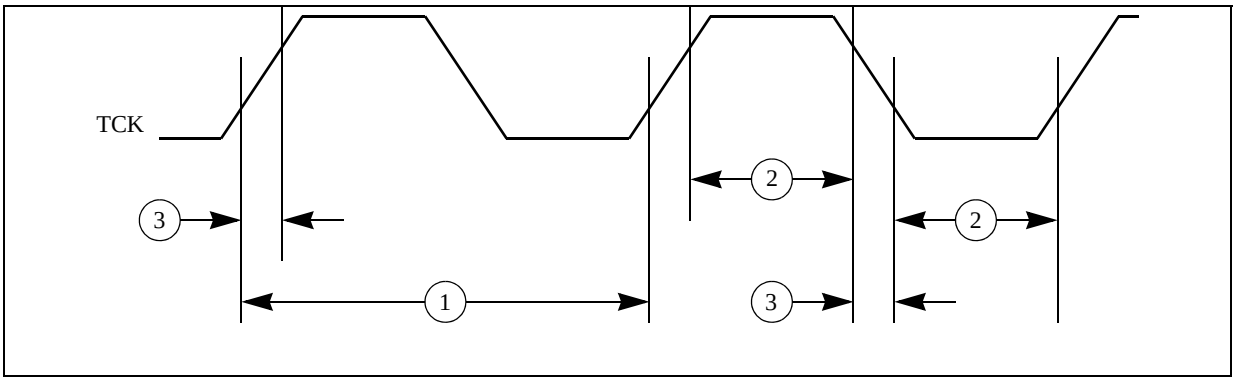
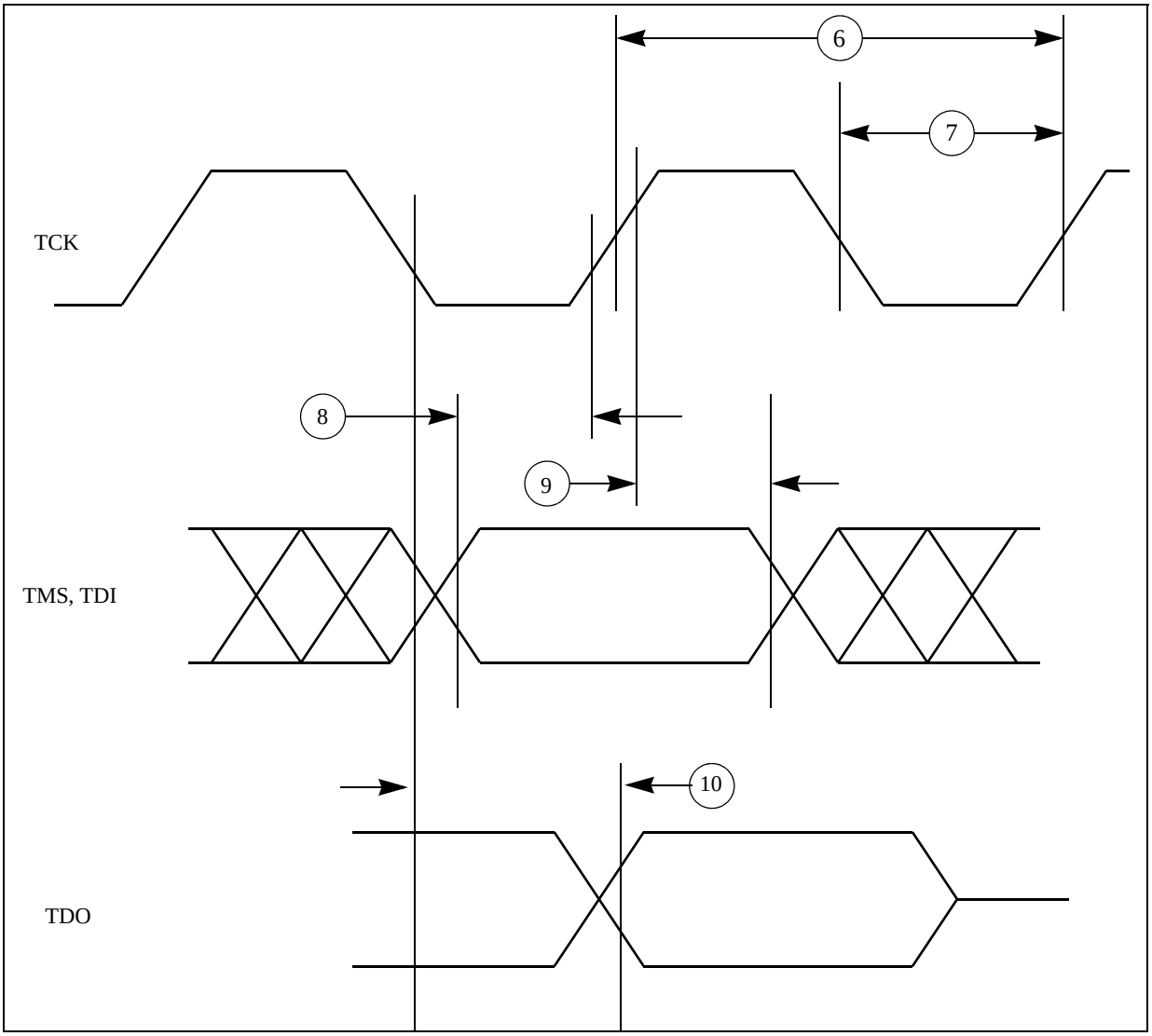


Figure 28. Nexus TDI, TMS, TDO timing



3.20.5 External interrupt timing (IRQ pin)

Table 38. External interrupt timing

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	D	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	D	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	D	IRQ edge to edge time(1)	—	6	—	t_{CYC}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

4 Package characteristics

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 Package mechanical data

Figure 39. LQFP100 package mechanical drawing