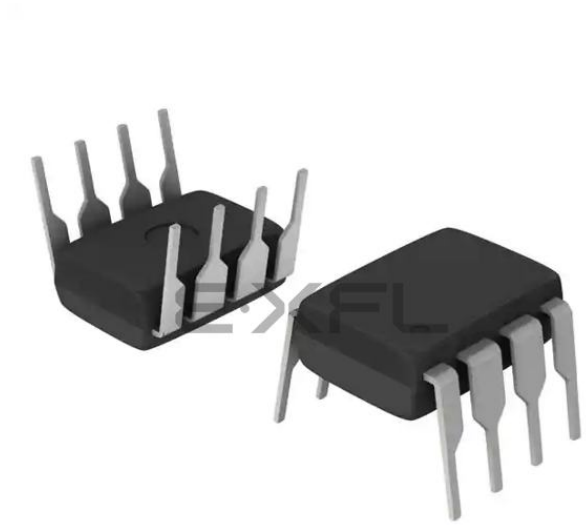

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	5
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7foxa0b6

Contents

Legend / Abbreviations for *Table 2*:

Type: I = input, O = output, S = supply

In/Output level:C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Output level: HS = 20 mA high sink (on N-buffer only)

Port and control configuration:

- Input: float = floating, wpu = weak pull-up, int = interrupt, ana = analog
- Output: OD = open drain, PP = push-pull

Note: The RESET configuration of each pin is shown in bold which is valid as long as the device is in reset state.

Table 2. Device pin description (8-pin package)

Pin No.	Pin Name	Type	Level		Port / Control						Main Function (after reset)	Alternate Function
					Input				Output			
			Input	Output	float	wpu	int	ana	OD	PP		
1	V_{DD} (1)	S									Main power supply	
2	PA5/AIN4/ CLKIN	I/O	C_T	HS	**X**	ei4		X	X	X	**Port A5**	Analog input 4 or External Clock Input
3	PA4/AIN3/MCO	I/O	C_T	HS	**X**	ei3		X	X	X	**Port A4**	Analog input 3 or Main clock output
4	PA3/$\overline{\text{RESET}}$ (2)	O				**X**			X	X	**Port A3**	RESET (2)
5	PA2/AIN2/LTIC	I/O	C_T	HS	**X**	ei2		X	X	X	**Port A2**	Analog input 2 or Lite Timer Input Capture
6	PA1/AIN1/ ICCCLK	I/O	C_T	HS	X	**ei1**		X	X	X	**Port A1**	Analog input 1 or In Circuit Communication Clock **Caution:** During normal operation this pin must be pulled-up, internally or externally (external pull-up of 10k mandatory in noisy environment). This is to avoid entering ICC mode unexpectedly during a reset. In the application, even if the pin is configured as output, any reset will put it back in pull-up
7	PA0/AIN0/ ATPWM/ ICCDATA	I/O	C_T	HS	**X**	ei0		X	X	X	**Port A0**	Analog input 0 or Auto-Reload Timer PWM or In Circuit Communication Data
8	V_{SS} (1)	S									Ground	

1. It is mandatory to connect all available V_{DD} and V_{DDA} pins to the supply voltage and all V_{SS} and V_{SSA} pins to ground.
2. After a reset, the multiplexed PA3/RESET pin will act as $\overline{\text{RESET}}$. To configure this pin as output (Port A3), write 55h to MUXCR0 and AAh to MUXCR1.

Table 3. ST7FOXA0 Hardware register map(1) (continued)

Address	Block	Register label	Register name	Reset status	Remarks
004Bh	DM (4)	DMCR	DM Control Register	00h	R/W
004Ch		DMSR	DM Status Register	00h	R/W
004Dh		DMBK1H	DM Breakpoint Register 1 High	00h	R/W
004Eh		DMBK1L	DM Breakpoint Register 1 Low	00h	R/W
004Fh		DMBK2H	DM Breakpoint Register 2 High	00h	R/W
0050h		DMBK2L	DM Breakpoint Register 2 Low	00h	R/W
0051h to 007Fh	Reserved area (47 bytes)				

1. Legend: x=undefined, R/W=read/write.
2. The contents of the I/O port DR registers are readable only in output configuration. In input configuration, the values of the I/O pins are returned instead of the DR register contents.
3. The bits associated with unavailable pins must always keep their reset value.
4. For a description of the Debug Module registers, see ICC protocol reference manual.

Depending on the ICP Driver code downloaded in RAM, Flash memory programming can be fully customized (number of bytes to program, program locations, or selection of the serial communication interface for downloading).

4.3.2 In Application Programming (IAP)

This mode uses an IAP Driver program previously programmed in Sector 0 by the user (in ICP mode).

This mode is fully controlled by user software. This allows it to be adapted to the user application, (user-defined strategy for entering programming mode, choice of communications protocol used to fetch the data to be stored etc.)
IAP mode can be used to program any memory areas except Sector 0, which is Write/Erase protected to allow recovery in case errors occur during the programming operation.

4.4 ICC interface

ICP needs a minimum of 4 and up to 6 pins to be connected to the programming tool. These pins are:

- $\overline{\text{RESET}}$: device reset
- V_{SS}: device power supply ground
- ICCCLK: ICC output serial clock pin
- ICCDATA: ICC input serial data pin
- OSC1: main clock input for external source
- V_{DD}: application board power supply (optional, see Note 3)

Note: 1 If the ICCCLK or ICCDATA pins are only used as outputs in the application, no signal isolation is necessary. As soon as the Programming Tool is plugged to the board, even if an ICC session is not in progress, the ICCCLK and ICCDATA pins are not available for the application. If they are used as inputs by the application, isolation such as a serial resistor has to be implemented in case another device forces the signal. Refer to the Programming Tool documentation for recommended resistor values.

2 During the ICP session, the programming tool must control the $\overline{\text{RESET}}$ pin. This can lead to conflicts between the programming tool and the application reset circuit if it drives more than 5mA at high level (push pull output or pull-up resistor<1 kΩ). A schottky diode can be used to isolate the application RESET circuit in this case. When using a classical RC network with R>1 kΩ or a reset management IC with open drain output and pull-up resistor>1 kΩ, no additional components are needed. In all cases the user must ensure that no external reset is generated by the application during the ICC session.

3 The use of pin 7 of the ICC connector depends on the Programming Tool architecture. This pin must be connected when using most ST Programming Tools (it is used to monitor the application power supply). Please refer to the Programming Tool manual.

4 In "enabled option byte" mode (38-pulse ICC mode), the internal RC oscillator is forced as a clock source, regardless of the selection in the option byte. In "disabled option byte" mode (35-pulse ICC mode), pin 9 has to be connected to the CLKIN pin of the ST7 when the clock is not available in the application or if the selected clock option is not programmed in the option byte.

5 A serial resistor must be connected to ICC connector pin 6 in order to prevent contention on PA3/RESET pin. Contention may occur if a tool forces a state on RESET pin while PA3 pin forces the opposite state in output mode. The resistor value is defined to limit the current

4.5 Memory protection

There are two different types of memory protection: Read-Out Protection and Write/Erase Protection which can be applied individually.

4.5.1 Read-out protection

Read-Out Protection, when selected provides a protection against program memory content extraction and against write access to Flash memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

- In Flash devices, this protection is removed by reprogramming the option. In this case, the program memory is automatically erased and the device can be reprogrammed. The read-out protection is enabled and removed through the FMP_R bit in the option byte.

4.5.2 Flash write/erase protection

Write/Erase Protection, when set, makes it impossible to both overwrite and erase program memory. Its purpose is to provide advanced security to applications and prevent any change being made to the memory content. Write/Erase Protection is enabled through the FMP_W bit in the option byte.

Caution: **Once set, Write/Erase Protection can never be removed. A write-protected Flash device is no longer reprogrammable.**

4.6 Related documentation

For details on Flash programming and ICC protocol, refer to the ST7 Flash Programming Reference Manual and to the ST7 ICC Protocol Reference Manual.

5 Central processing unit

5.1 Introduction

This CPU has a full 8-bit architecture and contains six internal registers allowing efficient 8-bit data manipulation.

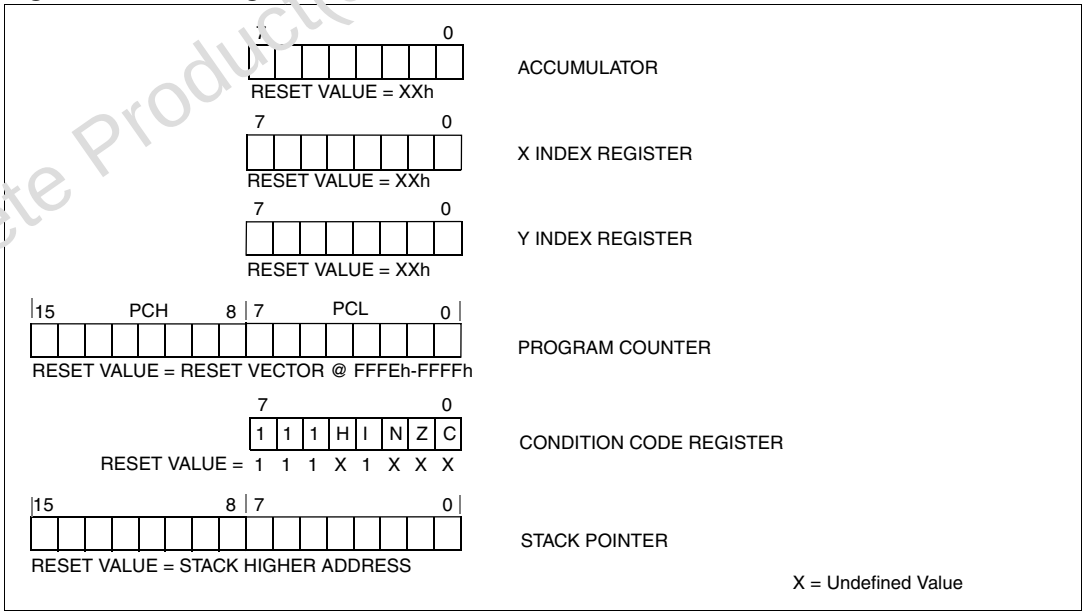
5.2 Main features

- 63 basic instructions
- Fast 8-bit by 8-bit multiply
- 17 main addressing modes
- Two 8-bit index registers
- 16-bit stack pointer
- Low power modes
- Maskable hardware interrupts
- Non-maskable software interrupt

5.3 CPU registers

The six CPU registers shown in *Figure 5*. They are not present in the memory mapping and are accessed by specific instructions.

Figure 5. CPU registers

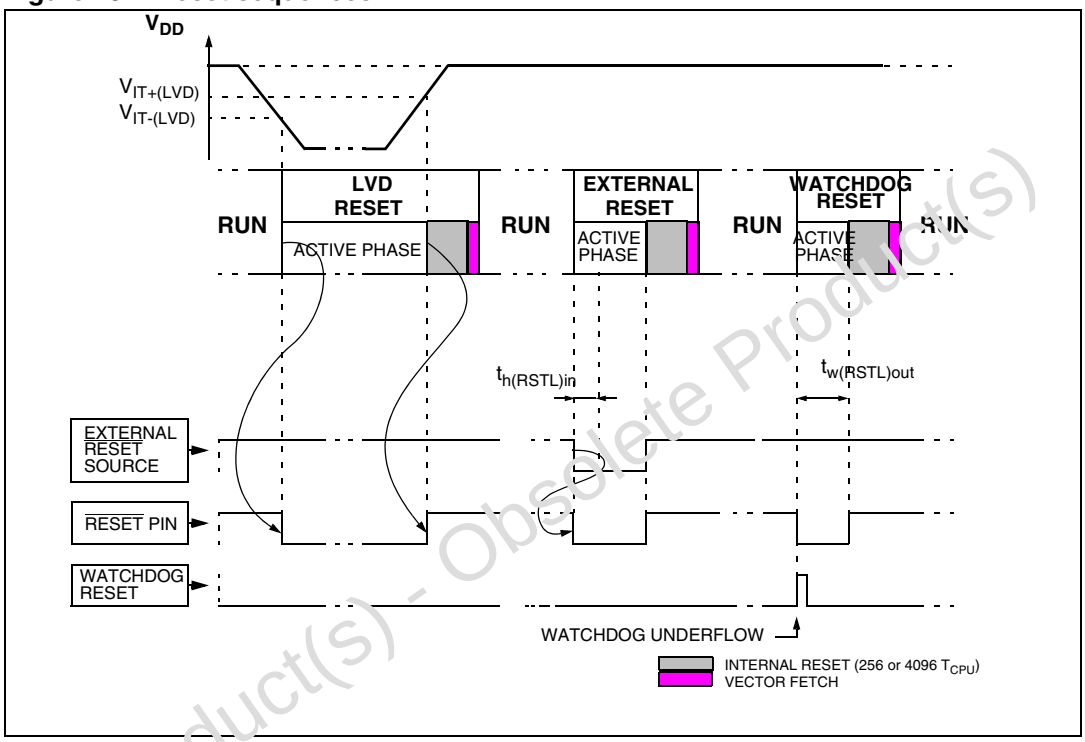


6.3.5 Internal watchdog reset

The Reset sequence generated by an internal watchdog counter overflow is shown in *Figure 13: Reset sequences*

Starting from the watchdog counter underflow, the device $\overline{\text{RESET}}$ pin acts as an output that is pulled low during at least $t_{w(RSTL)out}$.

Figure 13. Reset sequences



6.4 System Integrity management (SI)

The System Integrity Management block contains the Low voltage Detector (LVD).

Note: A reset can also be triggered following the detection of an illegal opcode or prebyte code. Refer to Section 10.2.1 on page 84 for further details.

6.4.1 Low Voltage Detector (LVD)

The Low Voltage Detector function (LVD) generates a static reset when the V_{DD} supply voltage is below a $V_{IT-(LVD)}$ reference value. This means that it secures the power-up as well as the power-down keeping the ST7 in reset.

The $V_{IT-(LVD)}$ reference value for a voltage drop is lower than the $V_{IT+(LVD)}$ reference value for power-on in order to avoid a parasitic reset when the MCU starts running and sinks current on the supply (hysteresis).

The LVD Reset circuitry generates a reset when V_{DD} is below:

- $V_{IT+(LVD)}$ when V_{DD} is rising
- $V_{IT-(LVD)}$ when V_{DD} is falling

The LVD function is illustrated in *Figure 14*.

The voltage threshold can be enabled/disabled by option byte. See *Section 13.1 on page 110*.

Provided the minimum V_{DD} value (guaranteed for the oscillator frequency) is above $V_{IT-(LVD)}$, the MCU can only be in two modes:

- Under full software control
- In static safe reset

In these conditions, secure operation is always ensured for the application without the need for external reset hardware.

During a Low Voltage Detector Reset, the $\overline{\text{RESET}}$ pin is held low, thus permitting the MCU to reset other devices.

Note: Use of LVD with capacitive power supply: with this type of power supply, if power cuts occur in the application, it is recommended to pull V_{DD} down to 0 V to ensure optimum restart conditions. Refer to circuit example in Figure 39 on page 106 and note 4.

The LVD is an optional function which can be selected by option byte. See Section 13.1 on page 110.

It allows the device to be used without any external RESET circuitry.

If the LVD is disabled, an external circuitry must be used to ensure a proper power-on reset.

It is recommended to make sure that the V_{DD} supply voltage rises monotonously when the device is exiting from Reset, to ensure the application functions properly.

Caution: If an LVD reset occurs after a watchdog reset has occurred, the LVD will take priority and will clear the watchdog flag.

6.5 Register description

6.5.1 RC calibration control/status register (RCC_CSR)

Reset value: 0000 0000 (00h)

7							0
0	0	0	0	0	0	RCCLAT	RCCPGM
Read/write							

Bits 7:2 = Reserved, forced by hardware to 0

0: Read mode

1: Write mode

Bit 1 = **RCCLAT** *Latch Access Transfer bit:* this bit is set by software.

It is cleared by hardware at the end of the programming cycle. It can only be cleared by software if the RCCPGM bit is cleared

Bit 0 = **RCCPGM** *Programming Control and Status bit*

This bit is set by software to begin the programming cycle. At the end of the programming cycle, this bit is cleared by hardware.

0: Programming finished or not yet started

1: Programming cycle is in progress

Note: *If the RCCPGM bit is cleared during the programming cycle, the memory data is not guaranteed.*

6.5.2 Main Clock Control/Status Register (MCCSR)

Reset value: 0000 0000 (00h)

7							0
0	0	0	0	0	0	MCO	SMS
Read/write							

Bits 7:2 = Reserved, must be kept cleared.

Bit 1 = **MCO** *Main Clock Out enable bit*

This bit is read/write by software and cleared by hardware after a reset. This bit allows to enable the MCO output clock.

0: MCO clock disabled, I/O port free for general purpose I/O.

1: MCO clock enabled.

Bit 0 = **SMS** *Slow mode selection bit*

This bit is read/write by software and cleared by hardware after a reset. This bit selects the input clock f_{OSC} or $f_{OSC}/32$.

0: Normal mode ($f_{CPU} = f_{OSC}$

1: Slow mode ($f_{CPU} = f_{OSC}/32$)

As soon as Halt mode is entered, and if the AWUEN bit has been set in the AWUCSR register, the AWU RC oscillator provides a clock signal (f_{AWU_RC}). Its frequency is divided by a fixed divider and a programmable prescaler controlled by the AWUPR register. The output of this prescaler provides the delay time. When the delay has elapsed, the following actions are performed:

- the AWUF flag is set by hardware,
- an interrupt wakes-up the MCU from Halt mode,
- the main oscillator is immediately turned on and the 256 CPU cycle delay is used to stabilize it.

After this start-up delay, the CPU resumes operation by servicing the AWUFH interrupt. The AWU flag and its associated interrupt are cleared by software reading the AWUCSR register.

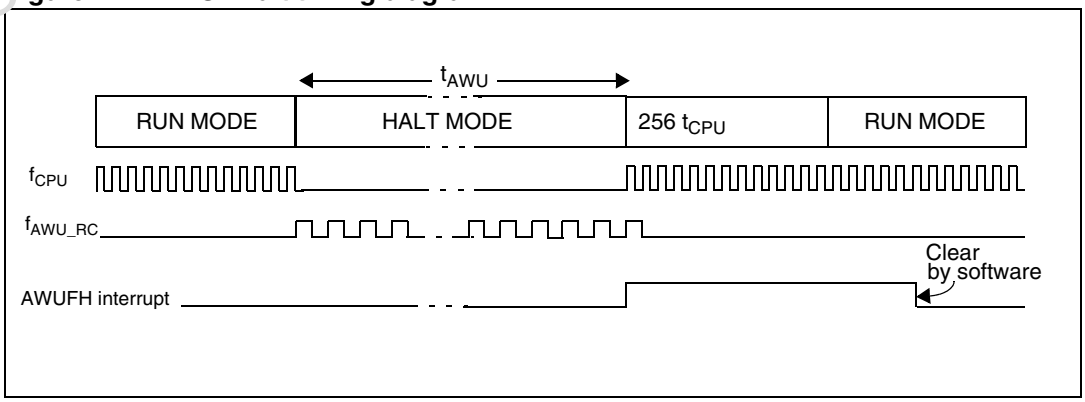
To compensate for any frequency dispersion of the AWU RC oscillator, it can be calibrated by measuring the clock frequency f_{AWU_RC} and then calculating the right prescaler value. Measurement mode is enabled by setting the AWUM bit in the AWUCSR register in Run mode. This connects f_{AWU_RC} to the Input Capture of the 8-bit Lite timer, allowing the f_{AWU_RC} to be measured using the main oscillator clock as a reference timebase.

Similarities with halt mode

The following AWUFH mode behavior is the same as normal Halt mode:

- The MCU can exit AWUFH mode by means of any interrupt with exit from Halt capability or a reset (see *Section 7.4: Active-halt and halt modes*).
- When entering AWUFH mode, the I bit in the CC register is forced to 0 to enable interrupts. Therefore, if an interrupt is pending, the MCU wakes up immediately.
- In AWUFH mode, the main oscillator is turned off causing all internal processing to be stopped, including the operation of the on-chip peripherals. None of the peripherals are clocked except those which get their clock supply from another clock generator (such as an external or auxiliary oscillator like the AWU oscillator).
- The compatibility of watchdog operation with AWUFH mode is configured by the WDGHALT option bit in the option byte. Depending on this setting, the HALT instruction when executed while the watchdog system is enabled, can generate a watchdog Reset.

Figure 24. AWUF halt timing diagram



Bits 15:12 = Reserved, must be kept cleared.

Bits 11:0 = **DCR[11:0]** *PWMx Duty Cycle Value*

This 12-bit value is written by software. The high register must be written first.

In PWM mode (OE0=1 in the PWMCR register) the DCR[11:0] bits define the duty cycle of the PWM0 output signal (see *Figure 32*). In Output Compare mode, (OE0=0 in the PWMCR register) they define the value to be compared with the 12-bit upcounter value.

PWM0 control/status register (PWM0CSR)

Reset value: 0000 0000 (00h)

7							0
0	0	0	0	0	0	OP0	CMPF0
Read/Write							

Bits 7:2 = Reserved, must be kept cleared.

Bit 1 = **OP0** *PWM0 Output Polarity.*

This bit is read/write by software and cleared by hardware after a reset. This bit selects the polarity of the PWM0 signal.
0: The PWM0 signal is not inverted.
1: The PWM0 signal is inverted.

Bit 0 = **CMPF0** PWM0 *Compare Flag.*

This bit is set by hardware and cleared by software by reading the PWM0CSR register. It indicates that the upcounter value matches the DCR0 register value.
0: Upcounter value does not match DCR value.
1: Upcounter value matches DCR value.

PWM output control register (PWMCR)

Reset value: 0000 0000 (00h)

7							0
0	0	0	0	0	0	0	OE0
Read/Write							

Bits 7:1 = Reserved, must be kept cleared.

Bit 0 = **OE0** *PWM0 Output enable*.

9.3 10-bit A/D converter (ADC)

9.3.1 Introduction

The on-chip Analog to Digital Converter (ADC) peripheral is a 10-bit, successive approximation converter with internal sample and hold circuitry. This peripheral has up to 5 multiplexed analog input channels (refer to device pin out description) that allow the peripheral to convert the analog voltage levels from up to 5 different sources.

The result of the conversion is stored in a 10-bit Data register. The A/D converter is controlled through a Control/Status register.

9.3.2 Main features

- 10-bit conversion
- Up to 5 channels with multiplexed input
- Linear successive approximation
- Data register (DR) which contains the results
- Conversion complete status flag
- On/off bit (to reduce consumption)

The block diagram is shown in *Figure 34*.

9.3.3 Functional description

Analog power supply

V_{DDA} and V_{SSA} are the high and low level reference voltage pins. In some devices (refer to device pin out description) they are internally connected to the V_{DD} and V_{SS} pins.

Conversion accuracy may therefore be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines.

Table 36. Illegal opcode detection (continued)

Mnemo	Description	Function/Example	Dst	Src		H	I	N	Z	C
WFI	Wait for Interrupt						0			
XOR	Exclusive OR	A = A XOR M	A	M				N	Z	

11.3.1 External Interrupt Control Register 1 (EICR1)

Reset value: 0000 0000 (00h)

7							0
0	0	IS21	IS20	IS11	IS10	IS01	IS00
Read/write							

Bits 7:6 = Reserved, must be kept cleared.

Bits 5:4 = **IS2[1:0]** *ei2 sensitivity bits*

These bits define the interrupt sensitivity for ei2 according to *Table ?*.

Bits 3:2 = **IS1[1:0]** *ei1 sensitivity bits*

These bits define the interrupt sensitivity for ei1 according to *Table ?*.

Bits 1:0 = **IS0[1:0]** *ei0 sensitivity bits*

These bits define the interrupt sensitivity for ei0 according to *Table ?*.

Note: 1 These 8 bits can be written only when the I bit in the CC register is set.

2 Changing the sensitivity of a particular external interrupt clears this pending interrupt. This can be used to clear unwanted pending interrupts. Refer to Section : External interrupt function.

3 Whatever the sensitivity configuration, ei2 cannot exit the MCU from HALT, ACTIVE-HALt and AWUFH modes when a falling edge occurs.

ISx1	ISx0	External interrupt sensitivity
0	0	Falling edge & low level
0	1	Rising edge only
1	0	Falling edge only
1	1	Rising and falling edge

12 Electrical characteristics

12.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

12.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean+3Σ).

12.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5 V (for the 4.5 V≤ V_{DD}≤ 5.5 V voltage range). They are given only as design guidelines and are not tested.

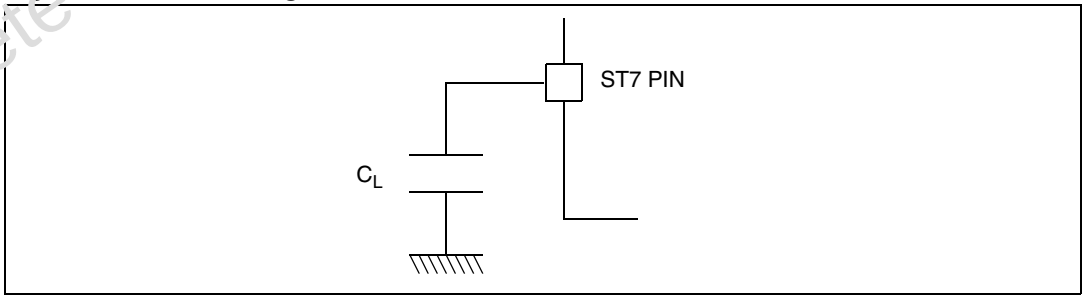
12.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

12.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 36*.

Figure 36. Pin loading conditions



12.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 37*.

12.6 Memory characteristics

T_A = -40 °C to 85 °C, unless otherwise specified.

Table 49. RAM and hardware registers characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode(1)	Halt mode (or Reset)	1.6			V

1. Minimum V_{DD} supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by construction, not tested in production.

Table 50. Flash program memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage for Flash Write/Erase	Refer to operating range of V_{DD} with T_A, *Section 12.3.1 on page 95*	4.5		5.5	V
t_{prog}	Programming time for 1~32 bytes(1)	T_A=–40 to +85 °C		5	10	ms
	Programming time for 4 kbytes	T_A=+25 °C		0.64	1.28	s
t_{RET}	Data retention(2)	T_A=+55 °C(3)	20			years
N_{RW}	Write erase cycles	T_A=+25 °C			1k	cycles
I_{DD}	Supply current(4)	Read / Write / Erase modes f_{CPU} = 8 MHz, V_{DD} = 5.5 V			2.6	mA
		No Read/No Write mode			100	µA
		Power down mode / Halt		0	0.1	µA

1. Up to 32 bytes can be programmed at a time.
2. Data based on reliability test results and monitored in production.
3. The data retention time increases when the T_A decreases.
4. Guaranteed by Design. Not tested in production.

Table 62. Development tool order codes

MCU	Debugging and programming tool	ST socket boards
ST7FOXA0M6 ST7FOXA0B6	STX-RLINK(1)(2), ST7-STICK(3)(4), EMU3 or STice emulator(5)	ST7SB10-SU0 socket board(3)

1. USB connection to PC.
2. Available from ST or from Raisonance, www.raisonance.com.
3. Add suffix /EU, /UK or /US for the power supply for your region.
4. Parallel port connection to PC.
5. Contact local ST sales office for sales types.

13.4 ST7 application notes

Table 63. ST7 application notes

Identification	Description
Application examples	
AN1658	Serial numbering implementation
AN1720	managing the Read-Out Protection in Flash microcontrollers
AN1755	A high resolution/precision thermometer using ST7 and NE555
AN1756	Choosing a DALI implementation strategy with ST7DALI
AN1812	A high precision, low cost, single supply ADC for positive and negative input voltages
Example drivers	
AN 969	SCI communication between ST7 and PC
AN 970	SPI communication between ST7 and EEPROM
AN 971	I²C communication between ST7 and M24Cxx EEPROM
AN 972	ST7 software SPI master communication
AN 973	SCI software communication with a PC using ST72251 16-bit timer
AN 974	Real time clock with ST7 timer Output Compare
AN 976	Driving a buzzer through ST7 timer PWM function
AN 979	Driving an analog keyboard with the ST7 ADC
AN 980	ST7 keypad decoding techniques, implementing wakeup on keystroke
AN1017	Using the ST7 Universal Serial Bus microcontroller
AN1041	Using ST7 PWM signal to generate analog output (sinusoïd)
AN1042	ST7 routine for I²C Slave mode Management
AN1044	Multiple interrupt sources management for ST7 MCUs
AN1045	ST7 S/W implementation of I²C bus master

14 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.